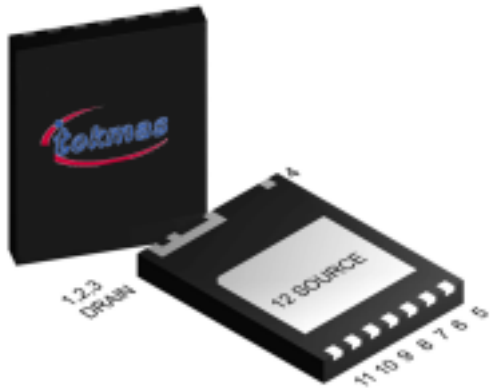
High-Performance 650-V GaN Transistor with Integrated Gate Driver

Features

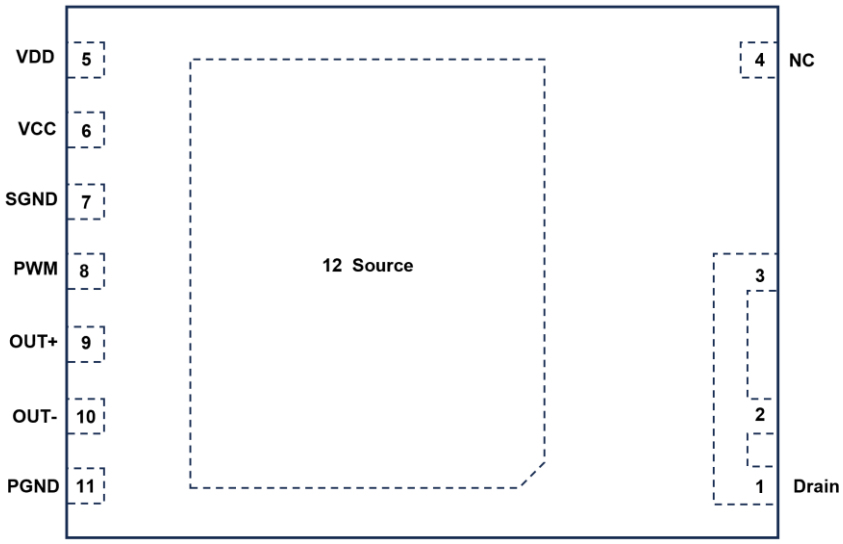
- GaN transistors with integrated gate drive
- 750V Transient Voltage Rating
- 650 V Continuous Voltage Rating
- Zero reverse recovery charge
- Typ./Max. $R_{DS(ON)}$ = 140/190 mΩ
- Wide logic input range with hysteresis
- Wide power supply range (10 V ~ 18 V)
- Internal regulator for stable gate drive voltage
- Independent SGND and PGND design
- Programmable turn-on dV/dt
- UVLO protection
- ESD protection of 2 kV (HBM), 1 kV (CDM)
- Up to 2 MHz operation
- 6*8 mm footprint with large cooling pad
- Minimized package inductance

Typical applications

- AC-DC, DC-DC, DC-AC
- Buck, boost, half bridge, full bridge
- Active Clamp Flyback, LLC resonant, Class D
- Quasi-Resonant Flyback
- Mobile fast-chargers, adapters
- LED lighting, solar micro-inverters
- TV / monitor, wireless power
- Server, telecom & networking SMPS



Pin configuration and functions



Package Top View

Pin #	Name	I/O	Description
1,2,3	D	P	Drain of GaN transistor
4	-	NC	Not connected
5	VDD	I	Gate driver supply voltage
6	VCC	P	Logic supply voltage
7	SGND	G	Logic ground
8	PWM	I	Logic input
9	OUT+	-	Gate driver turn-on current set pin (Using R_{gon})
10	OUT-	-	Gate driver turn-on current set pin (Using R_{gon})
11	PGND	G	Gate driver ground. Internally connected to S
12	S	O, G	Source of GaN transistor

I = Input, O = Output, P = Power, G = Ground, NC = No Connect

Ordering information

Ordering No.	Description
CID12N65D	DFN6*8, 2500 pcs/reel

1 Absolute maximum ratings

At T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate product lifetime. For further information, contact Tokmas sales office.

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
V_{CC}-SGND voltage	V_{CC}	-0.3	-	24	V	
V_{DD}-PGND voltage	V_{DD}	-0.3	-	7	V	
SGND-PGND voltage	V_{SP}	-5	-	5	V	
Continuous current, drain-source	I_D	-	-	11.5	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	20.5	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	11.5	A	T_c = 125 °C
Operating temperature	T_j	-40	-	125	°C	
Storage temperature	T_{stg}	-55	-	150	°C	

Notes

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.

2. Pulse width = 10 μs.

2 Recommended operating conditions

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
V_{DD}-SGND voltage	V_{DD}	10		18	V	
PWM input pin voltage	V_{PWM}	0		18	V	
Gate driver turn-on set resistance	R_{DD}	10			Ω	
Junction temperature	T_j	-40	-	+125	°C	
Ambient temperature	T_a	-40	-	+125	°C	

3 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	-	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

4 Electrical characteristics

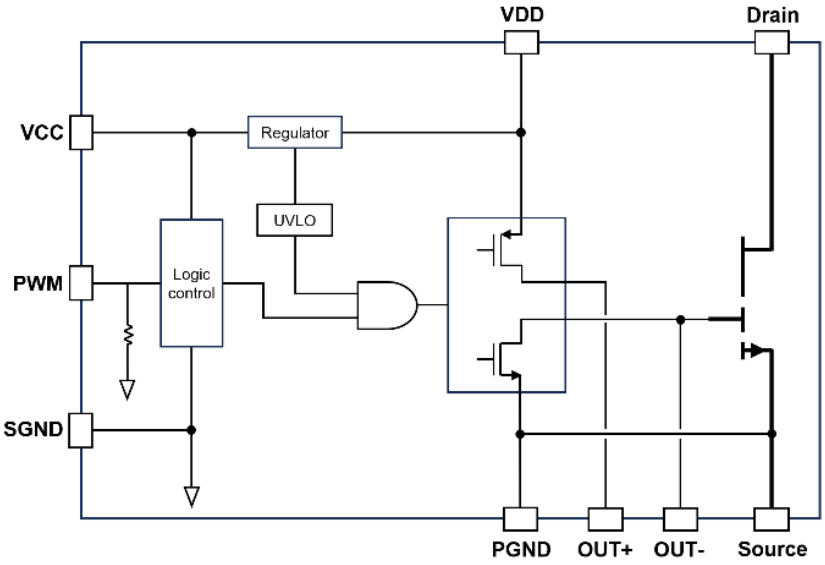
at V_{CC} = 12 V, F_{SW} = 500 kHz, T_j = 25 °C, unless specified otherwise.

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
V_{CC} Supply Characteristics						
V_{CC} quiescent current	I_{QCC}		0.42		mA	V_{PWM} = 0 V
V_{CC} operating current	I_{QCC-SW}		1		mA	F_{SW} = 500 kHz; V_{DS} = open
V_{CC} UVLO rising threshold	V_{CC-ON}	8.1	8.4	8.8	V	
V_{CC} UVLO falling threshold	V_{CC-OFF}	7.5	7.8	8.1	V	
V_{CC} UVLO hysteresis	V_{CC-HYS}	0.4	0.6	-	V	
Low-side logic input Characteristics						
Input pin pull-down resistance	R_{PWM-PD}		200		kΩ	
Input pin high logic bias current	I_{PWM-H}		20		μA	
Input logic high threshold (rising edge)	V_{PWMH}	1.7	2.1	2.5	V	
Input logic low threshold (falling edge)	V_{PWML}	0.9	1.2	1.5	V	
Input logic hysteresis	V_{I-HYS}	0.8	0.9		V	
Turn-on propagation delay	T_{ON}		30	60	ns	
Turn-off propagation delay	T_{OFF}		30	60	ns	
Drain rise time	T_R		5		ns	
Drain fall time	T_F		3		ns	
Switching Characteristics						
Switching frequency	F_{SW}			2	MHz	
Pulse width	T_{PW}	0.02		1000	μs	
GaN FET Characteristics						
Drain-source leakage current	I_{DSS}	-	-	10	μA	V_{DS} = 650V; V_{PWM} = 0; T_j = 25°C
		-	-	50		V_{DS} = 650V; V_{PWM} = 0; T_j = 125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	138	190	mΩ	V_{PWM} = 12V; I_D = 4A; T_j = 25 °C
		-		-	mΩ	V_{PWM} = 12V; I_D = 4A; T_j = 125 °C
Source-drain reverse voltage	V_{SD}	-	2.6	-	V	V_{PWM} = 0 V; I_{SD} = 4 A
Output charge	Q_{OSS}	-	24.5	-	nC	V_{PWM} = 0 V; V_{DS} = 0 to 400 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 4 A; V_{DS} = 400 V
Output capacitance	C_{oss}	-	30	-	pF	V_{PWM} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	43	-	pF	V_{PWM} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	60	-	pF	V_{PWM} = 0 V; V_{DS} = 0 to 400 V

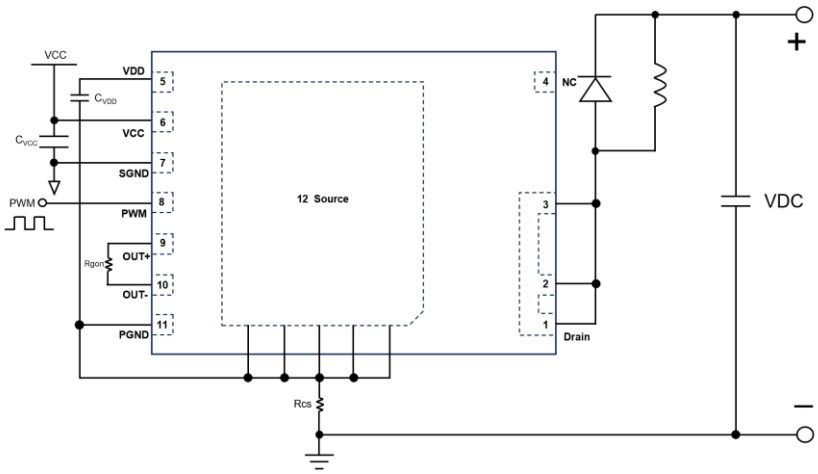
Notes

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

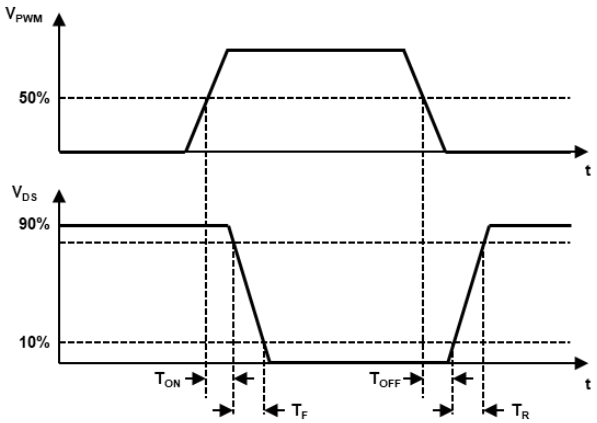
5 Block diagram



6 Switching waveforms



Inductive-load switching circuit

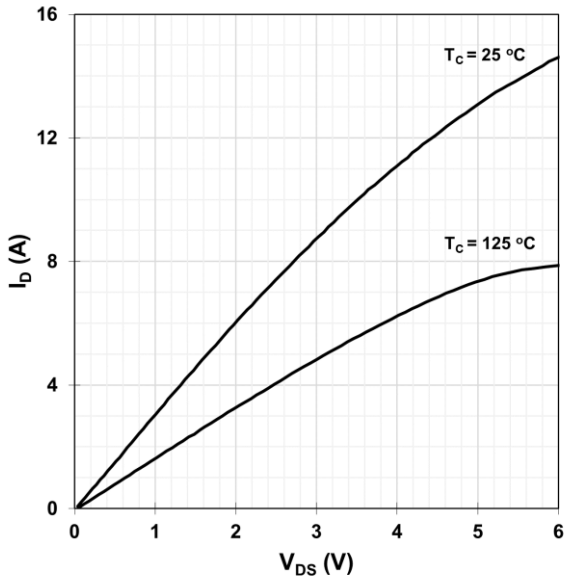


Propagation delay and rise/fall time definitions

7 Electrical characteristics diagrams

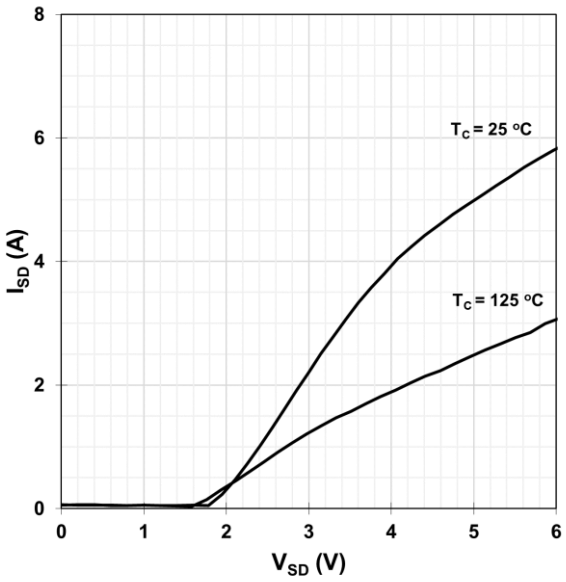
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



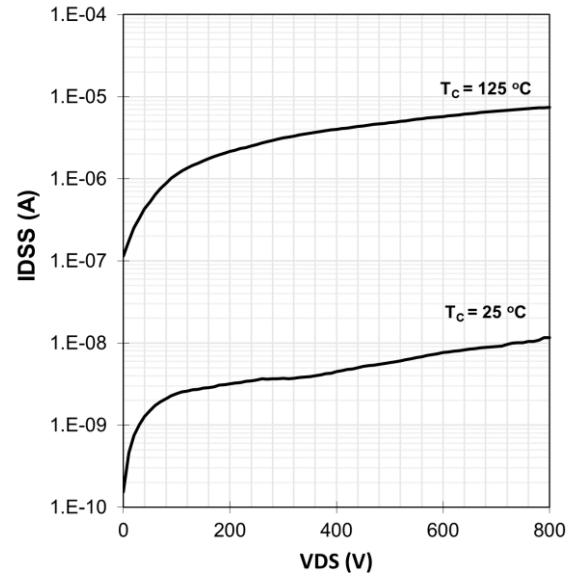
$I_D = f(V_{DS})$; V_{PWM} = 12 V

Figure 2 Typ. channel reverse characteristics



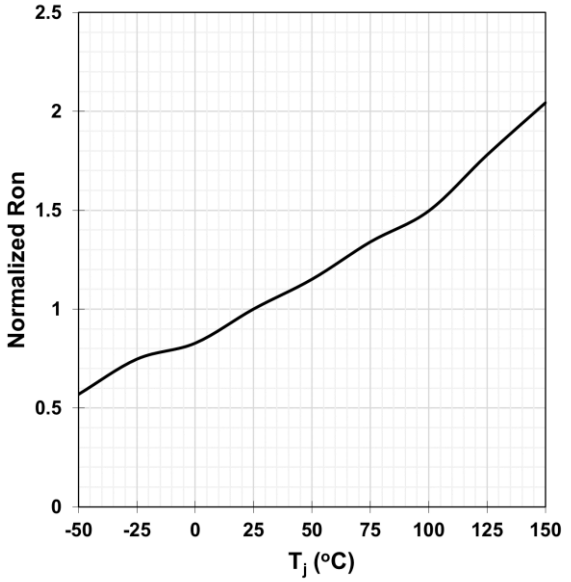
$I_{SD} = f(V_{SD})$; V_{PWM} = 0 V

Figure 3 Typ. drain-source leakage characteristics



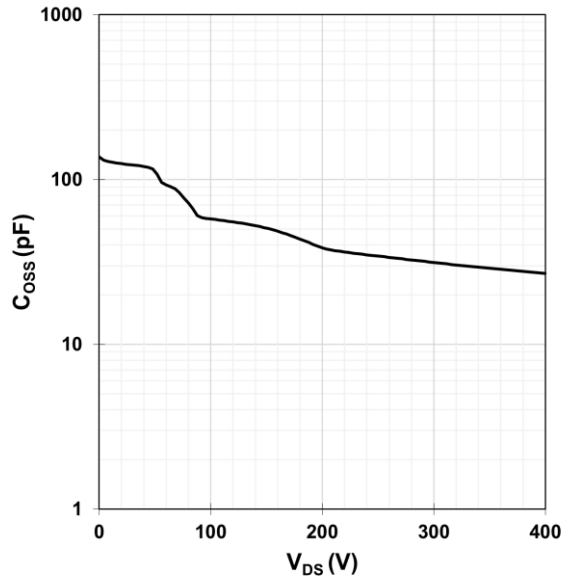
$I_{DSS} = f(V_{DS})$; V_{PWM} = 0 V

Figure 4 Typ. drain-source on-state resistance



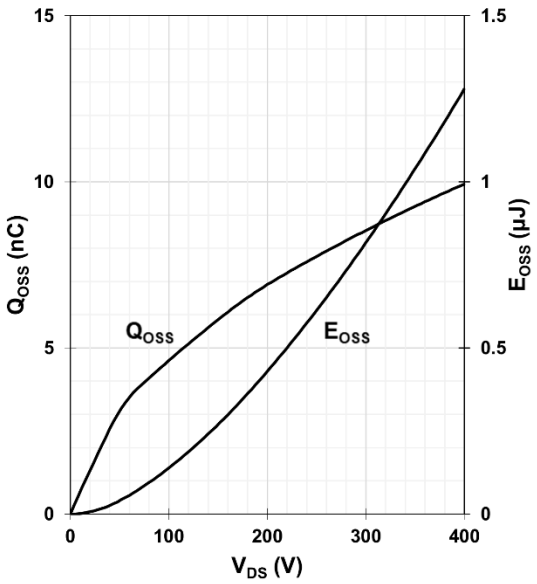
$R_{DS(on)} = f(T_j)$; I_D = 2 A; V_{PWM} = 0 V

Figure 5 Typ. output capacitance



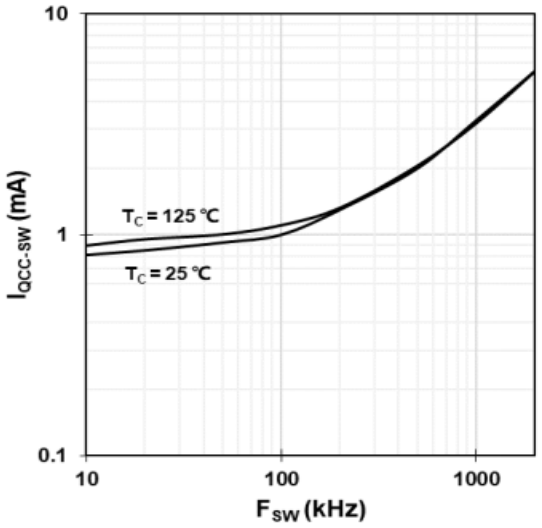
C_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 6 Typ. C_{OSS} stored energy



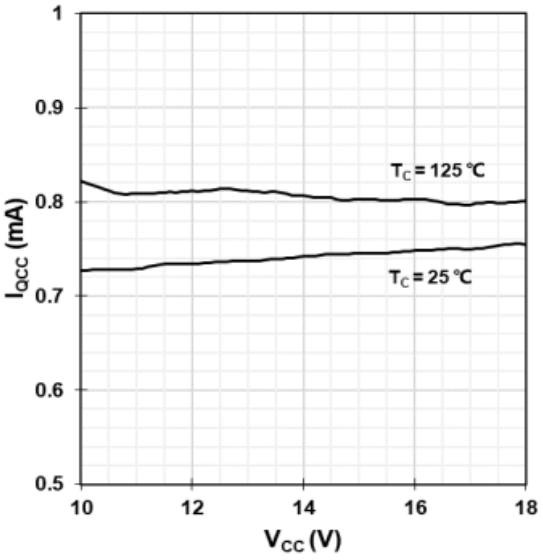
Q_{OSS} = f(V_{DS}); E_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 7 VCC operating current (I_{QCC-SW}) vs. f_{SW}



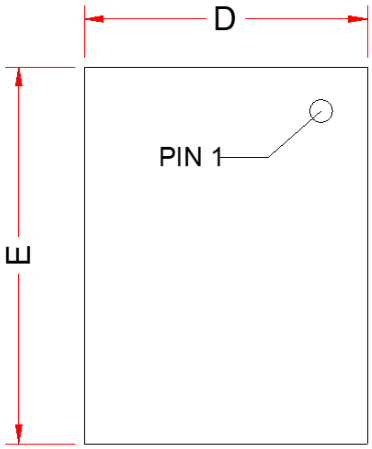
VCC = 12 V, V_{PWM} = 0 V

Figure 8 VCC quiescent current (I_{QCC}) vs. VCC

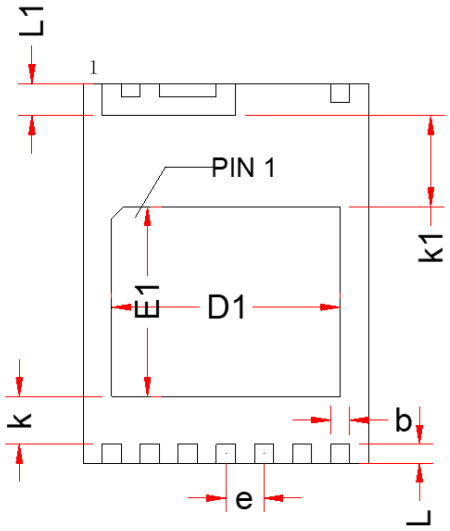


V_{PWM} = 0 V

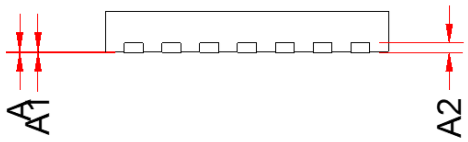
8 Package outlines



TOP VIEW



BOTTOM VIEW



SIDE VIEW

	MIN	MID	MAX
A	0.800	0.850	0.950
A1	0.000	0.020	0.050
A2		0.203REF	
b	0.350	0.400	0.450
D		6.00BSC	
D1	4.750	4.800	4.850
E		8.00BSC	
E1	3.950	4.000	4.050
e		0.800BSC	
k	0.900	1.000	1.100
k1	1.825	1.925	2.025
L	0.350	0.400	0.450
L1	0.625	0.675	0.725

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