

# LED EMULATOR INPUT OPEN COLLECTOR OUTPUT ISOLATORS

## FEATURES

Pin to pin compatible with popular High-Speed optocouplers

High data rates 10Mbps

High common-mode transient immunity: 50kV/ $\mu$ s typical

High robustness to radiated and conducted noise

Diode emulator input

4.5V-26.4V open collector output

Propagation delay 65ns

3750Vrms/5000Vrms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

DIN V VDE V 0884-11:2017-01

$V_{IORM} = 1200V$  peak

Wide temperature range: -40°C to 125°C

RoHS-compliant, DIP-8/NB SOIC-8 package

## APPLICATIONS

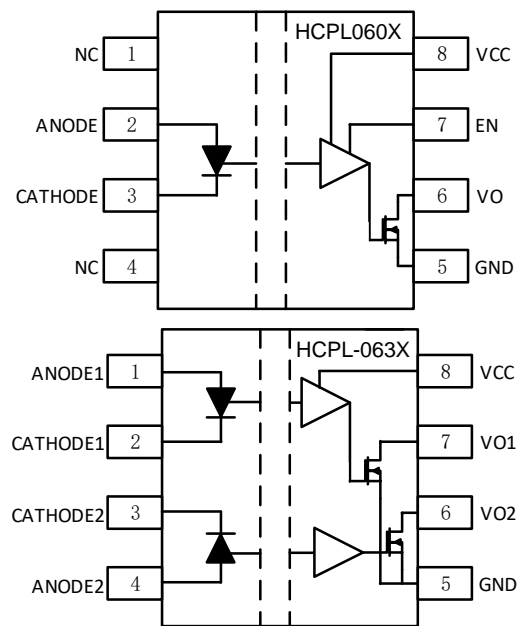
General-purpose isolation

Industrial field bus isolation

Motor controls and drives

EV traction inverters

## FUNCTIONAL BLOCK DIAGRAMS



SOIC-8, DIP-8

Open Collector Output

Figure1. HCPL060X/HCPL-063XXX functional Block Diagram

## SELECTION GUIDE

**Table 1. Selection guide**

Model Name <sup>1</sup>	Temperature Range	No. of channels	Data rate (Mbps)	Isolation Rating (kV rms)	Package
HCPL0602R2	-40~125°C	1	1	3750	NB SOIC-8
HCPL0601R2	-40~125°C	1	10	3750	NB SOIC-8
HCPL-0630-400E	-40~125°C	2	1	3750	NB SOIC-8
HCPL-0630-500E	-40~125°C	2	10	3750	NB SOIC-8
HCPL0602R3	-40~125°C	1	1	5000	DIP-8
HCPL0601R3	-40~125°C	1	10	5000	DIP-8
HCPL-0630-400C	-40~125°C	2	1	5000	DIP-8
HCPL-0630-500C	-40~125°C	2	10	5000	DIP-8

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

**Table 2. Absolute Maximum Ratings**

Parameter	Rating
<b>INPUT</b>	
Average forward current (I <sub>F</sub> )	20mA
Reverse input voltage (V <sub>R</sub> )	5 V (min)
Enable input voltage (V <sub>E</sub> )	V <sub>DD</sub> + 0.5 V
Input Power Dissipation (P <sub>I</sub> )	90mW
<b>OUTPUT</b>	
Supply voltage (V <sub>DD</sub> )	27V
Output sink current (I <sub>SINK</sub> )	50mA
Output voltage (V <sub>O</sub> )	27V
Output power dissipation (P <sub>diss</sub> )	50mW
<b>ISOLATOR</b>	
Total Power Dissipation (P <sub>T</sub> )	140mW
HBM Rating ESD	±4KV
Maximum Isolation Voltage DIP-8	5000V <sub>RMS</sub>
Maximum Isolation Voltage SO-8	3750V <sub>RMS</sub>
Storage Temperature (T <sub>STG</sub> )	-65°C to +150°C
Operating Temperature (T <sub>A</sub> )	-40°C to +125°C
Junction Temperature (T <sub>J</sub> )	+150°C

## RECOMMENDED OPERATING CONDITIONS

**Table 3. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5		26.4	V
Input Current, low level each channel	I <sub>F(OFF)</sub>	0		250	μA
Input Current, high level each channel	I <sub>F(ON)</sub>	3		15	mA
Enable Voltage, Low Level	V <sub>EL</sub>	0		0.8	V
Enable Voltage, High Level	V <sub>EH</sub>	2		V <sub>DD</sub>	V
Output Pull-up Resistor	RL	330		4k	Ω

Ambient Operating Temperature	$T_A$	-40	125	°C
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## Truth Tables

**Table 4. HCPL060X/HCP-063XXXX Truth Table <sup>1</sup>**

Input	$V_{DD}$	EN	VO <sup>2</sup>
OFF	> UVLO	H	HIGH
OFF	> UVLO	L	HIGH
OFF	< UVLO	H	HIGH
OFF	< UVLO	L	HIGH
ON	> UVLO	H	LOW
ON	> UVLO	L	HIGH
ON	< UVLO	H	HIGH
ON	< UVLO	L	HIGH

Notes:

<sup>1</sup> The output voltage level is determined by the external pull-up supply.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

**Table 5. DC Specifications**

$V_{CC} = 5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40$  to  $+125\text{ °C}$ ; typical specs at  $25\text{ °C}$ ; unless otherwise noted.

Parameter	Symbol	Device	Min	Typ	Max	Unit	Test Conditions/Comments
Supply Voltage	$V_{CC}$		4.5		26.4	V	
Supply Current	$I_{CC}$	Single		0.7	2	mA	
		Dual		1.4	4		
Input Current Threshold	$I_{F(TH)}$			2.0	3	mA	
Input Forward Voltage (OFF)	$V_{F(OFF)}$			1.5	1.7	V	
Input Forward Voltage (ON)	$V_{F(ON)}$		1.8	2	2.2	V	
Logic Low Output Voltage	$V_{OL}$			0.25	0.6	V	$V_{CC} = 5.5\text{ V}$ , $I_F = 5\text{ mA}$ , $I_{OL}(\text{Sinking}) = 13\text{ mA}$
Logic High Output Current	$I_{OH}$				0.5	$\mu\text{A}$	
Peak Output Current	$I_{OPK}$			50		mA	
Enable High Min	$V_{EH}$	Single	2		$V_{CC}$	V	
Enable Low Max	$V_{EL}$	Single			0.8	V	
Enable High Current Draw	$I_{EH}$	Single		10		$\mu\text{A}$	
Enable Low Current Draw	$I_{EL}$	single		-100		$\mu\text{A}$	

**Table 6. Switching Specifications**

VDCC= 5 V; GND = 0 V; RL = 350 Ω ; CL = 30 pF; TA = -40 to +125 °C; typical specs at 25 °C; TJ = -40 to +125 °C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum Data Rate	HCPL06XX/500X F <sub>DATA</sub>			10	Mbps	Within pulse width distortion (PWD) limit
	HCPL06XX/400X F <sub>DATA</sub>			1	Mbps	Within pulse width distortion (PWD) limit
Minimum Pulse Width	MPW	50			ns	Within PWD limit
Propagation Delay (Low-to-High)	t <sub>PLH</sub>		40	60	ns	The different time between 50% input signal to 50% output signal 50% @ 5V <sub>DC</sub> supply
Propagation Delay (High-to-Low)	t <sub>PHL</sub>		40	60	ns	@ 5V <sub>DC</sub> supply
Pulse Width Distortion	PWD		8	30	ns	The max different time between t <sub>PHL</sub> and t <sub>PLH</sub> @ 5V <sub>DC</sub> supply. And The value is   t <sub>PHL</sub> - t <sub>PLH</sub>
Propagation Delay Skew	t <sub>PSK(p-p)</sub>			45	ns	@ 5V <sub>DC</sub> supply
Rise Time	t <sub>R</sub>		25	40	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V <sub>DC</sub> supply
Fall Time	t <sub>F</sub>		5	10	ns	@ 5V <sub>DC</sub> supply
Device Startup Time	t <sub>START</sub>		13	25	μs	The max amount propagation delay time differs between any two output channels in the single device @ 5V <sub>DC</sub> supply.
Propagation Delay Time of Enable from VEH to VEL	t <sub>ELH</sub>		9	30	ns	VDD = 5 V, RL = 350 Ω, CL = 30 pF
Propagation Delay Time of Enable from VEL to VEH	t <sub>EHL</sub>		13	30	ns	VDD = 5 V, RL = 350 Ω, CL = 30 pF
Common Mode Transient Immunity	CMTI	50			kV/μs	@ 5V <sub>DC</sub> supply

## INSULATION AND SAFETY RELATED SPECIFICATIONS

**Table 7. Insulation Specifications**

Parameter	Symbol	DIP-8	NB SOIC-8	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	≥ 7.1	≥ 4	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	≥ 7.4	≥ 4	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		≥ 21	≥ 21	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II	II		Material Group (DIN VDE 0110, 1/89, Table 1)

**PACKAGE CHARACTERISTICS**
**Table 8. Package Characteristics**

Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		DIP-8	NB SOIC-8		
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>	10 <sup>11</sup>	10 <sup>11</sup>	Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>	0.6	0.6	pF	@1MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>	100	45	°C/W	Thermocouple located at center of package underside

Notes:

<sup>1</sup>The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4(DIP-8 Pin 1-Pin4) are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8(DIP-8 Pin 5-Pin8) are shorted together as the other terminal.

<sup>2</sup>Testing from the input signal pin to ground.

**REGULATORY INFORMATION**

See Table 9 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

**Table 9. Regulatory**

Regulatory	DIP-8	NB SOIC-8
UL	Recognized under UL 1577	Recognized under UL 1577
	Component Recognition Program <sup>1</sup>	Component Recognition Program <sup>1</sup>
	Single Protection, 5000 V rms Isolation Voltage	Single Protection, 3750V rms Isolation Voltage
	File (pending)	File (pending)
VDE	DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 <sup>2</sup>	DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 <sup>2</sup>
	Basic insulation, V <sub>IORM</sub> = 1200 V peak, V <sub>IOSM</sub> = 6250 V peak	Basic insulation, V <sub>IORM</sub> = 1200 V peak, V <sub>IOSM</sub> = 6250 V peak
	File (pending)	File (pending)
CQC	Certified under	Certified under
	CQC11-471543-2012	CQC11-471543-2012
	GB4943.1-2011	GB4943.1-2011
	Basic insulation at 845 V rms (1200 V peak) working voltage	Basic insulation at 845 V rms (1200 V peak) working voltage
	Reinforced insulation at 422 V rms (600 V peak)	Reinforced insulation at 422 V rms (600 V peak)
	File (pending)	File (pending)

Notes:

<sup>1</sup> In accordance with UL 1577, SOP-8 is tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec; DIP-8 is tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec

<sup>2</sup> In accordance with DIN V VDE V 0884-10, SOP-8 is tested by applying an insulation test voltage ≥ 1800V peak for 1 sec (partial discharge detection limit = 5 pC); DIPP-8 is tested by ≥ 1800V peak for 1 sec.

**DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The \* marking on packages denotes DIN V VDE V 0884-10 approval.

**Table 10. VDE Insulation Characteristics**

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			DIP-8	NB SOIC-8	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150 V rms			I to IV	I to IV	

For Rated Mains Voltage $\leq 300$ V rms For Rated Mains Voltage $\leq 400$ V rms			I to III I to III	I to III I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum Working Insulation Voltage		$V_{IORM}$	1200	1200	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	1800	1800	V peak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	1560	1560	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC		1440	1440	V peak
Highest Allowable Overvoltage		$V_{IOTM}$	7071	5300	V peak
Surge Isolation Voltage	Basic insulation, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) <sup>1</sup>	$V_{IOSM}$	5000	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure				
Maximum Junction Temperature		$T_S$	150	150	$^{\circ}$ C
Total Power Dissipation at 25 $^{\circ}$ C		$P_S$	0.14	0.14	W
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	$>10^9$	$>10^9$	$\Omega$

Notes:

<sup>1</sup>In accordance with DIN V VDE V 0884-11, [HCPL060X/HCP-063XXXX](#) is proof tested by applying a surge isolation voltage 6500 V.

## TYPICAL CHARACTERISTIC

VCC=5V, 0.1 $\mu$ F capacitor from VCC to GND, TA = -40 $^{\circ}$ C to 125 $^{\circ}$ C (Unless otherwise noted).

Figure 2: Typical High Level Output Current vs. Temperature

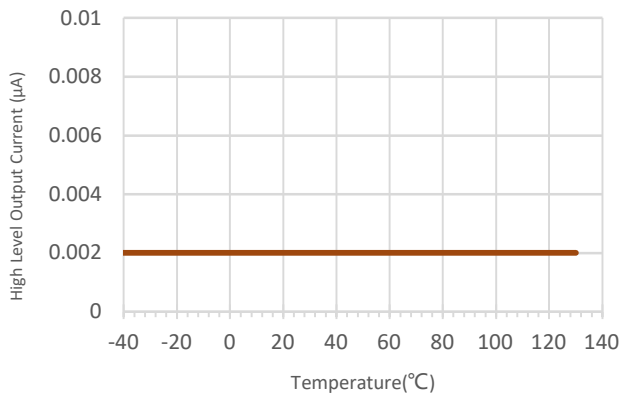


Figure 3: Typical Input Threshold Current vs. Temperature

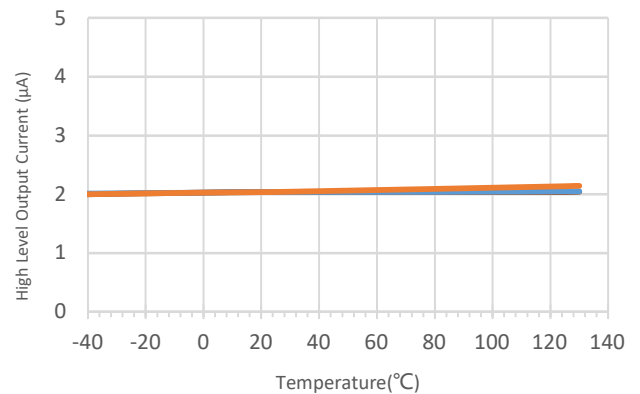


Figure 4: Typical Low Level Output Voltage vs. Temperature

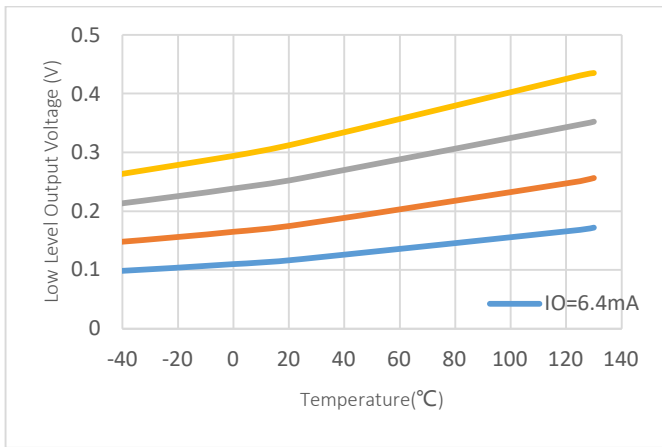


Figure 5: Typical Low Level Output Current vs. Temperature

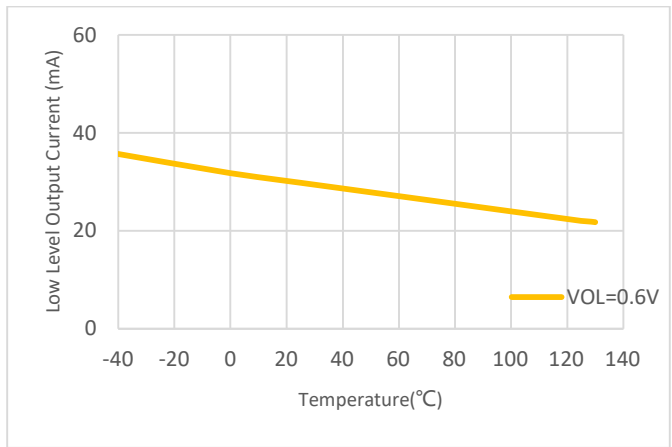


Figure 6: Typical Propagation Delay TPHL vs. Temperature

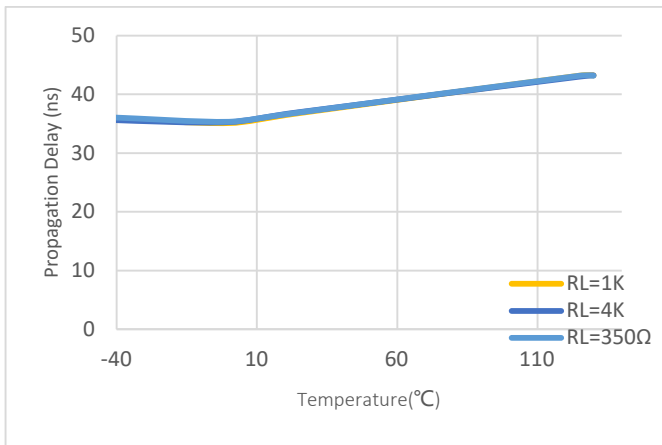


Figure 7: Typical Propagation Delay TPLH vs. Temperature

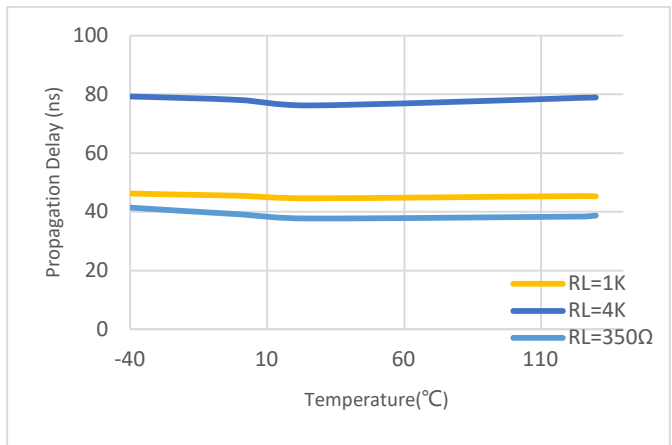


Figure 8: Typical Rise Time vs. Temperature

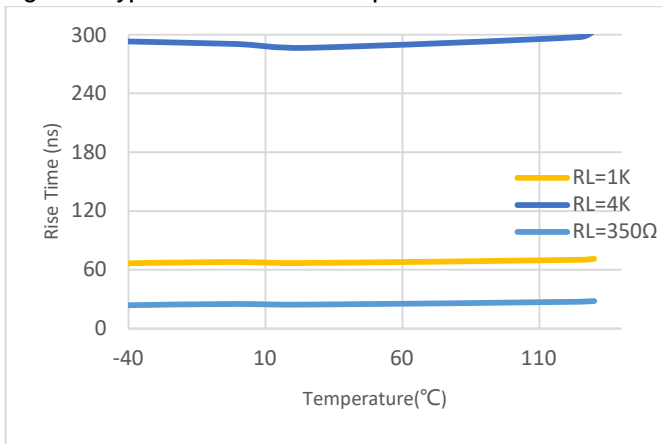


Figure 9: Typical Fall Time vs. Temperature

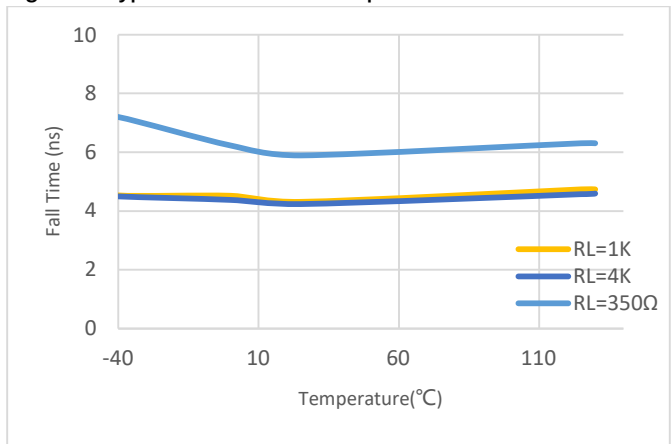


Figure 10: Enable Propagation Delay TEHL vs. Temperature

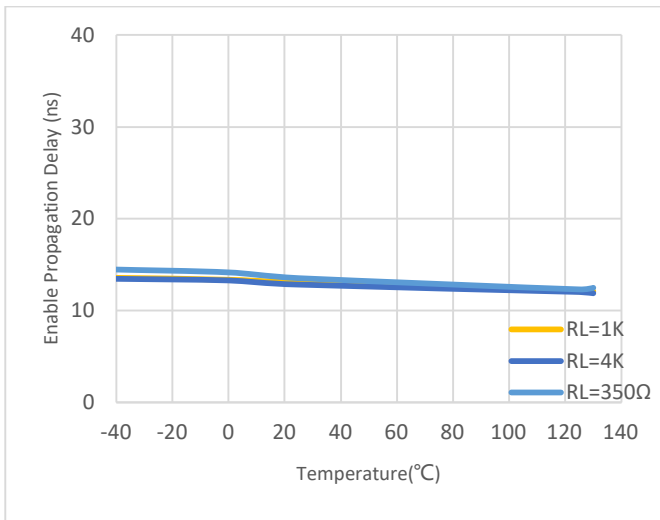


Figure 11: Enable Propagation Delay TELH vs. Temperature

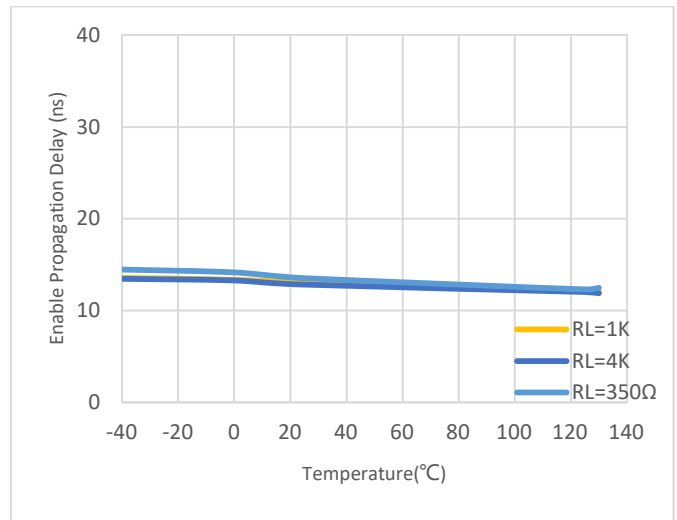
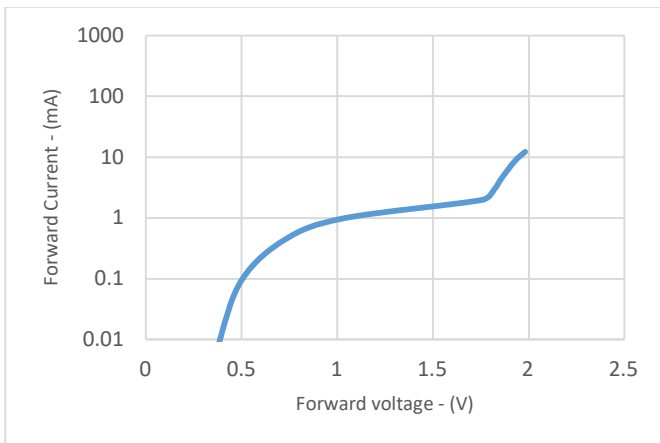
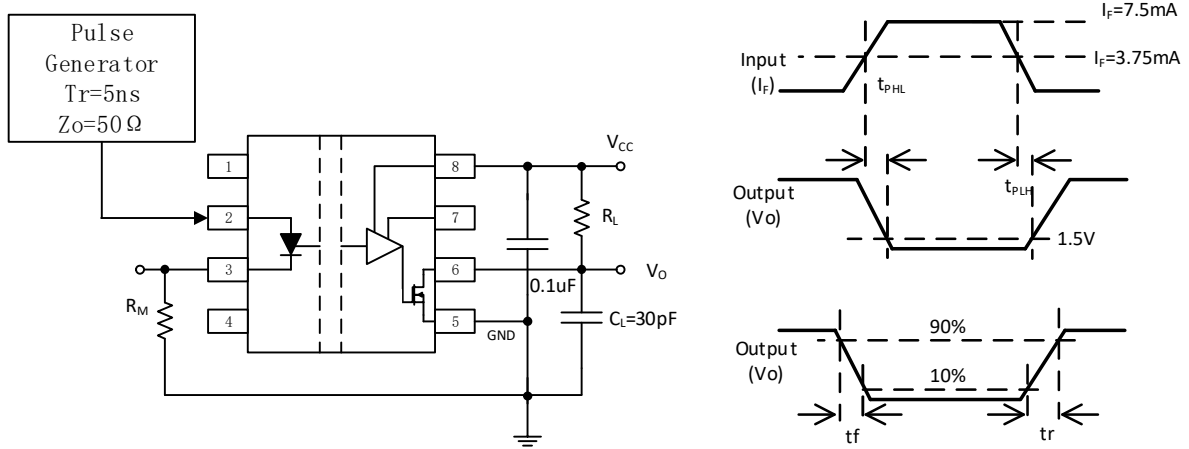


Figure 12: Typical Input Diode Forward Characteristic

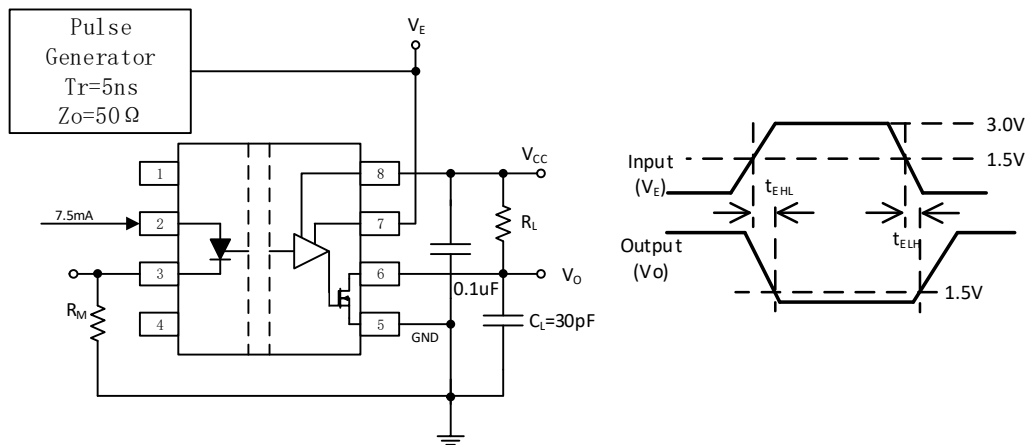




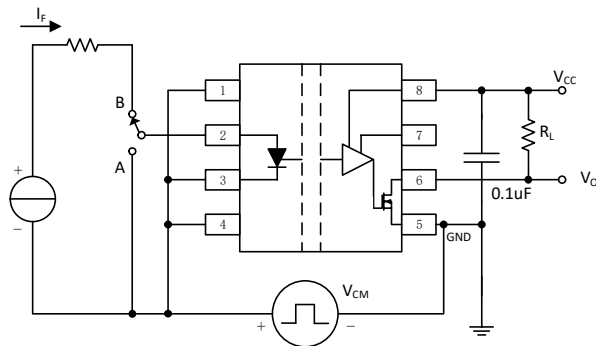
**Fig. 13 Test circuit and waveforms for  $t_{PHL}$ ,  $t_{PLH}$ ,  $t_r$ , and  $t_f$**



**Fig. 14 Test circuit and waveform for  $t_{EHL}$  and  $t_{ELH}$**



**Fig. 15 Test circuit Common mode Transient Immunity**



## OUTLINE DIMENSIONS

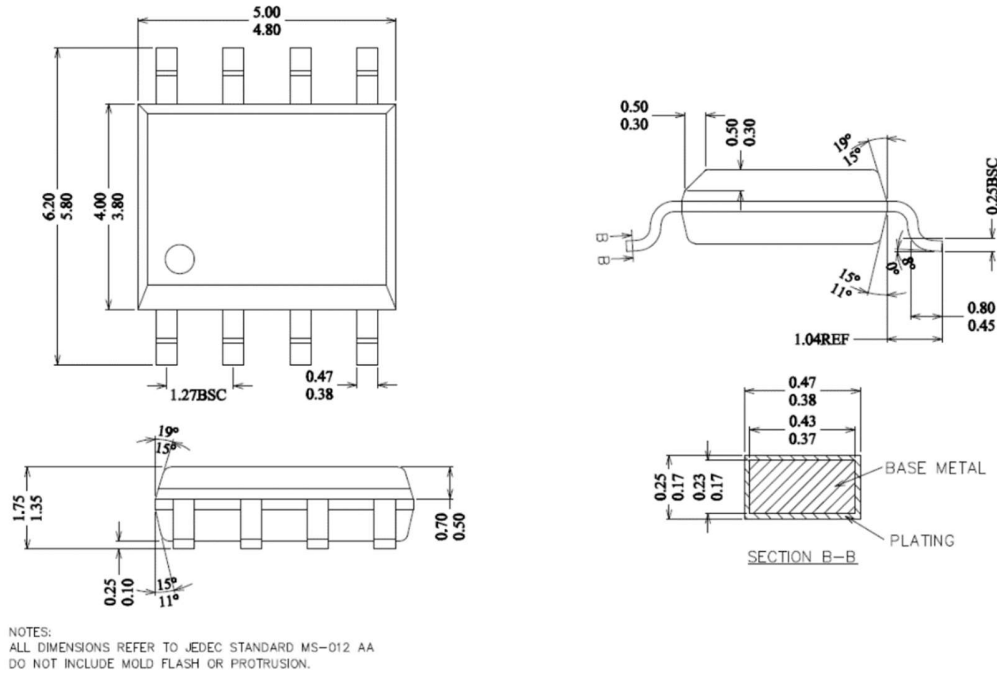
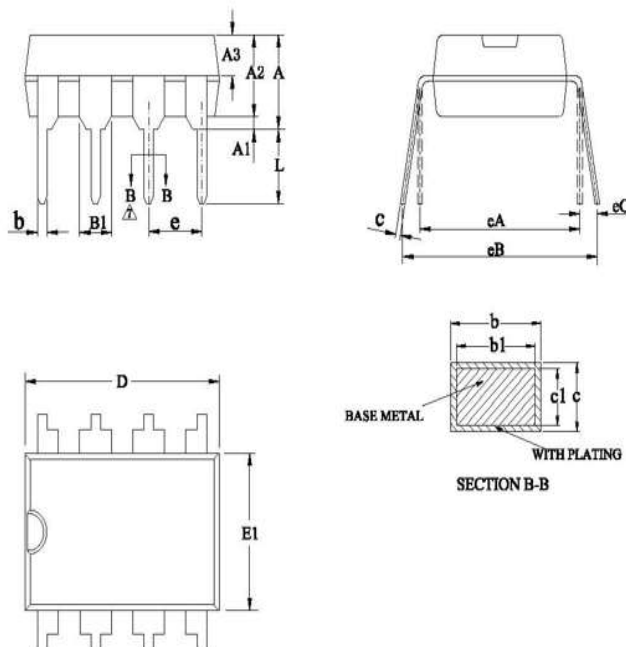


Figure15. 8-Lead Standard Small Outline Package [NB SOIC-8]

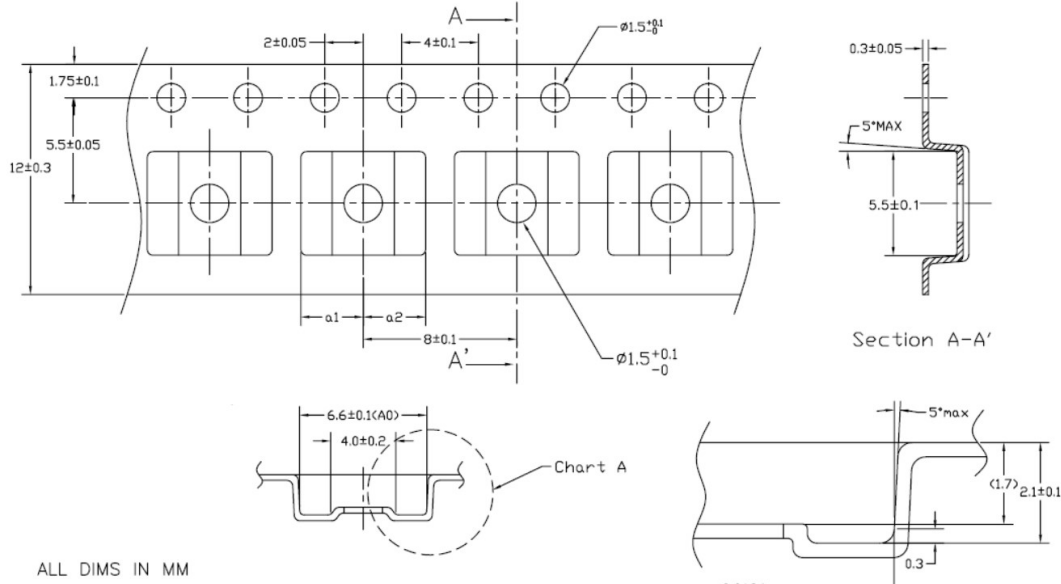


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.55	1.60	1.65
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52REF		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	9.15	9.25	9.35
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—

Figure16. 8-Lead DIP Outline Package [DIP-8]

## REEL INFORMATION

8-Lead SOIC\_N



## SELECTION GUIDE

Table 11. Ordering Guide

Model Name <sup>1</sup>	Temperature Range	Package	MSL Peak Temp <sup>2</sup>	MOQ/Quantity per reel <sup>3</sup>
HCPL0602R2	-40~125°C	NB SOIC-8	Level-2-260C-1 YEAR	2500
HCPL0601R2	-40~125°C	NB SOIC-8	Level-2-260C-1 YEAR	2500
HCPL-0630-400E	-40~125°C	NB SOIC-8	Level-2-260C-1 YEAR	2500
HCPL-0630-500E	-40~125°C	NB SOIC-8	Level-2-260C-1 YEAR	2500
HCPL0602R3	-40~125°C	DIP-8		2500
HCPL0601R3	-40~125°C	DIP-8		2500
HCPL-0630-400C	-40~125°C	DIP-8		2500
HCPL-0630-500C	-40~125°C	DIP-8		2500

<sup>1</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>2</sup> MOQ, minimum ordering quantity.

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[TLP5772H\(D4LF4,E](#) [TLP5774H\(LF4,E](#) [TLP5771H\(D4LF4,E](#) [TLP5771H\(LF4,E](#) [TLP5214A\(E\(O](#) [FOD3125SD](#) [FOD8482T](#) [LTV-3120S-](#)  
[TA1-H](#) [LTV-332J-TP1](#) [PC923LRNIP0F](#) [HCPL-0630-500E\(TOKMAS\)](#) [TLP719F\(D4-TP,F\)](#) [TLP5702\(D4-TP,E\(T](#) [TLP105\(TPL,F\)](#)  
[TLP2301\(GB-TPL,E\(T](#) [TLP715\(D4-TP,F\)](#) [TLP2348\(TPL,E\(T](#) [6N137S](#) [KPC410 0E](#) [ELM600\(TA\)](#) [6N138M](#) [6N137M](#) [ELS3120P\(TA\)-VG](#)  
[6N137-500E-JSM](#) [H11L1S-TA1-L](#) [CY4N33S\(TP1\)](#) [CY4N33](#) [PC923LRNSZ0F](#) [SL0601](#) [6N136S](#) [6N137\(SL\)\(T1\)](#) [ELS680P\(TA\)-VG](#)  
[H11L1S\(TA\)](#) [H11L3SR2M](#) [HCPL-0302-000E](#) [HCPL-6730](#) [HCPL-J312-000E](#) [LTV-3120S-TA1](#) [TLP155E\(TPL,E\)](#) [TLP2345\(E\(T](#)  
[TLP2348\(E\(T](#) [TLP350H\(F\)](#)