

## Enhanced ESD, 3.0 KV rms/5.0 KV rms 200Mbps Dual-channel Digital Isolators

### FEATURES

Ultra-low power consumption (1Mbps): 0.58mA/Channel

High data rate: 200Mbps

High common-mode transient immunity:

ISO772x: 75kV/ $\mu$ s typical

ISO773x: 120kV/ $\mu$ s typical

High robustness to radiated and conducted noise

Low propagation delay: 9ns typical

Isolation voltages:

ISO772x: AC 3000Vrms

ISO773x: AC 5000Vrms

High ESD rating:

ESDA/JEDEC JS-001-2017

Human body model (HBM)  $\pm$ 8kV

Safety and regulatory approvals:

3000Vrms/5000Vrms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

DIN VDE V 0884-11:2017-01

$V_{IORM} = 565V$  peak/1200V peak

CQC certification per GB4943.1-2011

3 V to 5.5 V level translation

AEC-Q100 qualification

Wide temperature range:  $-40^{\circ}C$  to  $125^{\circ}C$

RoHS-compliant, NB SOIC-8, WB SOIC-16 package

### APPLICATIONS

General-purpose multichannel isolation

Industrial field bus isolation

Isolation Industrial automation systems

Isolated switch mode supplies

Isolated ADC, DAC

Motor control

### FUNCTIONAL BLOCK DIAGRAMS

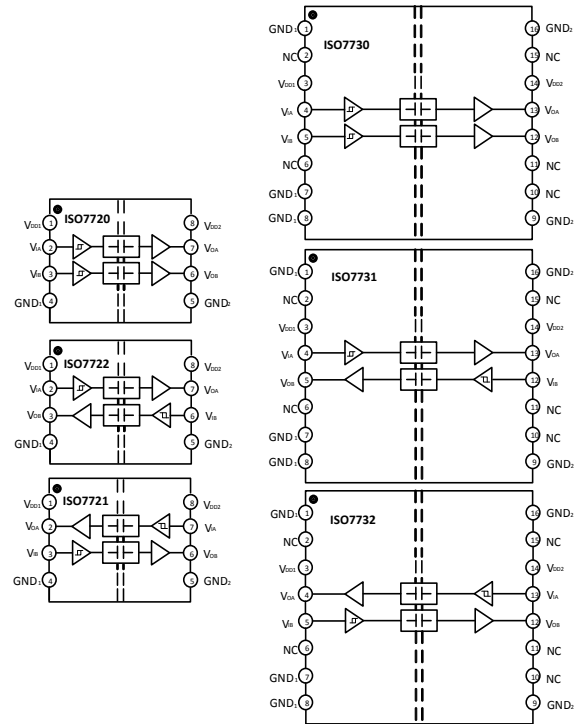


Figure 1. ISO772x/773x functional Block Diagram

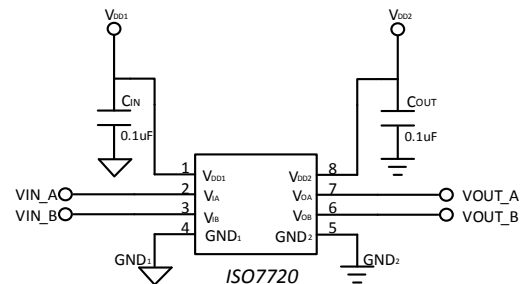


Figure 2. ISO7720 Typical Application Circuit

## PIN CONFIGURATIONS AND FUNCTIONS

Table 1. ISO7720 Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>OA</sub>	Logic Output A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

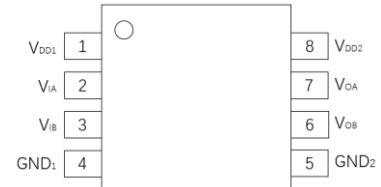


Figure 3. ISO7720 Pin Configuration

Table 2. ISO7722 Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>OB</sub>	Logic Output B.
4	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V <sub>IB</sub>	Logic Input B.
7	V <sub>OA</sub>	Logic Output A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

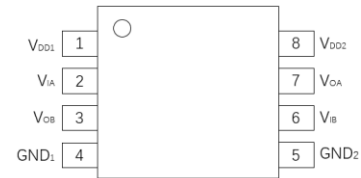


Figure 4. ISO7722 Pin Configuration

Table 3. ISO7721 Pin Function Descriptions

Pin No.	Name	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>OA</sub>	Logic Output A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>IA</sub>	Logic Input A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

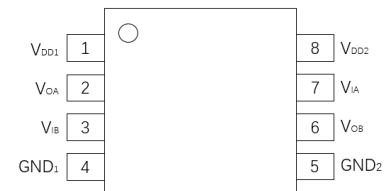


Figure 5. ISO7721 Pin Configuration

Table 4. ISO7730 Pin Function Descriptions

Pin No.	Name	Description
1	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No connect.
3	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
4	V <sub>IA</sub>	Logic Input A.
5	V <sub>IB</sub>	Logic Input B.
6	NC	No Connect.
7	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V <sub>OB</sub>	Logic Output B.
13	V <sub>OA</sub>	Logic Output A.
14	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.

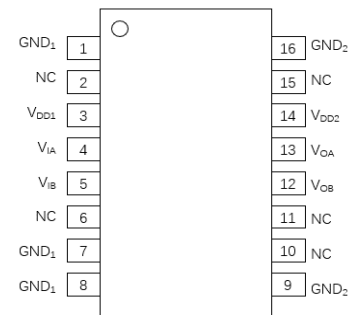


Figure 6. ISO7730 Pin Configuration

Table 5.ISO7731 Pin Function Descriptions

Pin No.	Name	Description
1	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
4	V <sub>IA</sub>	Logic Input A.
5	V <sub>OB</sub>	Logic Output B.
6	NC	No Connect.
7	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V <sub>IB</sub>	Logic Input B.
13	V <sub>OA</sub>	Logic Output A.
14	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.

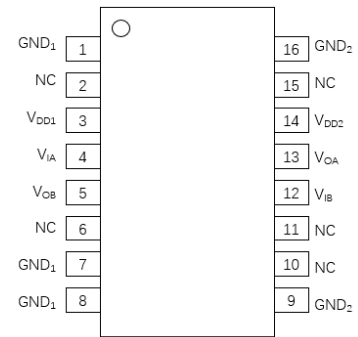


Figure 7. ISO7731 Pin Configuration

Table 6.ISO7732 Pin Function Descriptions

Pin No.	Name	Description
1	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
4	V <sub>OA</sub>	Logic Output A.
5	V <sub>IB</sub>	Logic Input B.
6	NC	No Connect.
7	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND <sub>1</sub>	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V <sub>OB</sub>	Logic Output B.
13	V <sub>IA</sub>	Logic Input A.
14	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND <sub>2</sub>	Ground 2. This pin is the ground reference for Isolator Side 2.

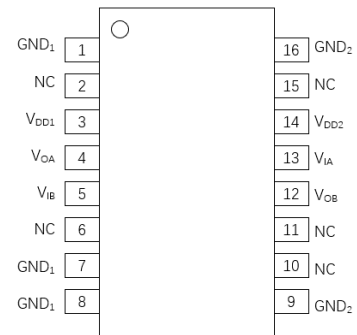


Figure 8. ISO7732 Pin Configuration

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

 Table 7.Absolute Maximum Ratings<sup>4</sup>

Parameter	Rating
Supply Voltages (V <sub>DD1</sub> -GND <sub>1</sub> , V <sub>DD2</sub> -GND <sub>2</sub> )	-0.5 V ~ +7.0 V
Input Voltages (V <sub>IA</sub> , V <sub>IB</sub> ) <sup>1</sup>	-0.5 V ~ V <sub>DDx</sub> + 0.5 V
Output Voltages (V <sub>OA</sub> , V <sub>OB</sub> ) <sup>1</sup>	-0.5 V ~ V <sub>DDx</sub> + 0.5 V
Average Output Current per Pin <sup>2</sup> Side 1 Output Current (I <sub>O1</sub> )	-10 mA ~ +10 mA
Average Output Current per Pin <sup>2</sup> Side 2 Output Current (I <sub>O2</sub> )	-10 mA ~ +10 mA
Common-Mode Transients Immunity <sup>3</sup>	-200 kV/μs ~ +200 kV/μs
Storage Temperature (T <sub>ST</sub> ) Range	-65°C ~ +150°C
Ambient Operating Temperature (T <sub>A</sub> ) Range	-40°C ~ +125°C

Notes:

<sup>1</sup> V<sub>DDx</sub> is the side voltage power supply V<sub>DD</sub>, where x = 1 or 2.

<sup>2</sup> See Figure 9 for the maximum rated current values for various temperatures.

<sup>3</sup> See Figure 17 for Common-mode transient immunity (CMTI) measurement.

<sup>4</sup> Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## RECOMMENDED OPERATING CONDITIONS

Table 8. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DDx}^1$	3		5.5	V
High Level Input Signal Voltage	$V_{IH}$	$0.7 \cdot V_{DDx}^1$		$V_{DDx}^1$	V
Low Level Input Signal Voltage	$V_{IL}$	0		$0.3 \cdot V_{DDx}^1$	V
High Level Output Current	$I_{OH}$	-6			mA
Low Level Output Current	$I_{OL}$			6	mA
Data Rate		0		200	Mbps
Junction Temperature	$T_J$	-40		150	°C
Ambient Operating Temperature	$T_A$	-40		125	°C

Notes:

<sup>1</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where  $x = 1$  or  $2$ .

## Truth Tables

Table 9. ISO772X/773X Truth Table

$V_{ix}$ Input <sup>1</sup>	$V_{DDI}$ State <sup>1</sup>	$V_{DDO}$ State <sup>1</sup>	Default Low $V_{ox}$ Output <sup>1</sup>	Default High $V_{ox}$ Output <sup>1</sup>	Test Conditions /Comments
Low	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	Low	Normal operation
High	Powered <sup>2</sup>	Powered <sup>2</sup>	High	High	Normal operation
Open	Powered <sup>2</sup>	Powered <sup>2</sup>	Low	High	Default output
Don't Care <sup>4</sup>	Unpowered <sup>3</sup>	Powered <sup>2</sup>	Low	High	Default output <sup>5</sup>
Don't Care <sup>4</sup>	Powered <sup>2</sup>	Unpowered <sup>3</sup>	High Impedance	High Impedance	

Notes:

<sup>1</sup>  $V_{ix}/V_{ox}$  are the input/output signals of a given channel (A or B).  $V_{DDI}/V_{DDO}$  are the supply voltages on the input/output signal sides of this given channel.

<sup>2</sup> Powered means  $V_{DDx} \geq 2.95$  V

<sup>3</sup> Unpowered means  $V_{DDx} < 2.30$  V

<sup>4</sup> Input signal ( $V_{ix}$ ) must be in a low state to avoid powering the given  $V_{DDI}^1$  through its ESD protection circuitry.

<sup>5</sup> If the  $V_{DDI}$  goes into unpowered status, the channel outputs the default logic signal after around 1 $\mu$ s. If the  $V_{DDI}$  goes into powered status, the channel outputs the input status logic signal after around 3 $\mu$ s.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

Table 10. ISO772X/773X Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			5	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		200			Mbps	Within PWD limit
Propagation Delay Time <sup>1</sup>	$t_{pHL}, t_{pLH}$	5.5	8	12.5	ns	@ 5V <sub>DC</sub> supply
		6.5	9	13.5	ns	@ 3.3V <sub>DC</sub> supply
Pulse Width Distortion	PWD		0.3	3.0	ns	The max different time between $t_{pHL}$ and $t_{pLH}$ @ 5V <sub>DC</sub> supply. And The value is   $t_{pHL} - t_{pLH}$
			0.4	3.0	ns	The max different time between $t_{pHL}$ and $t_{pLH}$ @ 3.3V <sub>DC</sub> supply. And The value is   $t_{pHL} - t_{pLH}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Part to Part Propagation Delay Skew	$t_{PSK}$			2	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V <sub>DC</sub> supply
				2	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V <sub>DC</sub> supply
Channel to Channel Propagation Delay Skew	$t_{CSK}$		0	1.8	ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V <sub>DC</sub> supply.
			0	2	ns	The max amount propagation delay time differs between any two output channels in the single device @ 3.3V <sub>DC</sub> supply
Output Signal Rise/Fall Time <sup>4</sup>	$t_r/t_f$		1.5		ns	See Figure 13.
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		9		$\mu A$ /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V <sub>DC</sub> Supply
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		38		$\mu A$ /Mbps	
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		5		$\mu A$ /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V <sub>DC</sub> Supply
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		23		$\mu A$ /Mbps	
Common-Mode Transient Immunity <sup>3</sup>	CMTI		75		kV/ $\mu s$	$V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V.
Jitter			120		ps p-p	See the Jitter Measurement section
			20		ps rms	
ESD(HBM - Human body model)	ESD		$\pm 8$		kV	

Notes:

<sup>1</sup>  $t_{PLH}$  = low-to-high propagation delay time,  $t_{PHL}$  = high-to-low propagation delay time. See Figure 14.

<sup>2</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.

<sup>3</sup> See Figure 17 for Common-mode transient immunity (CMTI) measurement.

<sup>4</sup>  $t_r$  means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal,  $t_f$  means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 11. ISO773X Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			5	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		200			Mbps	Within PWD limit
Propagation Delay Time <sup>1</sup>	$t_{PHL}, t_{PLH}$		12	16	ns	@ 5V <sub>DC</sub> supply
			14	18.5	ns	@ 3.3V <sub>DC</sub> supply
Pulse Width Distortion	PWD		0.3	3.0	ns	The max different time between $t_{PHL}$ and $t_{PLH}$ @ 5V <sub>DC</sub> supply. And The value is $ t_{PHL} - t_{PLH} $
			0.4	3.0	ns	The max different time between $t_{PHL}$ and $t_{PLH}$ @ 3.3V <sub>DC</sub> supply. And The value is $ t_{PHL} - t_{PLH} $
Part to Part Propagation Delay Skew	$t_{PSK}$			2	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V <sub>DC</sub> supply
				2	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V <sub>DC</sub> supply

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Channel to Channel Propagation Delay Skew	$t_{CSK}$	0	1.8		ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V <sub>DC</sub> supply.
		0	2		ns	The max amount propagation delay time differs between any two output channels in the single device @ 3.3V <sub>DC</sub> supply
Output Signal Rise/Fall Time <sup>4</sup>	$t_r/t_f$		1.5		ns	See Figure 13.
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		10		$\mu A$ /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V <sub>DC</sub> Supply
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		45		$\mu A$ /Mbps	
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		9		$\mu A$ /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V <sub>DC</sub> Supply
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		28		$\mu A$ /Mbps	
Common-Mode Transient Immunity <sup>3</sup>	CMTI		120		kV/ $\mu s$	$V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V.
Jitter			180		ps p-p	See the Jitter Measurement section
			30		ps rms	
ESD(HBM - Human body model)	ESD		$\pm 8$		kV	

Notes:

<sup>1</sup> $t_{pLH}$  = low-to-high propagation delay time,  $t_{pHL}$  = high-to-low propagation delay time. See Figure 14.

<sup>2</sup> $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.

<sup>3</sup>See Figure 17 for Common-mode transient immunity (CMTI) measurement.

<sup>4</sup> $t_r$  means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal ,  $t_f$  means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 12.DC Specifications

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	$V_{IT+}$		$0.6 * V_{DDx}^1$	$0.7 * V_{DDx}^1$	V	
Falling Input Signal Voltage Threshold	$V_{IT-}$	$0.3 * V_{DDx}^1$	$0.4 * V_{DDx}^1$		V	
High Level Output Voltage	$V_{OH}^1$	$V_{DDx} - 0.1$	$V_{DDx}$		V	-20 $\mu A$ output current
		$V_{DDx} - 0.2$	$V_{DDx} - 0.1$		V	-2 mA output current
Low Level Output Voltage	$V_{OL}$		0	0.1	V	20 $\mu A$ output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	$I_{IN}$	-10	0.5	10	$\mu A$	$0 V \leq \text{Signal voltage} \leq V_{DDx}^1$
$V_{DDx}^1$ Undervoltage Rising Threshold	$V_{DDxUV+}$	2.45	2.75	2.95	V	
$V_{DDx}^1$ Undervoltage Falling Threshold	$V_{DDxUV-}$	2.30	2.60	2.75	V	
$V_{DDx}^1$ Hysteresis	$V_{DDxUVH}$		0.15		V	

Notes:

<sup>1</sup> $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.

Table 13.Quiescent Supply Current

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $C_L = 0$  pF, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
ISO7720	$I_{DD1(Q)}$	0.06	0.08	0.10	mA	5V <sub>DC</sub>	$V_I = 0V$ for ISO772X
	$I_{DD2(Q)}$	0.78	0.98	1.27	mA		$V_I = 5V$ for ISO772X
	$I_{DD1(Q)}$	0.16	0.20	0.26	mA		$V_I = 5V$ for ISO772X

Part	Symbol	Min	Typ	Max	Unit	Test Conditions			
						Supply voltage	Input signal		
	I <sub>DD2</sub> (Q)	0.74	0.92	1.20	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.06	0.08	0.10	mA		VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.77	0.97	1.26	mA		VI=3.3V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.12	0.15	0.19	mA		VI=3.3V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.71	0.89	1.15	mA		VI=0V for ISO77xx1		
ISO7722	I <sub>DD1</sub> (Q)	0.42	0.52	0.68	mA	5V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.42	0.52	0.68	mA		VI=5V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.44	0.55	0.71	mA		VI=5V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.44	0.55	0.71	mA		VI=0V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.52	0.67	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.52	0.67	mA		VI=3.3V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.51	0.66	mA		VI=3.3V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.51	0.66	mA		VI=0V for ISO77xx1		
	ISO7721	I <sub>DD1</sub> (Q)	0.42	0.52	0.68		mA	5V <sub>DC</sub>	VI=0V for ISO77xx0
		I <sub>DD2</sub> (Q)	0.42	0.52	0.68		mA		VI=5V for ISO77xx1
I <sub>DD1</sub> (Q)		0.44	0.55	0.71	mA	VI=5V for ISO77xx0			
I <sub>DD2</sub> (Q)		0.44	0.55	0.71	mA	VI=0V for ISO77xx1			
I <sub>DD1</sub> (Q)		0.41	0.52	0.67	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx0		
I <sub>DD2</sub> (Q)		0.41	0.52	0.67	mA		VI=3.3V for ISO77xx1		
I <sub>DD1</sub> (Q)		0.41	0.51	0.66	mA		VI=3.3V for ISO77xx0		
I <sub>DD2</sub> (Q)		0.41	0.51	0.66	mA		VI=0V for ISO77xx1		
ISO7730		I <sub>DD1</sub> (Q)	0.06	0.10	0.13		mA	5V <sub>DC</sub>	VI=0V for ISO77xx0
		I <sub>DD2</sub> (Q)	0.78	1.12	1.46		mA		VI=5V for ISO77xx1
	I <sub>DD1</sub> (Q)	0.16	0.32	0.41	mA	VI=5V for ISO77xx0			
	I <sub>DD2</sub> (Q)	0.74	1.03	1.35	mA	VI=0V for ISO77xx1			
	I <sub>DD1</sub> (Q)	0.06	0.10	0.12	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.77	1.09	1.42	mA		VI=3.3V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.12	0.21	0.27	mA		VI=3.3V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.71	1.01	1.30	mA		VI=0V for ISO77xx1		
ISO7731	I <sub>DD1</sub> (Q)	0.42	0.60	0.78	mA	5V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.42	0.60	0.78	mA		VI=5V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.44	0.66	0.85	mA		VI=5V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.44	0.66	0.85	mA		VI=0V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.58	0.74	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.58	0.74	mA		VI=3.3V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.59	0.77	mA		VI=3.3V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.59	0.77	mA		VI=0V for ISO77xx1		
ISO7732	I <sub>DD1</sub> (Q)	0.42	0.60	0.78	mA	5V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.42	0.60	0.78	mA		VI=5V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.44	0.66	0.85	mA		VI=5V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.44	0.66	0.85	mA		VI=0V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.58	0.74	mA	3.3V <sub>DC</sub>	VI=0V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.58	0.74	mA		VI=3.3V for ISO77xx1		
	I <sub>DD1</sub> (Q)	0.41	0.59	0.77	mA		VI=3.3V for ISO77xx0		
	I <sub>DD2</sub> (Q)	0.41	0.59	0.77	mA		VI=0V for ISO77xx1		

Table 14.Total Supply Current vs. Data Throughput (CL = 0 pF)

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\% \text{ or } 5V_{DC} \pm 10\%, T_A = 25^\circ C, C_L = 0 \text{ pF, unless otherwise noted.}$

Part	Symbol	2 Mbps			20 Mbps			200 Mbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
ISO7720	I <sub>DD1</sub>		0.23	0.36		0.48	0.77		3.72	5.95	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		1.12	1.80		2.64	4.22		17.20	27.52		
	I <sub>DD1</sub>		0.16	0.25		0.36	0.58		2.16	3.46	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		1.07	1.71		2.15	3.43		11.14	17.82		
ISO7722	I <sub>DD1</sub>		0.64	1.02		1.94	3.10		10.40	16.64	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		0.64	1.02		1.94	3.10		10.40	16.64		
	I <sub>DD1</sub>		0.59	0.95		1.54	2.46		6.58	10.53	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		0.59	0.95		1.54	2.46		6.58	10.53		
ISO7721	I <sub>DD1</sub>		0.64	1.02		1.94	3.10		10.40	16.64	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		0.64	1.02		1.94	3.10		10.40	16.64		
	I <sub>DD1</sub>		0.59	0.95		1.54	2.40		6.58	10.53	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		0.59	0.95		1.54	2.40		6.58	10.53		
ISO7730	I <sub>DD1</sub>		0.33	0.53		1.06	1.70		8.78	14.05	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		1.28	2.04		2.93	4.68		19.54	31.26		
	I <sub>DD1</sub>		0.22	0.35		0.68	1.09		5.16	8.26	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		1.21	1.94		2.39	3.82		13.28	21.25		
ISO7731	I <sub>DD1</sub>		0.77	1.23		2.54	4.06		14.92	23.87	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		0.77	1.23		2.54	4.06		14.92	23.87		
	I <sub>DD1</sub>		0.69	1.11		1.98	3.17		9.88	15.81	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		0.69	1.11		1.98	3.17		9.88	15.81		
ISO7733	I <sub>DD1</sub>		0.77	1.23		2.54	4.06		14.92	23.87	mA	5V <sub>DC</sub>
	I <sub>DD2</sub>		0.77	1.23		2.54	4.06		14.92	23.87		
	I <sub>DD1</sub>		0.69	1.11		1.98	3.17		9.88	15.81	mA	3.3V <sub>DC</sub>
	I <sub>DD2</sub>		0.69	1.11		1.98	3.17		9.88	15.81		

## INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 15. Insulation Specifications

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		ISO772x	ISO773x		
Rated Dielectric Insulation Voltage		3000	5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		≥11	≥21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	
Material Group		II	II		

## PACKAGE CHARACTERISTICS

Table 16. Package Characteristics



Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		ISO772x	ISO773x		
Resistance (Input to Output) <sup>1</sup>	R <sub>io</sub>	10 <sup>11</sup>	10 <sup>11</sup>	Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>io</sub>	1.5	1.5	pF	@1MHz
Input Capacitance <sup>2</sup>	C <sub>i</sub>	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>	100	45	°C/W	Thermocouple located at center of package underside

Notes:

<sup>1</sup>The device is considered a 2-terminal device; Short-circuit all terminals on the VDD1 side as one terminal, and short-circuit all terminals on the VDD2 side as the other terminal.

<sup>2</sup>Testing from the input signal pin to ground.

### DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

Table 18.VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			ISO772x	ISO773x	
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to III	I to IV I to III I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive peak isolation voltage		V <sub>IORM</sub>	565	1200	V peak
Input to Output Test Voltage, Method B1	V <sub>IORM</sub> × 1.5 = V <sub>pd(m)</sub> , 100% production test, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, partial discharge < 5 pC	V <sub>pd(m)</sub>	848	1800	V peak

Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup	$V_{IORM} \times 1.3 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	735	1560	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1440	V peak
Highest Allowable Overvoltage		$V_{IOTM}$	4200	7071	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2/50 $\mu$ s combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	$V_{IOSM}$	3615	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 9)				
Maximum safety Temperature		$T_S$	150	150	$^{\circ}C$
Maximum Power Dissipation at 25 $^{\circ}C$		$P_S$	1.25	2.78	W
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	> $10^9$	> $10^9$	$\Omega$

### Typical Thermal Characteristic

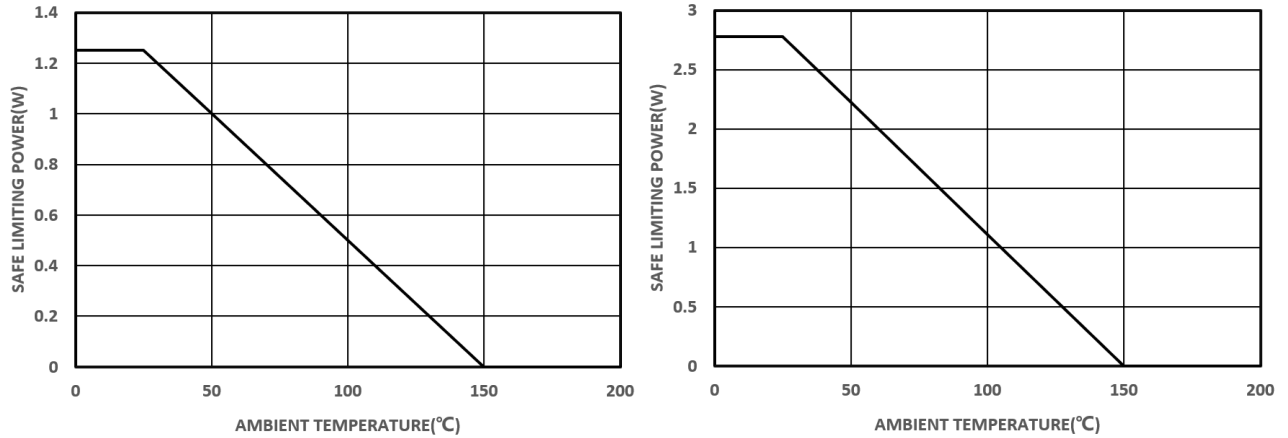


Figure 9. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE (left:ISO772x ; right: ISO773x )

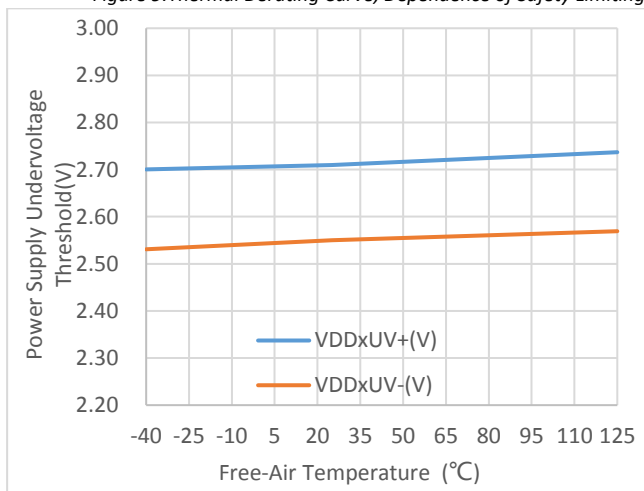


Figure 10. UVLO vs. Free-Air Temperature

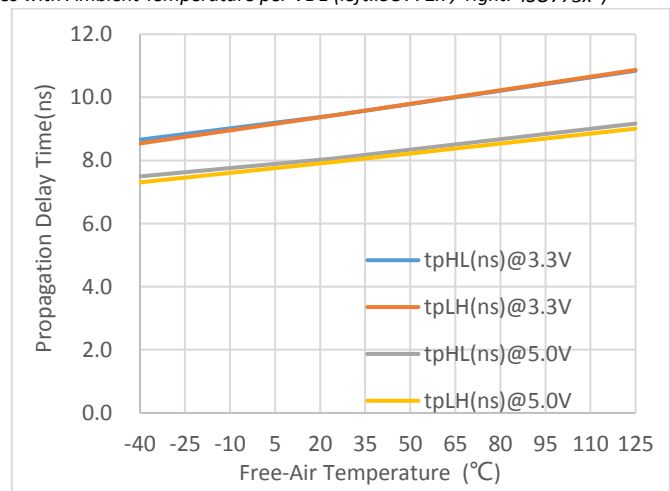


Figure 11. ISO772x Propagation Delay Time vs. Free-Air Temperature

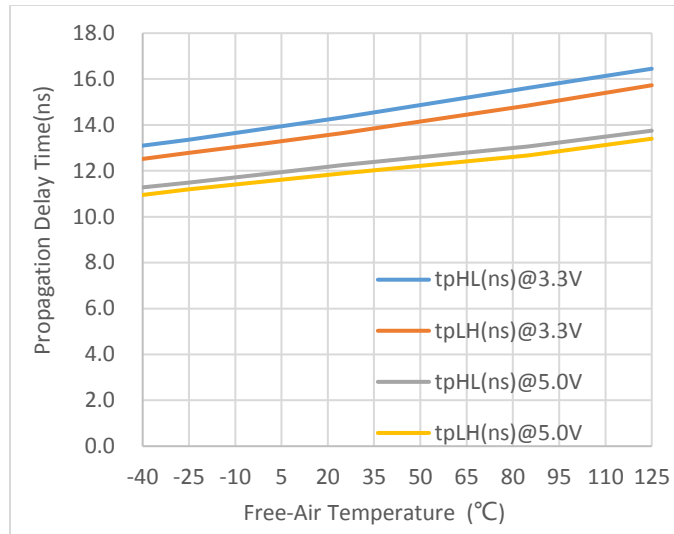


Figure 12. ISO773x Propagation Delay Time vs. Free-Air Temperature

**Timing test information**

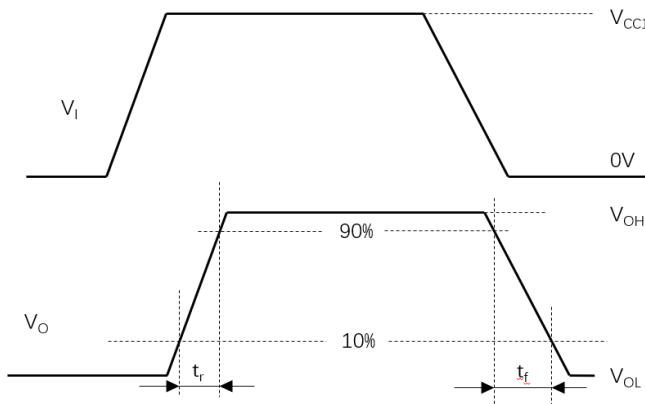


Figure 13. Transition time waveform measurement

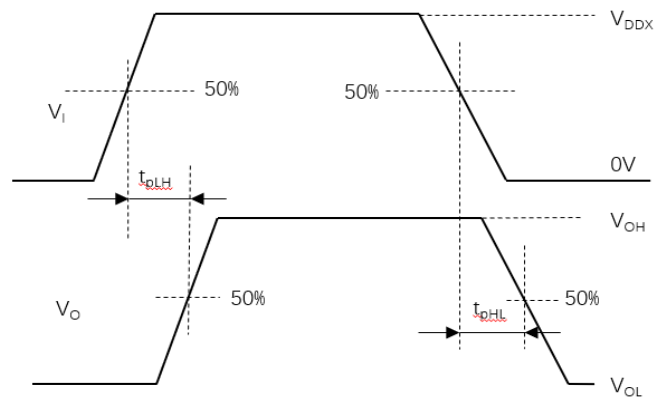


Figure 14. Propagation delay time waveform measurement

## PCB LAYOUT

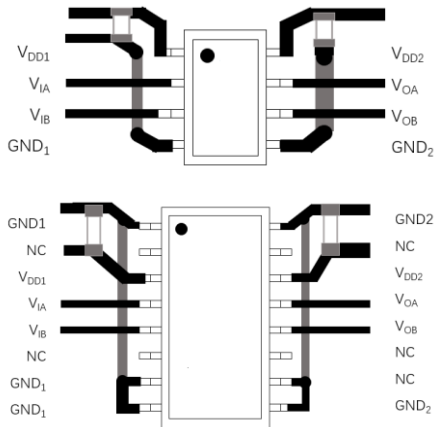


Figure 15. Recommended Printed Circuit Board Layout

The low-ESR ceramic bypass capacitors must be connected between  $V_{DD1}$  and  $GND_1$  and between  $V_{DD2}$  and  $GND_2$ . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between  $0.1 \mu\text{F}$  and  $10 \mu\text{F}$ . The user may also include resistors ( $50\text{--}300 \Omega$ ) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and its return path.

## JITTER MEASUREMENT

The eye diagram shown in the figure below provides the jitter measurement result for the ISO772x/ISO773x. The Keysight 81160A pulse function arbitrary generator works as the data source for the ISO772x/ISO773x, which generates 100Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the ISO772x/ISO773x output waveform and recovers the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement jitter data.

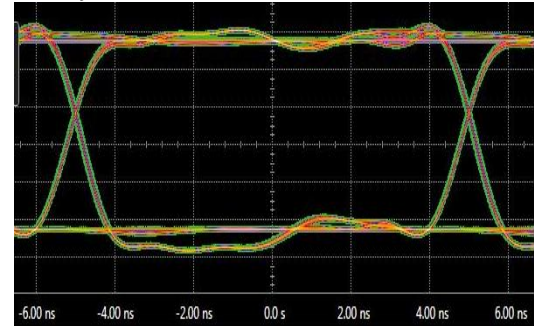


Figure 16. ISO772x/773x Eye Diagram

## CMTI MEASUREMENT

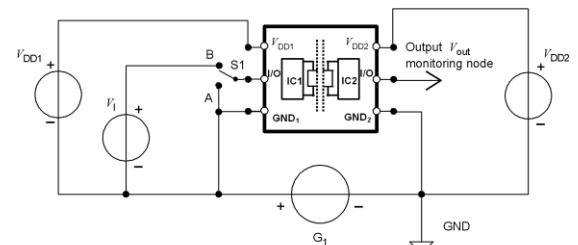
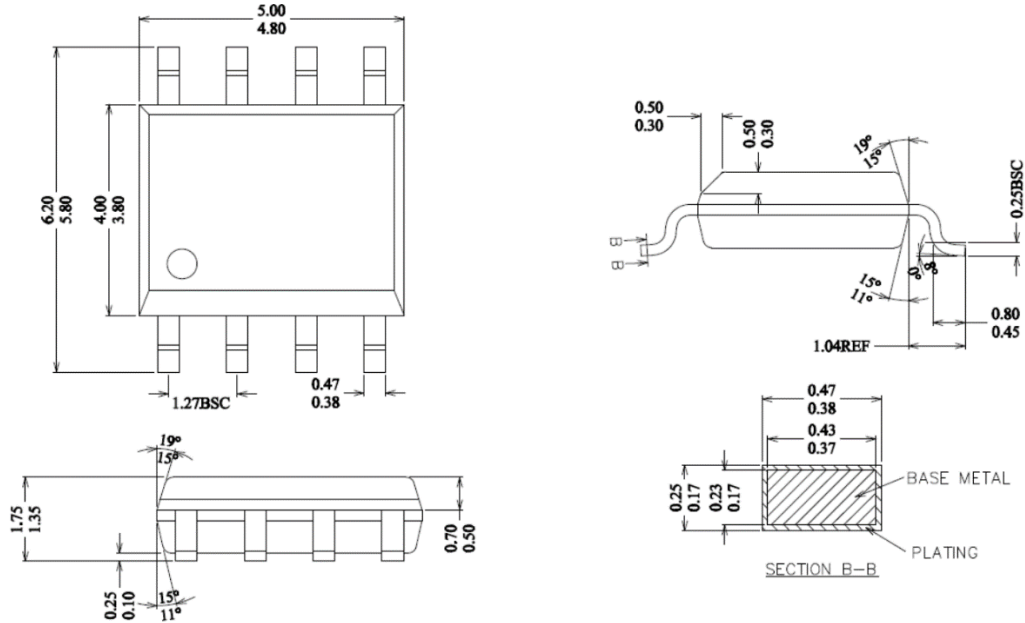


Figure 17. Common-mode transient immunity (CMTI) measurement

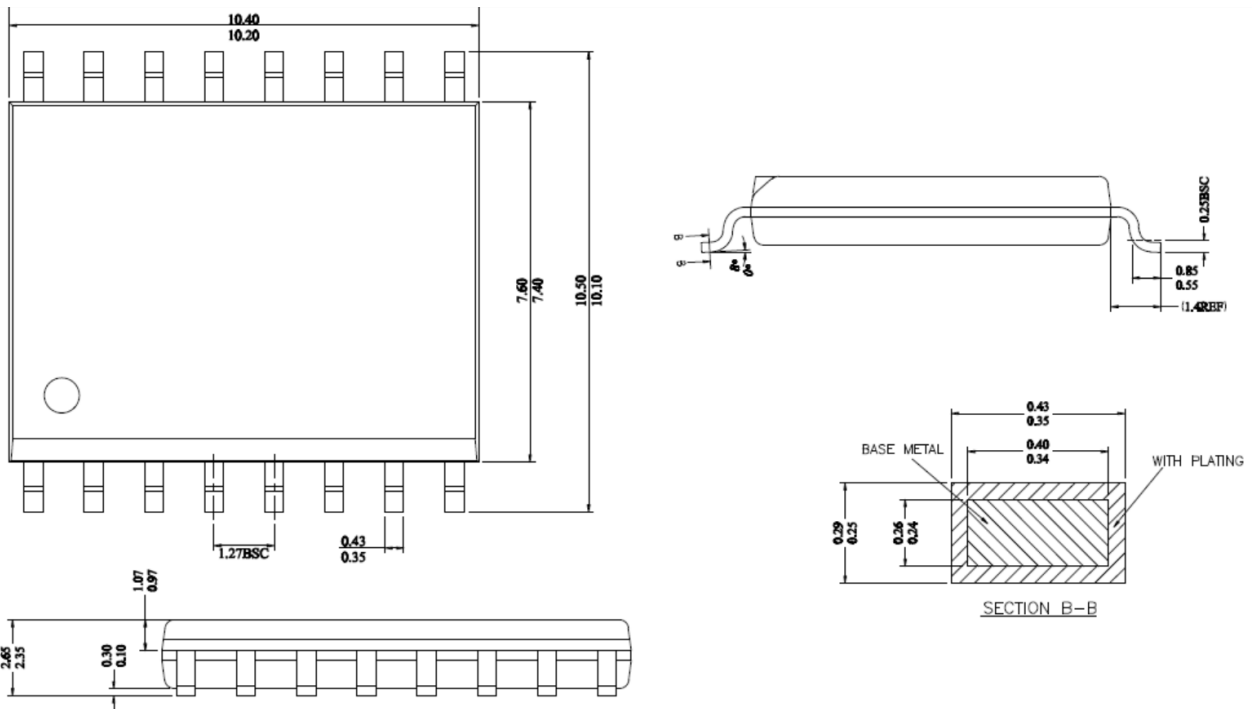
To measure the Common-Mode Transient Immunity (CMTI) of ISO77xx isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM), such that the maximum common-mode slew rates (dVCM/dt) can be applied to ISO77xx isolator coupler under measurement. The common-mode pulse is applied between one side ground  $GND_1$  and the other side ground  $GND_2$  of ISO77xx isolator, and shall be capable of providing positive transients as well as negative transients.

# OUTLINE DIMENSIONS



NOTES:  
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA  
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 18. 8-Lead Narrow Body SOIC [NB SOIC-8] Outline Package-dimension unit(mm)

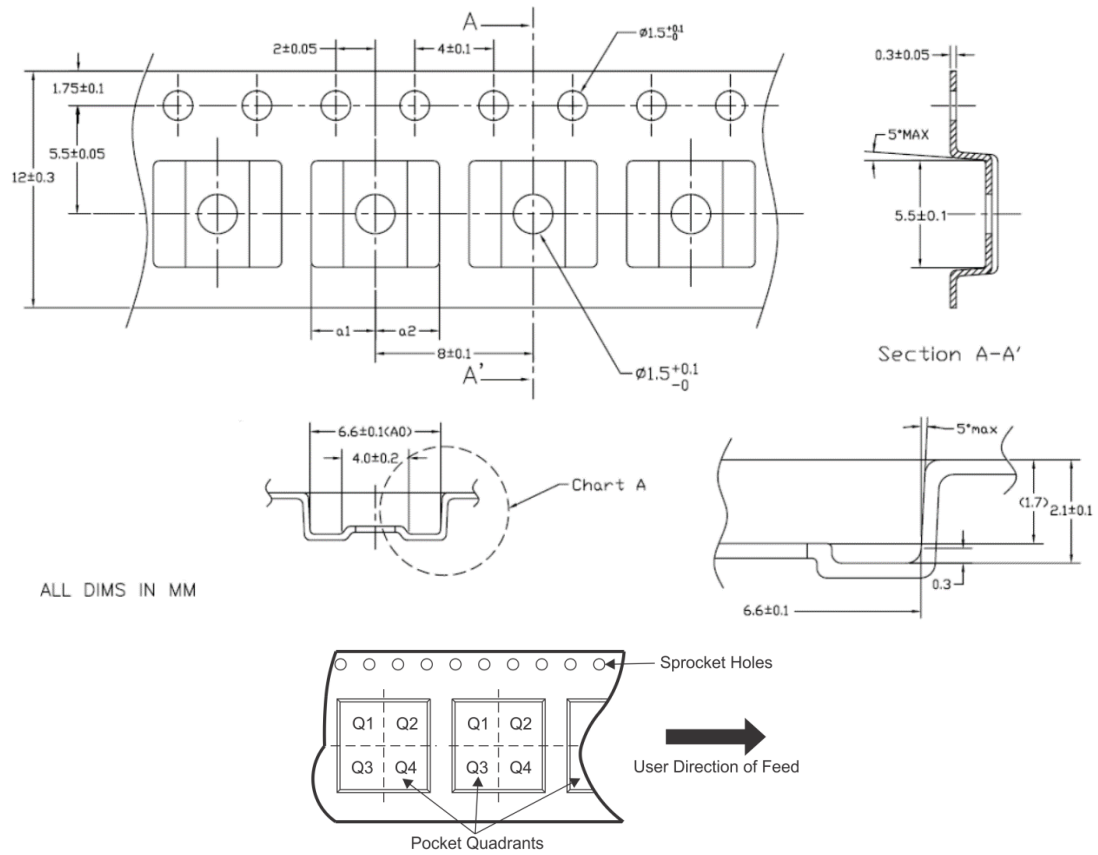


Notes:  
ALL DIMENSIONS MEET JEDEC STANDARD MS-013 AA  
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 19. 16-Lead Wide Body SOIC [WB SOIC-16] Outline Package-dimension unit(mm)

## REEL INFORMATION

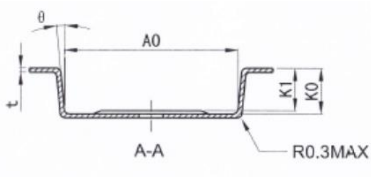
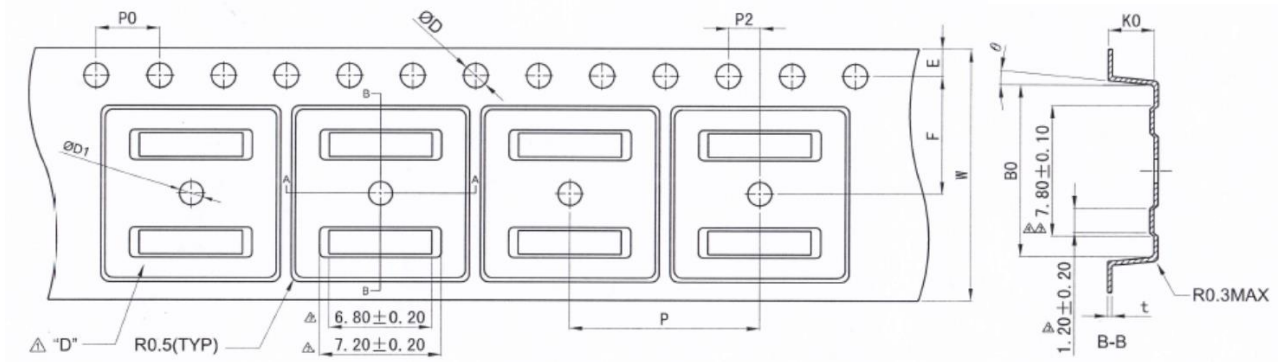
8-Lead Narrow Body SOIC [NB SOIC-8]



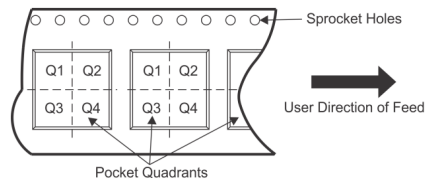
Note: The Pin 1of the chip is in the quadrant Q1

Figure 23. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information—dimension unit(mm)

16-Lead Wide Body SOIC [WB SOIC-16]



Items	Size(mm)	Items	Size(mm)
W	16.00±0.30	W	16.00±0.30
E	1.75±0.10	P	12.00±0.10
F	7.50±0.05	A0	10.90±0.10
P2	2.00±0.05	B0	10.80±0.10
D	1.55±0.05	K0	3.00±0.10
D1	1.5±0.10	t	0.30±0.05
P0	4.00±0.10	K1	2.70±0.10
10P0	40.00±0.20	θ	5° TYP



Note: The Pin 1 of the chip is in the quadrant Q1

Figure 24. 16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

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