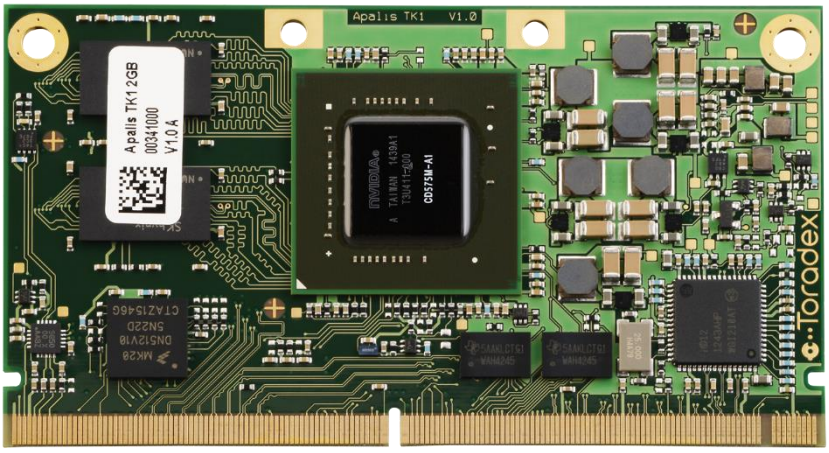
Toradex
Swiss. Embedded. Computing.

Apalis TK1

Datasheet



Revision History

Date	Doc. Rev.	Apalis TK1 Version	Changes
23-Feb-2016	Rev. 0.9	V1.0A	Initial Release
09-Jun-2016	Rev. 1.0	V1.0A V1.0B	Add module picture on the front page Section 8: add reference to the errata document Section 9.6: add reference for suitable heatsink Minor changes
07-Jul-2016	Rev. 1.1	V1.0C	Section 6.5.5: Add routing information to eDP interface Section 9.6: Correct operation temperature (extend) Minor changes
29-Sep-2016	Rev. 1.2	V1.1A	Update assignment of pin 190 (SD1_CD#) according to changes in PCB version 1.1 Adding a recommendation to non-used input level shifted signals
07-Nov-2017	Rev. 1.3	V1.2A	Section 1: Correction of maximum CPU frequency Section 1.3.3: Add remark to eMMC flash endurance Section 1.3.4: Update number of available interfaces Section 1.4: Update number of available interfaces Section 3.2: Update pin assignment Section 4.5: Update function list Section 6.2: Update GPIOs and Wake source Section 6.3: Add IEEE1588 function and SPD pins Section 6.4: Update pin assignment Section 6.5: Update DDC interface pins, clarify USB 3.0 OTG Section 6.8: Update DDC pins, remove I2C on Pin 5/7 Section 6.18: Add information about unused touch signals Section 6.19: Correct I/O direction of CSI clock Section 9.1: Correction of Vmax USBO1_VBUS Section 9.3: Typical consumption values added
08-Oct-2018	Rev. 1.4	V1.2A	Section 3.2: rename DAP1_RESET to DAP1_RESET# Section 6.14: correct SGTL500 pin number for AAP1_HP_L Section 6.15: rename DAP1_RESET to DAP1_RESET# Section 9.5: correct SoC position in Figure 13 Section 9.6: correct junction temperature specification
30-Sep-2020	Rev. 1.5	V1.2A	Section 9.5.1: Update the MXM3 connector
07-Jan-2021	Rev. 1.6	V1.3A	Update Figure 3 and Figure 4 Section 6.8: Correction of the description of I^2C ports Spelling corrections Minor changes

Contents

1. Introduction 5
1.1 Hardware 5
1.2 Software 5
1.3 Main Features 6
1.3.1 CPU 6
1.3.2 MCU 6
1.3.3 Memory 6
1.3.4 Interfaces 7
1.3.5 Graphics Processing Unit 8
1.3.6 HD Video Decode 8
1.3.7 HD Video Encode 8
1.3.8 Supported Operating Systems 8
1.4 Interface Overview 8
1.5 Reference Documents 9
1.5.1 NVIDIA Tegra K1 9
NXP (Freescale) K20 10
1.5.2 Ethernet Controller 10
1.5.3 Audio Codec 10
1.5.4 Apalis Carrier Board Design Guide 10
1.5.5 Layout Design Guide 10
1.5.6 Toradex Developer Center 10
1.5.7 Apalis Evaluation Board Schematics 10
1.5.8 Toradex Pinout Designer 10

2. Architecture Overview 11
2.1 Block Diagram 11

3. Apalis TK1 Connectors 12
3.1 Pin Numbering 12
3.2 Assignment 12

4. Tegra K1 I/O Pins 18
4.1 I/O Pin Types 18
4.1.1 3.3V Signals 18
4.1.2 1.8V/3.3V Signals 18
4.1.3 3.3V Tolerant Signals 19
4.1.4 Output Shifted Signals 19
4.1.5 Input Shifted Signals 19
4.1.6 Bidirectional Shifted Signals 20
4.2 TK1 Pin Control 20
4.3 TK1 Function Multiplexing 21
4.4 Pin Reset Status 21
4.5 TK1 Functions List 21

5. Kinetis K20 Companion MCU I/O Pins 27
5.1 K20 Pin Control 28
5.2 K20 Functions List 29

6. Interface Description 32
6.1 Power Signals 32
6.1.1 Digital Supply 32
6.1.2 Analogue Supply 32
6.1.3 Power Management Signals 32
6.2 GPIOs 33
6.2.1 Wakeup Source 33
6.3 Ethernet 34
6.4 USB 34

6.4.1 USB Data Signal 35
6.4.2 USB Control Signals 36
6.5 Display 36
6.5.1 Parallel RGB LCD interface 36
6.5.2 LVDS 36
6.5.3 HDMI 39
6.5.4 Analog VGA 40
6.5.5 Embedded Display Port (eDP) 40
6.5.6 Display Serial Interface (DSI) 41
6.6 PCI Express 43
6.7 SATA 44
6.8 I²C 44
6.8.1 Real-Time Clock (RTC) recommendation 45
6.9 UART 46
6.10 SPI 48
6.11 PWM (Pulse Width Modulation) 50
6.12 OWR (One Wire) 52
6.13 SD/MMC 52
6.14 Analog Audio 55
6.15 Digital Audio 55
6.16 S/PDIF (Sony-Philips Digital Interface I/O) 56
6.17 Touch Panel Interface 56
6.18 Analog Inputs 57
6.19 Camera Interface 58
6.20 Clock Output 60
6.21 Keypad 61
6.22 Controller Area Network (CAN) 61
6.23 JTAG 62

7. Recovery Mode 63

8. Known Issues 64

9. Technical Specifications 65
9.1 Absolute Maximum Ratings 65
9.2 Recommended Operation Conditions 65
9.3 Electrical Characteristics 65
9.4 Power Ramp-Up Time Requirements 65
9.5 Mechanical Characteristics 66
9.5.1 Sockets for the Apalis Modules 66
9.6 Thermal Specification 67
9.7 Product Compliance 67

1. Introduction

1.1 Hardware

The Apalis TK1 is a computer module based on the NVIDIA® Tegra® K1 embedded System on Chip (SoC). The Cortex A15 quad-core CPU peaks up to 2.1 GHz (2.07 GHz). Additionally, the Tegra K1 features a fifth low-power Cortex A15 processor, which can be used instead of the four high-performance cores during low compute workload operations.

The Tegra K1 features a powerful NVIDIA® GeForce® Kepler™ Mobile Graphics Processing Unit (GPU), which extends the CUDA® compute architecture to low power consumption devices. Due to its 192 CUDA cores, the GPU shader can peak with up to 325 GFLOPS and supports OpenGL® 4.4 and OpenGL® ES 3.1.

The Apalis TK1 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling, enabling the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

Besides the powerful NVIDIA Tegra K1 SoC, the Apalis TK1 features an NXP (Freescale) Kinetis K20 Micro Controller Unit (MCU) as a companion. The K20 features a low power ARM Cortex M4 processor which runs up to 100MHz. The MCU extends the module with two Controller Area Network (CAN) interfaces, several ADC, additional GPIOs, and several other low-speed interfaces. Since the controller is independent of the Tegra K1, it can be used for hard real-time and security-critical tasks.

The module targets a wide range of applications, including Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming, and much more

It offers a wide range of interfaces from simple GPIOs, industry-standard I2C, and SPI buses through to high-speed USB 3.0 interfaces, high-speed PCI Express, and SATA. The HDMI and LVDS interfaces make it very easy to connect large, full HD, and beyond resolution displays.

The Apalis TK1 module encapsulates the complexity associated with modern-day electronic design, such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology. This allows the customer to create a carrier board that implements the application-specific electronics, which is generally much less complicated. The Apalis TK1 module takes this one step further and implements an interface pinout, which allows direct connection of real-world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed, serial technologies that use impedance controlled differential pairs. It allows them to easily route such interfaces to standard connectors in a simple, robust fashion.

1.2 Software

The Apalis TK1 comes with a preinstalled Embedded Linux Images. Android is available from Toradex partners.

1.3 Main Features

1.3.1 CPU

	Apalis TK1 2GB
NVIDIA SoC	CD575M-A1
CPU Cores	4+1
ARM Cortex Version	A15
L1 Instruction Cache (each core)	32KByte
L1 Data Cache (each core)	32KByte
L2 Cache (shared by cores)	2MByte
NEON MPE	✓
Maximum CPU frequency	2.07GHz

1.3.2 MCU

	Apalis TK1 2GB
NXP MCU	MK20DN512VMC10
CPU Cores	1
ARM Cortex Version	M4
Maximum CPU frequency	100MHz
SRAM	128KByte
Flash Memory	512KByte

1.3.3 Memory

	Apalis TK1 2GB
DDR3L RAM Size	2GByte
DDR3L RAM Speed	1848MT/s
DDR3L RAM Memory Width	64bit
eMMC NAND Flash (8bit)*	16GByte

* eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear-leveling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.3.4 Interfaces

	Apalis TK1 2GB
LCD RGB (24bit, 225 Mpixel/s)	-
LVDS (1x single channel 165 MHz)	1
HDMI 1.4b (max 4096x2160)	1
VGA Analogue Video	-
eDP	1*
MIPI DSI	1x 4 Data Lanes* + 1x 2 Data Lanes*
Resistive Touch Screen	4 Wire
Analog Audio Headphone out	1 (Stereo)
Analog Audio Line in	1 (Stereo)
Analog Audio Mic-in	1 (Mono)
I^2S	1
S/PDIF	1 in / 1 out
Parallel Camera Interface	-
MIPI CSI-2	2x 4 Data Lanes* + 1x 1 Data Lane*
I^2C	3+3*
SPI	2+3*
UART	4+6*
SD/SDIO/MMC	2+1*
GPIO	87*
USB 3.0 OTG (host/device)	1
USB 3.0 host	1
USB 2.0 host	1
PCIe (Gen 2.0)	1+1* (max. 1x2 + 1x1)
Serial ATA II (3Gbit/s)	1
10/100/1000 MBit/s Ethernet	1
Ethernet Controller	Intel I210
PWM	4+12*
Analog Inputs	4*17*
CAN	2

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the type-specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. Some interfaces are provided by the companion MCU. The software support for the MCU interfaces might be limited. For more information, please check the list of type-specific interfaces in section 1.4 and the description of the associated interface in section 5

1.3.5 Graphics Processing Unit

	Apalis TK1 2GB
Kepler Mobile GPU Units	1
CUDA cores	192
OpenGL® ES 3.1	✓
OpenGL 4.4	✓
DirectX 12	✓
PhysX	✓

1.3.6 HD Video Decode

- ✓ MPEG-2 – 1080p60
- ✓ MPEG4/XviD (Simple Profile) – 1080p30
- ✓ H.264 (Baseline, Main, High, Stereo SEI Profile) – 2160p30, 1440p60, 1080p120
- ✓ H.264 Multiple Stream – 4x 1080p30
- ✓ VC1 (Simple, Main, Advanced Profile) – 2160p30, 1080p120
- ✓ WEBM VP8 – 2160p30, 1080p120
- ✓ MJPEG – 120MPixel/s

1.3.7 HD Video Encode

- ✓ MPEG4 (Simple Profile)
- ✓ H.263 (Profile 0)
- ✓ H.264 (Baseline, Main, High, Stereo SEI Profile) – 2160p24, 1440p30, 1080p60)
- ✓ WEBM VP8 – 2160p24, 1440p30, 1080p60)
- ✓ MJPEG –120MPixel/s
- ✓ VC1 (Advanced Profile) –720p30

1.3.8 Supported Operating Systems

- ✓ Embedded Linux
- ✓ Android available through Toradex partners

1.4 Interface Overview

The table in Figure 1 shows the interfaces supported on the Apalis® TK1 module and whether an interface is provided on standard or type-specific pins. Additionally, the table shows also whether the interface is provided by the NVIDIA Tegra K1 SoC or by the NXP K20 MCU. The I²C interface is an example of an interface that makes use of standard and type-specific pins – three USB ports are provided as part of the standard interface pinout. Additionally, four ports are type-specific. The SoC does not provide two out of these additional four ports. They are provided by the companion MCU.

The CAN, analog inputs, and the resistive touch interface provided by the MCU will be supported in the Toradex Linux image. Other interfaces provided by the MCU might be not supported by the standard OS image.

Some interfaces are available as an alternate function of a pin. This function can only be used if the primary function of the pin is not used. Check section 4.5 for a list of all alternate functions of the MXM3 pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Colibri iMX7 Module. The tool allows comparing the interfaces of different Colibri modules. More information on this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	TK1 SoC	K20 MCU	Standard	Type Specific	Alternate Function
4 Wire Resistive Touch	4		4	4		
Analog Inputs	21		21	4		17
Analog Audio (Line-in/out, Mic-in)	1			1		
CAN	2		2	2		
CSI Ports	3	3			3	
DSI Ports	2	2			2	
Single Channel LVDS Display	1	1		1		
Gigabit Ethernet	1			1		
GPIO	87	36	51	8	4	74
GPI (Only Input possible)	15	15				15
GPO (Only Output possible)	24	24				24
I^2S	1	1		1		
HDMI (TDMS)	1	1		1		
eDP	1	1				1
I^2C	6	4	2	3		3
Parallel Camera						
Parallel LCD						
PCI-Express (lane count)	3	3		1	1	1
PWM	16	4	12	4		12
SATA	1	1		1		
SD/SDIO/MMC	3	2	1	2		1
S/PDIF In	1	1		1		
S/PDIF Out	1	1		1		
SPI	5	3	2	2		3
UART	10	4	6	4		6
USB 3.0 host/device	1	1		1		
USB 3.0 host	1	1		1		
USB 2.0 host	1	1		1		
USB 1.1 host	1		1	1		
VGA						

Figure 1: Apalis® TK1 Module Interfaces

1.5 Reference Documents

1.5.1 NVIDIA Tegra K1

You will find the details about Tegra K1 SoC in the Datasheet and Reference Manual provided by NVIDIA (registration required).
https://developer.nvidia.com/tegra-k1-technical-reference-manual

NXP (Freescale) K20

You will find the details about Kinetis K20 MCU in the Datasheet and Reference Manual provided by NXP.
http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/kinetis-cortex-m/k-series/k2x-usb-mcus/kinetis-k20-100-mhz-usb-high-precision-analog-integration-serial-communication-microcontrollers-mcus:K20_100

1.5.2 Ethernet Controller

Apalis TK1 uses the Intel I210-AT Gigabit Ethernet Controller Chip.
http://ark.intel.com/products/64400/Intel-Ethernet-Controller-I210-AT?wapkw=i210

1.5.3 Audio Codec

Apalis TK1 uses the NXP SGTL5000 Audio Codec.
http://www.nxp.com/products/interface-and-connectivity/interface-and-system-management/switch-monitoring-ics/ultra-low-power-audio-codec:SGTL5000

1.5.4 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide to make the board compatible with the Apalis module family. Please study this document in detail before starting your carrier board design.
http://docs.toradex.com/101123-apalis-arm-carrier-board-design-guide.pdf

1.5.5 Layout Design Guide

This document contains information about high-speed layout design and additional information to get the carrier board layout the first time right.
http://docs.toradex.com/102492-layout-design-guide.pdf

1.5.6 Toradex Developer Center

You can find much additional information in the Toradex Developer Center, updated regularly with the latest product support information.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Apalis TK1.
http://www.developer.toradex.com

1.5.7 Apalis Evaluation Board Schematics

We provide the completed schematics plus the Altium project file, including library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board free of charge. This is of great help when designing your own Carrier Board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.5.8 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

2. Architecture Overview

2.1 Block Diagram

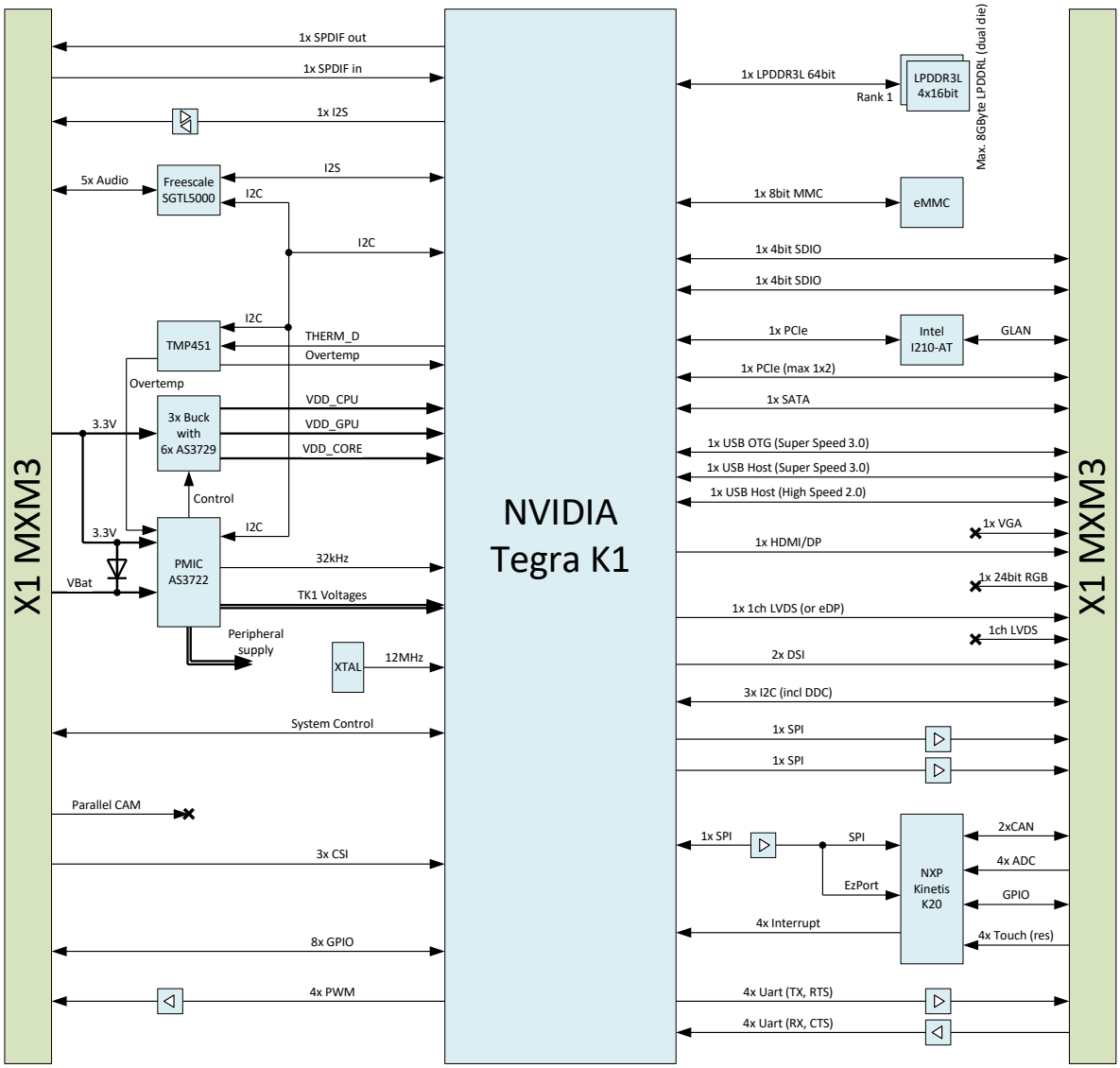


Figure 2 Apalis TK1 Block Diagram

3. Apalis TK1 Connectors

3.1 Pin Numbering

The diagrams in Figure 3 and Figure 4 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema. Pins on the top side of the module have even numbers, and pins on the bottom side have odd numbers.

The pin number increases linearly as a multiple of the pitch – that is, pins that are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins that do not exist due to the connector notch are also accounted for (pins 166 through 172).

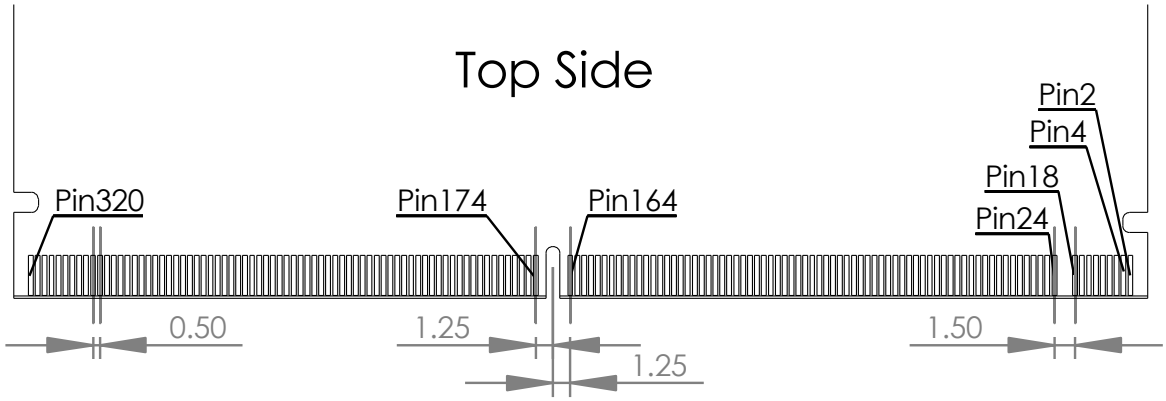


Figure 3: Pin numbering schema on the top side of the module

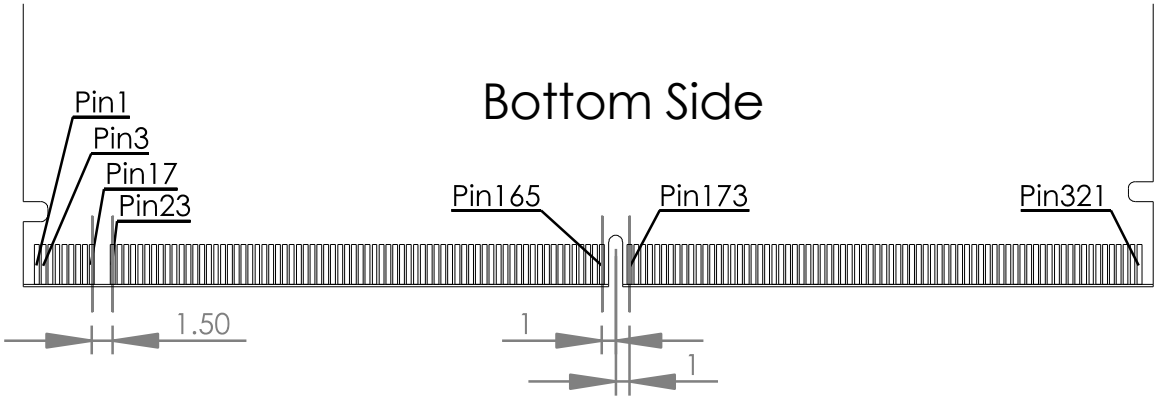


Figure 4: Pin numbering schema on the bottom side of the module

3.2 Assignment

The following table describes the MXM3 connector pinout. Some pins are shaded dark grey as type-specific interfaces. These pins might not be compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that type-specific interfaces will be kept standard across modules that share such interfaces wherever possible. For example, suppose both module A and module B have three additional PCI-Express lanes available in the same configurations as a type-specific interface. In that case, they shall be assigned to the same pins in

the type-specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

- X1: Pin number on the MXM3 module edge connector (X1).
- Apalis Signal Name: The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have an alternate function, but to be compatible with other Apalis modules, only the default function should be used, and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- TK1 Ball Name: The name of the pin of the Tegra K1 SoC.

Table 3-1 X1 Connector

X1	Apalis Signal Name	TK1 Ball Name	Notes	X1	Apalis Signal Name	TK1 Ball Name	Notes
1	GPIO1	GPIO_PFF2		2	PWM1	GPIO_PH0	Output Shifter
3	GPIO2	DP_HPD		4	PWM2	GPIO_PH1	Output Shifter
5	GPIO3	USB_VBUS_EN0		6	PWM3	GPIO_PH2	Output Shifter
7	GPIO4	USB_VBUS_EN1		8	PWM4	GPIO_PH3	Output Shifter
9	GND			10	VCC		
11	GPIO5	PEX_L1_RST_N		12	CAN1_RX		K20 PTA13
13	GPIO6	PEX_L1_CLKREQ_N / OWR	Two Soc Pins connected	14	CAN1_TX		K20 PTA12
15	GPIO7	PEX_L0_RST_N		16	CAN2_RX		K20 PTC16
17	GPIO8	PEX_L0_CLKREQ_N		18	CAN2_TX		K20 PTC17
23	GND			24	POWER_ENABLE_MOCI		PWR Management
25	SATA1_RX+	SATA_L0_RXP		26	RESET_MOCI#		PWR Management
27	SATA1_RX-	SATA_L0_RXN		28	RESET_MICO#		PWR Management
29	GND			30	VCC		
31	SATA1_TX-	SATA_L0_TXN		32	ETH1_MDI2+		I210 Pin 32
33	SATA1_TX+	SATA_L0_TXP		34	ETH1_MDI2-		I210 Pin 34
35	SATA1_ACT#	DAP1_DOUT	Output Shifter	36	VCC		
37	WAKE1_MICO	PEX_WAKE_N		38	ETH1_MDI3+		I210 Pin 38
39	GND			40	ETH1_MDI3-		I210 Pin 40
41	PCIE1_RX-	PEX_RX4N		42	ETH1_ACT		I210 Pin 42
43	PCIE1_RX+	PEX_RX4P		44	ETH1_LINK		I210 Pin 44
45	GND			46	ETH1_CTREF		NC
47	PCIE1_TX-	PEX_TX4N		48	ETH1_MDI0-		I210 Pin 57
49	PCIE1_TX+	PEX_TX4P		50	ETH1_MDI0+		I210 Pin 58
51	GND			52	VCC		
53	PCIE1_CLK-	PEX_CLK1N		54	ETH1_MDI1-		I210 Pin 54

X1	Apalis Signal Name	TK1 Ball Name	Notes
55	PCIE1_CLK+	PEX_CLK1P	
57	GND		
59	TS_DIFF1-	PEX_RX3N	
61	TS_DIFF1+	PEX_RX3P	
63	TS_1		Recovery Circuit
65	TS_DIFF2-	PEX_TX3N	
67	TS_DIFF2+	PEX_TX3P	
69	GND		
71	TS_DIFF3-	DP_AUX_CH0_N	
73	TS_DIFF3+	DP_AUX_CH0_P	
75	GND		
77	TS_DIFF4-	DSI_A_D1_N	
79	TS_DIFF4+	DSI_A_D1_P	
81	GND		
83	TS_DIFF5-	DSI_A_D0_N	
85	TS_DIFF5+	DSI_A_D0_P	
87	TS_2		PMIC Power Button
89	TS_DIFF6-	DSI_A_CLK_N	
91	TS_DIFF6+	DSI_A_CLK_P	
93	GND		
95	TS_DIFF7-	CSI_E_D0_N	
97	TS_DIFF7+	CSI_E_D0_P	
99	TS_3		I210 Pin 63 SDP0
101	TS_DIFF8-	DSI_B_D3_N	
103	TS_DIFF8+	DSI_B_D3_P	
105	GND		
107	TS_DIFF9-	DSI_B_D2_N	
109	TS_DIFF9+	DSI_B_D2_P	
111	GND		
113	TS_DIFF10-	DSI_B_D1_N	
115	TS_DIFF10+	DSI_B_D1_P	
117	GND		
119	TS_DIFF11-	DSI_B_D0_N	
121	TS_DIFF11+	DSI_B_D0_P	
123	TS_4		I210 Pin 61 SDP1
125	TS_DIFF12-	DSI_B_CLK_N	

X1	Apalis Signal Name	TK1 Ball Name	Notes
56	ETH1_MDI1+		I210 Pin 55
58	VCC		
60	USBO1_VBUS	USB0_VBUS	
62	USBO1_SSRX+	PEX_USB3_RX1P	
64	USBO1_SSRX-	PEX_USB3_RX1N	
66	VCC		
68	USBO1_SSTX+	PEX_USB3_TX1P	
70	USBO1_SSTX-	PEX_USB3_TX1N	
72	USBO1_ID	USB0_ID	
74	USBO1_D+	USB0_DP	
76	USBO1_D-	USB0_DN	
78	VCC		
80	USBH2_D+	USB1_DP	
82	USBH2_D-	USB1_DN	
84	USBH_EN	GEN2_I2C_SDA	Output Shifter
86	USBH3_D+		K20 USB0_DP
88	USBH3_D-		K20 USB0_DM
90	VCC		
92	USBH4_SSRX-	USB3_RX0N	
94	USBH4_SSRX+	USB3_RX0P	
96	USBH_OC#	GPIO_PBB0	Input Shifter
98	USBH4_D+	USB2_DP	
100	USBH4_D-	USB2_DN	
102	VCC		
104	USBH4_SSTX-	USB3_TX0N	
106	USBH4_SSTX+	USB3_TX0P	
108	VCC		
110	UART1_DTR	UART3_RTS_N	Output Shifter
112	UART1_TXD	GPIO_PU0	Output Shifter
114	UART1_RTS	GPIO_PU3	Output Shifter
116	UART1_CTS	GPIO_PU2	Input Shifter
118	UART1_RXD	GPIO_PU1	Input Shifter
120	UART1_DSR	UART3_CTS_N	Input Shifter
122	UART1_RI	GPIO_PK7	Input Shifter
124	UART1_DCD	GPIO_PB1	Input Shifter
126	UART2_TXD	UART2_TXD	Output Shifter

X1	Apalis Signal Name	TK1 Ball Name	Notes
127	TS_DIFF12+	DSI_B_CLK_P	
129	GND		
131	TS_DIFF13-	CSI_E_CLK_N	
133	TS_DIFF13+	CSI_E_CLK_P	
135	TS_5		I210 Pin 62 SDP2
137	TS_DIFF14-	CSI_B_D1_N	
139	TS_DIFF14+	CSI_B_D1_P	
141	GND		
143	TS_DIFF15-	CSI_B_D0_N	
145	TS_DIFF15+	CSI_B_D0_P	
147	GND		
149	TS_DIFF16-	CSI_A_D1_N	
151	TS_DIFF16+	CSI_A_D1_P	
153	GND		
155	TS_DIFF17-	CSI_A_D0_N	
157	TS_DIFF17+	CSI_A_D0_P	
159	TS_6		NC
161	TS_DIFF18-	CSI_A_CLK_N	
163	TS_DIFF18+	CSI_A_CLK_P	
165	GND		
173	CAM1_D7		K20 PTE1
175	CAM1_D6		K20 PTE0
177	CAM1_D5		K20 PTB17
179	CAM1_D4		K20 PTE3
181	CAM1_D3		K20 PTE5
183	CAM1_D2		K20 PTE24
185	CAM1_D1		K20 PTE4
187	CAM1_D0		K20 PTA17
189	GND		
191	CAM1_PCLK		K20 PTE25
193	CAM1_MCLK	CAM_MCLK	Output Shifter
195	CAM1_VSYNC		K20 PTA5
197	CAM1_HSYNC		K20 PTA3

X1	Apalis Signal Name	TK1 Ball Name	Notes
128	UART2_RTS	UART2_RTS_N	Output Shifter
130	UART2_CTS	UART2_CTS_N	Input Shifter
132	UART2_RXD	UART2_RXD	Input Shifter
134	UART3_TXD	UART3_TXD	Output Shifter
136	UART3_RXD	UART3_RXD	Input Shifter
138	UART4_TXD	GPIO_PJ7	Output Shifter
140	UART4_RXD	GPIO_PB0	Input Shifter
142	GND		
144	MMC1_D2	SDMMC1_DAT2	
146	MMC1_D3	SDMMC1_DAT3	
148	MMC1_D4	CLK2_REQ	
150	MMC1_CMD	SDMMC1_CMD	
152	MMC1_D5	CLK2_OUT	
154	MMC1_CLK	SDMMC1_CLK	
156	MMC1_D6	SDMMC3_CLK_LB_IN	
158	MMC1_D7	USB_VBUS_EN2	
160	MMC1_D0	SDMMC1_DAT0	
162	MMC1_D1	SDMMC1_DAT1	
164	MMC1_CD#	SDMMC1_WP_N	
174	VCC_BACKUP		
176	SD1_D2	SDMMC3_DAT2	
178	SD1_D3	SDMMC3_DAT3	
180	SD1_CMD	SDMMC3_CMD	
182	GND		
184	SD1_CLK	SDMMC3_CLK	
186	SD1_D0	SDMMC3_DAT0	
188	SD1_D1	SDMMC3_DAT1	
190	SD1_CD#	SDMMC3_CD_N	Input Shifter (diode circuit)
192	GND		
194	DAP1_MCLK	CLK3_OUT	Output Shifter
196	DAP1_D_OUT	DAP2_DOUT	Output Shifter
198	DAP1_RESET#		Output Shifter

X1	Apalis Signal Name	TK1 Ball Name	Notes
199	GND		
201	I2C3_SDA (CAM)	CAM_I2C_SDA	1.8V signal, 3.3V tolerant
203	I2C3_SCL (CAM)	CAM_I2C_SCL	1.8V signal, 3.3V tolerant
205	I2C2_SDA (DDC)	DDC_SDA	OD and input only
207	I2C2_SCL (DDC)	DDC_SCL	OD and input only
209	I2C1_SDA	GEN1_I2C_SDA	1.8V signal, 3.3V tolerant
211	I2C1_SCL	GEN1_I2C_SCL	1.8V signal, 3.3V tolerant
213	GND		
215	SPDIF1_OUT	SPDIF_OUT	
217	SPDIF1_IN	SPDIF_IN	
219	GND		
221	SPI1_CLK	ULPI_NXT	Output Shifter
223	SPI1_MISO	ULPI_DIR	Input Shifter
225	SPI1_MOSI	ULPI_CLK	Output Shifter
227	SPI1_CS	ULPI_STP	Output Shifter
229	SPI2_MISO	GPIO_PG7	Input Shifter
231	SPI2_MOSI	GPIO_PG6	Output Shifter
233	SPI2_CS	GPIO_PI3	Output Shifter
235	SPI2_CLK	GPIO_PG5	Output Shifter
237	GND		
239	BKL1_PWM	GPIO_PU6	Output Shifter
241	GND		
243	LCD1_PCLK		K20 PTD7
245	LCD1_VSYNC		K20 PTD5
247	LCD1_HSYNC		K20 PTD4
249	LCD1_DE		K20 PTC4
251	LCD1_R0		K20 PTD9
253	LCD1_R1		K20 PTD8
255	LCD1_R2		K20 PTD6
257	LCD1_R3		K20 PTD3
259	LCD1_R4		K20 PTC7
261	LCD1_R5		K20 PTC3
263	LCD1_R6		K20 PTC0
265	LCD1_R7		K20 PTB16
267	GND		
269	LCD1_G0		K20 PTD12

X1	Apalis Signal Name	TK1 Ball Name	Notes
200	DAP1_BIT_CLK	DAP2_SCLK	Bidirectional Shifter
202	DAP1_D_IN	DAP2_DIN	Input Shifter
204	DAP1_SYNC	DAP2_FS	Bidirectional Shifter
206	GND		
208	VGA1_R		NC
210	VGA1_G		NC
212	VGA1_B		NC
214	VGA1_HSYNC		NC
216	VGA1_VSYNC		NC
218	GND		
220	HDMI1_CEC	HDMI_CEC	
222	HDMI1_TXD2+	HDMI_TXD2P	
224	HDMI1_TXD2-	HDMI_TXD2N	
226	GND		
228	HDMI1_TXD1+	HDMI_TXD1P	
230	HDMI1_TXD1-	HDMI_TXD1N	
232	HDMI1_HPD	HDMI_INT	Level shifted
234	HDMI1_TXD0+	HDMI_TXD0P	
236	HDMI1_TXD0-	HDMI_TXD0N	
238	GND		
240	HDMI1_TXC+	HDMI_TXCP	
242	HDMI1_TXC-	HDMI_TXCN	
244	GND		
246	LVDS1_A_CLK-	LVDS0_TXD4N	
248	LVDS1_A_CLK+	LVDS0_TXD4P	
250	GND		
252	LVDS1_A_TX0-	LVDS0_TXD0N	
254	LVDS1_A_TX0+	LVDS0_TXD0P	
256	GND		
258	LVDS1_A_TX1-	LVDS0_TXD1N	
260	LVDS1_A_TX1+	LVDS0_TXD1P	
262	USBO1_OC#	GPIO_PBB4	Input Shifter
264	LVDS1_A_TX2-	LVDS0_TXD2N	
266	LVDS1_A_TX2+	LVDS0_TXD2P	
268	GND		
270	LVDS1_A_TX3-	LVDS0_TXD3N	

X1	Apalis Signal Name	TK1 Ball Name	Notes
271	LCD1_G1		K20 PTD11
273	LCD1_G2		K20 PTD2
275	LCD1_G3		K20 PTC6
277	LCD1_G4		K20 PTC2
279	LCD1_G5		K20 PTB19
281	LCD1_G6		K20 PTB11
283	LCD1_G7		K20 PTD14
285	GND		
287	LCD1_B0		K20 PTD13
289	LCD1_B1		K20 PTD1
291	LCD1_B2		K20 PTD0
293	LCD1_B3		K20 PTC1
295	LCD1_B4		K20 PTB18
297	LCD1_B5		K20 PTB10
299	LCD1_B6		K20 PTD15
301	LCD1_B7		K20 PTE2
303	AGND		
305	AN1_ADC0		K20 PTB0
307	AN1_ADC1		K20 PTB1
309	AN1_ADC2		K20 PTB2
311	AN1_TSWIP_ADC3		K20 PTB3
313	AGND		
315	AN1_TSPX		Touch Circuit
317	AN1_TSMX		Touch Circuit
319	AN1_TSPY		Touch Circuit
321	AN1_TSMY		Touch Circuit

X1	Apalis Signal Name	TK1 Ball Name	Notes
272	LVDS1_A_TX3+	LVDS0_TXD3P	
274	USBO1_EN	GEN2_I2C_SCL	Output Shifter
276	LVDS1_B_CLK-		NC
278	LVDS1_B_CLK+		NC
280	GND		
282	LVDS1_B_TX0-		NC
284	LVDS1_B_TX0+		NC
286	BKL1_ON	GPIO_PBB5	Output Shifter
288	LVDS1_B_TX1-		NC
290	LVDS1_B_TX1+		NC
292	GND		
294	LVDS1_B_TX2-		NC
296	LVDS1_B_TX2+		NC
298	GND		
300	LVDS1_B_TX3-		NC
302	LVDS1_B_TX3+		NC
304	AGND		
306	AAP1_MICIN		SGTL5000 Pin 10
308	AGND		
310	AAP1_LIN_L		SGTL5000 Pin 9
312	AAP1_LIN_R		SGTL5000 Pin 8
314	AVCC		
316	AAP1_HP_L		SGTL5000 Pin 4
318	AAP1_HP_R		SGTL5000 Pin 1
320	AVCC		

4. Tegra K1 I/O Pins

4.1 I/O Pin Types

To understand the Tegra K1 I/O Pins' capabilities, we need to distinguish between different types of Pins. The I/O pins are grouped into power rail blocks. Pins in the same block have the same I/O voltage. Since the I/O voltage of some of the blocks is limited to 1.8V, there are level shifters located on the module to get the 3.3V I/O voltage level of the Apalis standard. Since the level shifter changes the pins' behavior and usage, this document needs to distinguish the I/O pin types according to the kind of level shifter.

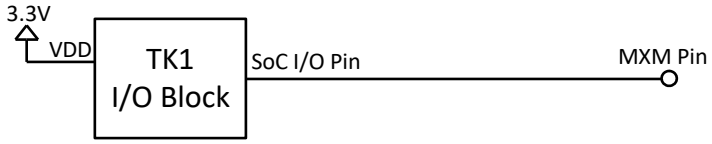
The Tegra K1 SoC itself distinguishes different MPIO Pad Types. The different types are:

- ST: Standard. Most common pads on the SoC.
- DD: Dual Drive. These pins are similar to the standard pin but allow a 3.3V tolerant proper open-drain mode.
- CZ: Controlled Output Impedance. These are mainly the SDMMC interface pins.
- LV: Low Voltage. These pins are optimized for low power supply. The maximum I/O voltage is 1.8V. Therefore, all these pins need to be level shifted on the Apalis module.
- OD: Open Drain: These pins do not have a push-pull output driver.

This differentiation of MPIO Pad Type is only applicable if there is no level shifter present on the module (3.3V, 1.8/3.3V, and 3.3V Tolerant signal types).

4.1.1 3.3V Signals

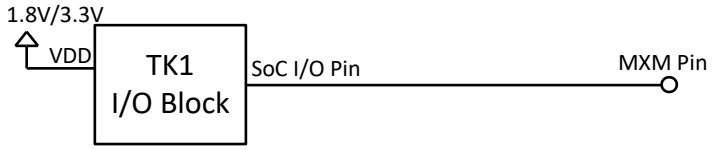
These are regular I/O pins connected directly from the Tegra K1 SoC to the module edge connector. The different functions of the pin can be used without any restriction. The corresponding I/O block supply voltage is 3.3V. The pin can usually be used as input as well as output. Since there is no level shifter between these signals, the Tegra K1 pin control options (for example, enabling internal pull up/down resistors, drive strength, slew rate, etc.) are applicable. More information on the available options can be found in section 4.2 and the NVIDIA reference manual.



4.1.2 1.8V/3.3V Signals

There are two I/O blocks which are sourced by an I/O voltage that can be changed between 1.8V and 3.3V. The I/O voltage of one block can be changed independently from the other block, but all the corresponding block signals change their voltage together. One block contains the signals for the Apalis SD1 interface (TK1 function block SDMMC3), while the other block contains mainly the signals of the Apalis MMC1 interface (TK1 function block SDMMC1).

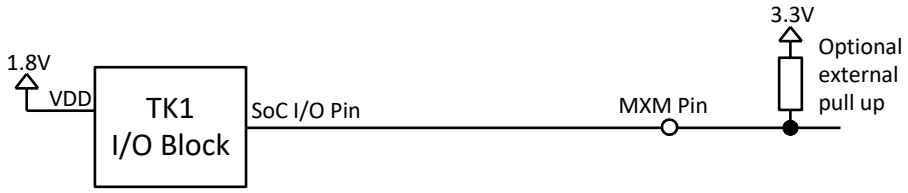
Besides the fact that the I/O voltage of these signals can be changed from 3.3V to 1.8V, the signals are similar to the regular 3.3V signals. This means the signals are also connected directly from the SoC to the module edge pin, and all pin control options are applicable.



4.1.3 3.3V Tolerant Signals

There are a couple of signals (Apalis I2C1 and I2C3 interface signals) with a 1.8V I/O voltage level, but they are 3.3V tolerant. This means, if they are used as output signals, the high level is only 1.8V. The signals can be configured as open drain. It is possible to add a pull-up resistor to 3.3V on the carrier board to get a 3.3V logic level. If the pins are configured to be used as input, the input voltage level is allowed to be up to 3.3V.

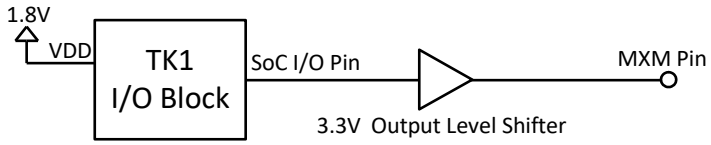
The signals themselves are connected directly from the Tegra K1 SoC to the module edge connector. This means all pin control options are applicable.



4.1.4 Output Shifted Signals

The I/O voltage of the corresponding block on the Tegra K1 is 1.8V. Since the pins on the module edge connector need to be 3.3V (tolerant) according to the Apalis specifications, there are output level shifters on the module. The direction of the level shifter cannot be changed, and the output cannot be disabled. This means these pins can only be used as output. The carrier board is not allowed to drive these pins. It is not possible to use these pins as real GPIO. The pins can only be used as GPO (general purpose output) signals. Due to the signal direction restriction, some alternate functions of these pins might not be usable.

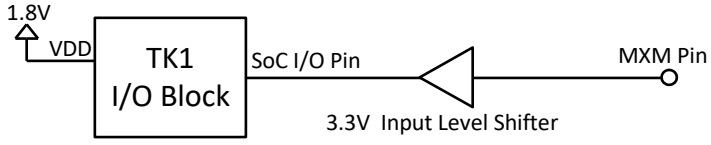
Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the drive strength does not affect the signal's actual drive strength at the module edge connector.



4.1.5 Input Shifted Signals

The I/O voltage of the corresponding block on the Tegra K1 is 1.8V. Since the pins on the module edge connector need to be 3.3V (tolerant) according to the Apalis specifications, there are input level shifters on the module. The level shifter direction cannot be changed, and the level shifter cannot be disabled. This means these pins can only be used as input. It is not possible to use these pins as real GPIO. The pins can only be used as GPI (general purpose input) signals. Due to the restriction of the signal direction, some alternate functions of these pins might be unusable.

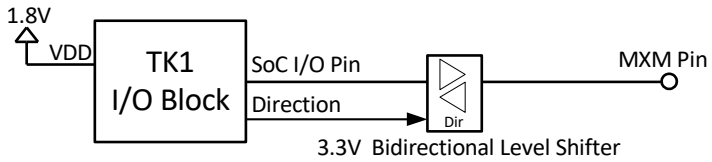
Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the enabling of the internal pull up/down resistors does not affect the input at the module edge connector. Since there are no pull up/down options available at the module edge connector, it is recommended tying the signal to the ground or VCC on the carrier board if unused.



4.1.6 Bidirectional Shifted Signals

There are two signals which feature a bidirectional level shifter. The signals are Pin 200 DAP1_BIT_CLK (TK1 signal DAP2_SCLK) and Pin 204 DAP1_SYNC (TK1 signal DAP2_FS). The direction of the level shifter can be changed from input to output. Noteworthy, the direction cannot be changed individually. It can only be changed for both signals together.

Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the enabling of the internal pull up/down resistors does not affect the input at the module edge connector.



4.2 TK1 Pin Control

As previously described, the Tegra K1 pin control settings are only applicable on pins that do not feature a level shifter on the module (3.3V, 1.8/3.3V, and 3.3V Tolerant signal types). The available pin control settings depend on the MPIO Pad Type. The following table describes the differences between the types:

Abbr.	MPIO Pad type	Input buffer	Output buffer	Nominal pull strength	Slew rate control	Drive strength control
ST	Standard	Schmitt / CMOS	Push-Pull	100kΩ	2-bits, up & down	5-bits, up & down
DD	Dual driver	Schmitt / CMOS	Push-Pull / Open-Drain	50kΩ	2-bits, up & down	5-bits, up & down
CZ	Controlled output impedance	Schmitt / CMOS	Push-Pull	15kΩ	2-bits, up & down	7-bits, up & down
OD	Open drain	Schmitt / CMOS	Open-Drain	100kΩ down only	2-bits, down only	5-bits, up only
LV	Low voltage	CMOS (level Shifter)	Push-Pull	5kΩ	4-bits, up & down	5-bits, up & down

For each GPIO pin, the following controls can be changed individually if the function is available for this pad type:

- Output Enable Control: Normal I/O or tristate
- Input Receiver: Enable/Disable input receiver
- Pull-up/down Control: Normal, pull-up, or pull-down
- Open Drain option: Option only available on DD and OD pins
- Alternative Function Selection: Up to 4 special functions are available per pin.

If the following functions are available for this pad type, they can only be set for a whole pad group (power rail block):

- High-Speed Mode (Enable/Disable)
- Schmitt Trigger (Enable/Disable)
- Low Power Mode (LPMD)
- Drive strength control down / up
- Slew rate control falling/rising

4.3 TK1 Function Multiplexing

The NVIDIA Tegra K1 SoC (low-speed) I/O pins can be configured for any of the (and up to) four alternate functions. Theoretically, most of the pins can also be used as GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). Due to the presence of a level shifter at some of the I/O pins, the interface direction is fixed. Therefore, it is not possible to use those pins are real GPIO. They can only be used as General-Purpose Output (GPO) or General-Purpose Input (GPI). See the different types of I/O pins in the previous sections.

For example, the Tegra K1 signal pin on the MXM3 finger pin 118 has the primary function UA3_RXD (Apalis standard function UART1_RXD). The TK1 would allow using the pin also as GPIO3_PU.01. Since the pin features an input level shifter, the GPIO functionality is limited to input. This means it is only possible to use it as UART1_RX and GPI.

The default setting for this pin is the primary function UA3_RXD. It is strongly recommended to, whenever possible, use a pin for a function that is compatible with all Apalis modules. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table listed in chapter 4.5, you will find a list of all pins with alternate functions. There you can see which alternate functions are available for each individual pin.

4.4 Pin Reset Status

After a reset, the Tegra K1 pins can be in different modes. Most of them are tri-stated, pulled up, or pulled low. A few are driven low or high. Please check the table in chapter 4.5 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

For pins with a level shifter, the reset status of the Tegra K1 is only relevant for the output level of the level shifter. The output of the level shifter itself is always driving.

4.5 TK1 Functions List

Below is a list of all the Tegra K1 pins which are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The table contains the information of the I/O Pin Types as well as the MPIO Pad Types. The alternate functions used to provide the primary interfaces to ensure the best compatibility with other Apalis modules are highlighted. Some of the alternate functions might be unusable due to the unidirectional level shifter.

Additional caution is required when using pin 13 (GPIO6). This module edge connector pin is connected to two different Tegra K1 signals, the ball named PEX_L1_CLKREQ_N as well as OWR. Set the unused ball to input (High-Z) when using the other. Make sure that both balls are not driving simultaneously.

Reset Status Description

z:	Tristate
pd:	Pull-Down
pu:	Pull-Up
0:	Drive Low
1:	Drive High

Function Short Forms

CSI:	Camera Serial Interface
DSI:	Display Serial Interface
DTV:	Digital TV input
eDP:	embedded Display Port
HDMI:	High Definition Multimedia Interface
I2C:	Inter-Integrated Circuit
I2S:	Inter IC Sound
LVDS:	Low Voltage Differential Signalling (also known as FPD-Link or FlatLink)
OWR:	One Wire Interface
PEX:	PCI Express
PWM:	Pulse Width Modulation
SATA:	Serial Advanced Technology Attachment
SDMMC:	Secure Card I/O (SD, MMC, CE-ATA, eMMC)
SPDIF:	S/PDIF (Sony-Philips Digital Interface I/O)
SPI:	Serial Peripheral Interface Bus
UART:	Serial Ports (Universal Asynchronous Receiver/Transmitter)
USB:	Universal Serial Bus
VGP:	Video General Purpose IO

X1 Pin	TK1 Ball Name	GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake/ Strap
1	GPIO_PFF2	GPIO3_PFF.02	SATA_DA				wake59
3	DP_HPD	GPIO3_PFF.00	DP_HPD				
5	USB_VBUS_EN0	GPIO3_PN.04	usb_vbus_en0				
7	USB_VBUS_EN1	GPIO3_PN.05	usb_vbus_en1				
11	PEX_L1_RST_N	GPIO3_PDD.05	pe1_rst_l				
13	OWR		OWR				
	PEX_L1_CLKREQ_N	GPIO3_PDD.06	pe1_clkreq_l				
15	PEX_L0_RST_N	GPIO3_PDD.01	pe0_rst_l				
17	PEX_L0_CLKREQ_N	GPIO3_PDD.02	pe0_clkreq_l				
25	SATA_L0_RXP		SATA_L0_RXP				
27	SATA_L0_RXN		SATA_L0_RXN				
31	SATA_L0_TXN		SATA_L0_TXN				
33	SATA_L0_TXP		SATA_L0_TXP				
35	DAP1_DOUT	GPIO3_PN.02	I2S0_SDATA_OUT			SATA_LED_ACTIVE	wake30
37	PEX_WAKE_N	GPIO3_PDD.03	pe_wake_l				wake14
41	PEX_RX4N		PEX_RX4N				
43	PEX_RX4P		PEX_RX4P				
47	PEX_TX4N		PEX_TX4N				
49	PEX_TX4P		PEX_TX4P				
53	PEX_CLK1N		PEX_CLK_OUT_1_N				
55	PEX_CLK1P		PEX_CLK_OUT_1_P				
59	PEX_RX3N		PEX_RX3N				
61	PEX_RX3P		PEX_RX3P				
65	PEX_TX3N		PEX_TX3N				
67	PEX_TX3P		PEX_TX3P				
71	DP_AUX_CH0_N		I2C6_DAT				
73	DP_AUX_CH0_P		I2C6_CLK				
77	DSI_A_D1_N		DSI_A_D1_N				
79	DSI_A_D1_P		DSI_A_D1_P				
83	DSI_A_D0_N		DSI_A_D0_N				
85	DSI_A_D0_P		DSI_A_D0_P				
89	DSI_A_CLK_N		DSI_A_CLK_N				
91	DSI_A_CLK_P		DSI_A_CLK_P				
95	CSI_E_D0_N		CSI_E_D0_N				
97	CSI_E_D0_P		CSI_E_D0_P				
101	DSI_B_D3_N		DSI_B_D3_N				
103	DSI_B_D3_P		DSI_B_D3_P				
107	DSI_B_D2_N		DSI_B_D2_N				
109	DSI_B_D2_P		DSI_B_D2_P				
113	DSI_B_D1_N		DSI_B_D1_N				
115	DSI_B_D1_P		DSI_B_D1_P				
119	DSI_B_D0_N		DSI_B_D0_N				
121	DSI_B_D0_P		DSI_B_D0_P				
125	DSI_B_CLK_N		DSI_B_CLK_N				
127	DSI_B_CLK_P		DSI_B_CLK_P				
131	CSI_E_CLK_N		CSI_E_CLK_N				

X1 Pin	TK1 Ball Name	GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake/ Strap
133	CSI_E_CLK_P		CSI_E_CLK_P				
137	CSI_B_D1_N		CSI_B_D1_N				
139	CSI_B_D1_P		CSI_B_D1_P				
143	CSI_B_D0_N		CSI_B_D0_N				
145	CSI_B_D0_P		CSI_B_D0_P				
149	CSI_A_D1_N		CSI_A_D1_N				
151	CSI_A_D1_P		CSI_A_D1_P				
155	CSI_A_D0_N		CSI_A_D0_N				
157	CSI_A_D0_P		CSI_A_D0_P				
161	CSI_A_CLK_N		CSI_A_CLK_N				
163	CSI_A_CLK_P		CSI_A_CLK_P				
193	CAM_MCLK	GPIO3_PCC.00			vimclk_alt3		
201	CAM_I2C_SDA	GPIO3_PBB.02		I2C3_DAT			wake48
203	CAM_I2C_SCL	GPIO3_PBB.01		I2C3_CLK			wake53
205	DDC_SDA	GPIO3_PV.05	I2C4_DAT				
207	DDC_SCL	GPIO3_PV.04	I2C4_CLK				
209	GEN1_I2C_SDA	GPIO3_PC.05	I2C1_DAT				wake44
211	GEN1_I2C_SCL	GPIO3_PC.04	I2C1_CLK				
215	SPDIF_OUT	GPIO3_PK.05	SPDIF_OUT				
217	SPDIF_IN	GPIO3_PK.06	SPDIF_IN				wake57
221	ULPI_NXT	GPIO3_PY.02	SPI1A_SCK				
223	ULPI_DIR	GPIO3_PY.01	SPI1A_DIN				
225	ULPI_CLK	GPIO3_PY.00	SPI1A_DOUT				
227	ULPI_STP	GPIO3_PY.03	SPI1A_CS0				
229	GPIO_PG7	GPIO3_PG.07				SPI4C_DIN	ram_code3
231	GPIO_PG6	GPIO3_PG.06				SPI4C_DOUT	ram_code2
233	GPIO_PI3	GPIO3_PI.03				SPI4C_CS0	
235	GPIO_PG5	GPIO3_PG.05				SPI4C_SCK	ram_code1
239	GPIO_PU6	GPIO3_PU.06	PM3_PWM3				wake7
2	GPIO_PH0	GPIO3_PH.00	PM3_PWM0	tracedata2		DTV_VALID	
4	GPIO_PH1	GPIO3_PH.01	PM3_PWM1				
6	GPIO_PH2	GPIO3_PH.02	PM3_PWM2				
8	GPIO_PH3	GPIO3_PH.03	PM3_PWM3				
60	USB0_VBUS		USB0_VBUS				
62	PEX_USB3_RX1P		PEX_USB3_RX1P				
64	PEX_USB3_RX1N		PEX_USB3_RX1N				
68	PEX_USB3_TX1P		PEX_USB3_TX1P				
70	PEX_USB3_TX1N		PEX_USB3_TX1N				
72	USB0_ID		USB0_ID				
74	USB0_DP		USB0_DP				
76	USB0_DN		USB0_DN				
80	USB1_DP		USB1_DP				

Toradex
Swiss. Embedded. Computing.

X1 Pin	TK1 Ball Name	GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake/ Strap
82	USB1_DN		USB1_DN				
84	GEN2_I2C_SDA	GPIO3_PT.06	I2C2_DAT				wake47
92	USB3_RX0N		USB3_RX0N				
94	USB3_RX0P		USB3_RX0P				
96	GPIO_PBB0	GPIO3_PBB.00				vimclk2_alt3	
98	USB2_DP		USB2_DP				
100	USB2_DN		USB2_DN				
104	USB3_TX0N		USB3_TX0N				
106	USB3_TX0P		USB3_TX0P				
110	UART3_RTS_N	GPIO3_PC.00	UC3_RTS				
112	GPIO_PU0	GPIO3_PU.00		UA3_TXD			
114	GPIO_PU3	GPIO3_PU.03		UA3_RTS			
116	GPIO_PU2	GPIO3_PU.02		UA3_CTS			
118	GPIO_PU1	GPIO3_PU.01		UA3_RXD			
120	UART3_CTS_N	GPIO3_PA.01	UC3_CTS				wake55
122	GPIO_PK7	GPIO3_PK.07	UD3_RTS				arm_jtag1
124	GPIO_PB1	GPIO3_PB.01	UD3_CTS				
126	UART2_TXD	GPIO3_PC.02	IR3_TXD				
128	UART2_RTS_N	GPIO3_PJ.06		UB3_RTS			
130	UART2_CTS_N	GPIO3_PJ.05		UB3_CTS			
132	UART2_RXD	GPIO3_PC.03	IR3_RXD				
134	UART3_TXD	GPIO3_PW.06	UC3_TXD				
136	UART3_RXD	GPIO3_PW.07	UC3_RXD				
138	GPIO_PJ7	GPIO3_PJ.07	UD3_TXD				arm_jtag0
140	GPIO_PB0	GPIO3_PB.00	UD3_RXD				
144	SDMMC1_DAT2	GPIO3_PY.05	SDMMC1_DAT2				
146	SDMMC1_DAT3	GPIO3_PY.04	SDMMC1_DAT3				
148	CLK2_REQ	GPIO3_PCC.05					
150	SDMMC1_CMD	GPIO3_PZ.01	SDMMC1_CMD				
152	CLK2_OUT	GPIO3_PW.05	extperiph2_clk				
154	SDMMC1_CLK	GPIO3_PZ.00	SDMMC1_CLK				
156	SDMMC3_CLK_LB_IN	GPIO3_PEE.05	SDMMC3_CLK_LB_IN				
158	USB_VBUS_EN2	GPIO3_PFF.01	usb_vbus_en2				
160	SDMMC1_DAT0	GPIO3_PY.07	SDMMC1_DAT0				
162	SDMMC1_DAT1	GPIO3_PY.06	SDMMC1_DAT1				wake13
164	SDMMC1_WP_N	GPIO3_PV.03	SDMMC1_WP_N				
176	SDMMC3_DAT2	GPIO3_PB.05	SDMMC3_DAT2			SPI3D_CS0*	
178	SDMMC3_DAT3	GPIO3_PB.04	SDMMC3_DAT3			SPI3D_CS1*	
180	SDMMC3_CMD	GPIO3_PA.07	SDMMC3_CMD			SPI3D_CS2*	
184	SDMMC3_CLK	GPIO3_PA.06	SDMMC3_CLK			SPI3D_SCK*	
186	SDMMC3_DAT0	GPIO3_PB.07	SDMMC3_DAT0			SPI3D_DIN*	
188	SDMMC3_DAT1	GPIO3_PB.06	SDMMC3_DAT1			SPI3D_DOUT*	wake3
190	SDMMC3_CD_N	GPIO3_PV.02	SDMMC3_CD_N				wake56
194	CLK3_OUT	GPIO3_PEE.00	extperiph3_clk				
196	DAP2_DOUT	GPIO3_PA.05	I2S1_SDATA_OUT				
198	GPIO_PBB3	GPIO3_PBB.03	VGP3				

X1 Pin	TK1 Ball Name	GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake/ Strap
200	DAP2_SCLK	GPIO3_PA.03	I2S1_SCLK				
202	DAP2_DIN	GPIO3_PA.04	I2S1_SDATA_IN				
204	DAP2_FS	GPIO3_PA.02	I2S1_LRCK				
220	HDMI_CEC	GPIO3_PEE.03	CEC				wake52
222	HDMI_TXD2P		HDMI_TXD2P				
224	HDMI_TXD2N		HDMI_TXD2N				
228	HDMI_TXD1P		HDMI_TXD1P				
230	HDMI_TXD1N		HDMI_TXD1N				
232	HDMI_INT	GPIO3_PN.07					wake4
234	HDMI_TXD0P		HDMI_TXD0P				
236	HDMI_TXD0N		HDMI_TXD0N				
240	HDMI_TXCP		HDMI_TXCP				
242	HDMI_TXCN		HDMI_TXCN				
246	LVDS0_TXD4N		LVDS0_TXD4N				
248	LVDS0_TXD4P		LVDS0_TXD4P				
252	LVDS0_TXD0N		LVDS0_TXD0N				
254	LVDS0_TXD0P		LVDS0_TXD0P				
258	LVDS0_TXD1N		LVDS0_TXD1N				
260	LVDS0_TXD1P		LVDS0_TXD1P				
262	GPIO_PBB4	GPIO3_PBB.04	VGP4				
264	LVDS0_TXD2N		LVDS0_TXD2N				
266	LVDS0_TXD2P		LVDS0_TXD2P				
270	LVDS0_TXD3N		LVDS0_TXD3N				
272	LVDS0_TXD3P		LVDS0_TXD3P				
274	GEN2_I2C_SCL	GPIO3_PT.05	I2C2_CLK				
286	GPIO_PBB5	GPIO3_PBB.05	VGP5				

5. Kinetis K20 Companion MCU I/O Pins

The Apalis TK1 features an additional NXP (Freescale) Kinetis K20 microcontroller. The primary purpose of this companion MCU is to extend the following interfaces:

- 2x CAN (FlexCAN)
- 4x ADC inputs
- Resistive touch interface
- Additional GPIOs

These primary interfaces are supported by the standard Linux BSP that comes with the module. The Kinetis Microcontroller features additional interfaces that are available as alternate functions. The software support for these interfaces is very limited. Drivers or firmware might need to be written by the customer. A few examples of such additional interfaces are:

- Additional I2C
- Additional PWM
- Additional ADC inputs
- Additional SD interface
- Additional UART ports
- Additional SPI
- Additional USB 1.1 interface
- Timer interface
- Capacitive touch buttons

The communication between the Tegra K1 SoC and the K20 companion MCU takes place over an SPI interface. The Tegra K1 is the SPI master. In addition to the K20 SPI slave input, the SPI interface between the two controllers is also connected to the EzPort of the K20 for flashing the MCU firmware. To set the K20 into programming mode, the Tegra K1 will need to drive the reset of the K20.

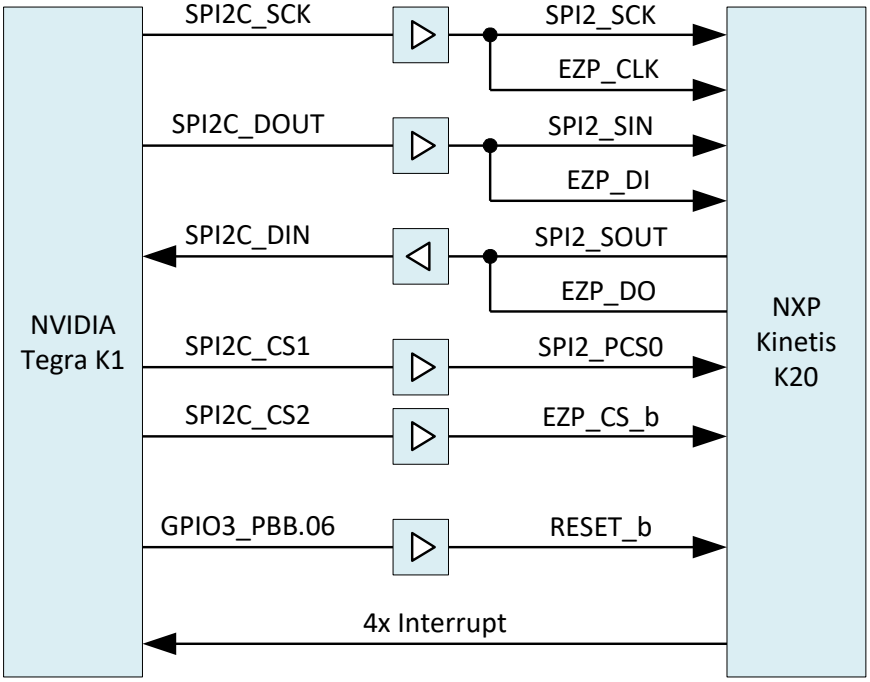


Figure 5: Connections between SoC and MCU

Table 5-1 Interface Signals between SoC and MCU

TK1 Ball Name	TK1 Function	K20 Function	K20 Ball Name	Description
GPIO_X4_AUD	SPI2C_DOUT	SPI2_SIN	PTB23	SPI MOSI for communication
		EZP_DI	**PTA1**	The programming data input of MCU
GPIO_X5_AUD	SPI2C_SCK	SPI2_SCK	PTB21	SPI CLK for communication
		EZP_CLK	**PTA0**	The programming clock input of MCU
GPIO_X7_AUD	SPI2C_DIN	SPI2_SOUT	PTB22	SPI MISO for communication
		EZP_DO	**PTA2**	The programming data output of MCU
GPIO_X6_AUD	SPI2C_CS1	SPI2_PCS0	PTB20	SPI CS for communication
GPIO_W2_AUD	SPI2C_CS2	EZP_CS_b	PTA4	Chip select for programming the MCU
GPIO_PBB6	GPIO3_PBB.06	**RESET_b**	**RESET_b**	Reset input of K20. K20 also features a power-on Reset.
GPIO_PK2	GPIO3_PK.02	PTA16	PTA16	MCU interrupt output 1 (no level shifter!)
GPIO_PJ2	GPIO3_PJ.02	PTA29	PTA29	MCU interrupt output 2 (no level shifter!)
GPIO_PI5	GPIO3_PI.05	PTB8	PTB8	MCU interrupt output 3 (no level shifter!)
GPIO_PJ0	GPIO3_PJ.00	PTE26	PTE26	MCU interrupt output 4 (no level shifter!)

There are four interrupt lines from the K20 MCU to the TK1 SoC. There is no level shifter between the two controllers. The SoC pins are only 1.8V capable, while all K20 pins do have a 3.3V logic level. Therefore, it is crucial to configure the interrupt pins correctly on both sides. The MCU's interrupt output pins need to be configured as open-drain output without enabling the internal pull-up resistors. The pull-up resistors need to be enabled at the SoC input since they pull up the signal to just 1.8V.

5.1 K20 Pin Control

Most of the K20 pins can be configured to any of up to eight alternate functions. Most pins can also be used as regular GPIOs. All K20 pins are 3.3V logic level. Therefore, no level shifters are needed. This means that there are no limitations for using the pins as GPIO as with the level-shifted TK1 signals.

For each regular K20 pin, the following controls can be changed individually:

- Pin mux control (selecting the alternate function)
- Interrupt configuration
- DMA configuration
- Drive strength
- Open-drain mode
- Passive filter (low pass filter for signals below 2MHz)
- Slew rate
- Pull-up or -down resistor enabling

5.2 K20 Functions List

The following list contains all K20 MCU pins which are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The alternate functions used to provide the primary interfaces to ensure the best compatibility with other Apalis modules are highlighted. Please be aware that the standard Linux BSP supports not all listed functions. For using these functions, additional firmware or drivers may need to be developed.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

Function Short Forms

ADC:	Analogue to Digital Converter
CAN:	Controller Area Network
CMP:	Comparator
EWM:	External Watchdog Monitor
FB:	FlexBus, external bus
FTM:	FlexTimer, a general-purpose timer, can be used as PWM output
I2C:	Inter-Integrated Circuit
I2S:	Inter IC Sound
PDB:	Programmable Delay Block
PTx:	General Purpose IO (GPIO)
SDHC:	Secure Digital Memory Card High Capacity (SD, MMC, CE-ATA, eMMC)
SPI:	Serial Peripheral Interface Bus
TSI:	Touch Sense Input
UART:	Serial Ports (Universal Asynchronous Receiver/Transmitter)
USB:	Universal Serial Bus

Toradex
Swiss. Embedded. Computing.

X1 Pin	K20 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	AL
12	K20_PTA13/ LLWU_P4	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1			I2S
14	K20_PTA12	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S
16	K20_PTC16		PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	
18	K20_PTC17		PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	
86	K20_USB0_DP	USB0_DP						
88	K20_USB0_DM	USB0_DM						
173	K20_PTE1/ LLWU_P0	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C
175	K20_PTE0	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C
177	K20_PTB17	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EW
179	K20_PTE3	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD		
181	K20_PTE5		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		
183	K20_PTE24	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EW
185	K20_PTE4/ LLWU_P2		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3		
187	K20_PTA17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S
191	K20_PTE25	ADC0_SE18	PTE25	CAN1_RX	UART4_RX			EW
195	K20_PTA5		PTA5	USB_CLKIN	FTM0_CH2		CMP2_OUT	I2S
197	K20_PTA3	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0			
243	K20_PTD7		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FT
245	K20_PTD5	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5	FB_AD1	EW
247	K20_PTD4/ LLWU_P14		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EW
249	K20_PTC4/ LLWU_P8		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CM
251	K20_PTD9		PTD9	I2C0_SDA	UART5_TX			FB
253	K20_PTD8		PTD8	I2C0_SCL	UART5_RX			FB
255	K20_PTD6/ LLWU_P15	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FT
257	K20_PTD3		PTD3	SPI0_SIN	UART2_TX		FB_AD3	
259	K20_PTC7	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8	
261	K20_PTC3/ LLWU_P7	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S
263	K20_PTC0	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	I2S
265	K20_PTB16	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EW
269	K20_PTD12		PTD12	SPI2_SCK		SDHC0_D4		FB
271	K20_PTD11		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB
273	K20_PTD2/ LLWU_P13		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX		FB_AD4	

Toradex
Swiss. Embedded. Computing.

X1 Pin	K20 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	AL
275	K20_PTC6/ LLWU_P10	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S
277	K20_PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S
279	K20_PTB19	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTA
281	K20_PTB11	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTA
283	K20_PTD14		PTD14	SPI2_SIN		SDHC0_D6		FB
287	K20_PTD13		PTD13	SPI2_SOUT		SDHC0_D5		FB
289	K20_PTD1	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b	
291	K20_PTD0/ LLWU_P12		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b	
293	K20_PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S
295	K20_PTB18	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTA
297	K20_PTB10	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTA
299	K20_PTD15		PTD15	SPI2_PCS1		SDHC0_D7		FB
301	K20_PTE2/ LLWU_P1	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK		
305	K20_PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTA
307	K20_PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTA
309	K20_PTB2	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTA
311	K20_PTB3	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_b			FTA
315	K20_PTB6	ADC1_SE12	PTB6				FB_AD23	
317	K20_PTB7	ADC1_SE13	PTB7				FB_AD22	
319	K20_PTC8	ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK	FB_AD7	
321	K20_PTC9	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTA

6. Interface Description

6.1 Power Signals

6.1.1 Digital Supply

Table 6-1 Digital Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	3.3V main power supply	Use decoupling capacitors on all pins.
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	Digital Ground	
174	VCC_BACKUP	I/O	RTC Power supply can be connected to a backup battery.	It can be left unconnected if the internal RTC is not used.

6.1.2 Analogue Supply

Table 6-2 Analogue Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
314, 320	AVCC	I	3.3V Analogue supply	Connect this pin to a 3.3V supply. For better audio accuracy, we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the VCC 3.3V input supply.
303, 313, 304, 308	AGND	I	Analogue Ground	Connect this pin to GND. For better audio accuracy, we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis TK1.

6.1.3 Power Management Signals

Table 6-3 Power Management Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
28	RESET_MICO#	I	Reset Input	This pin is low active and resets the Apalis module. This pin is connected to the power manager IC. There is a 100k pull-up resistor on the module.
26	RESET_MOCI#	O	Reset Output	This pin is active low. This pin is driven low at boot up. This is an open-drain signal with a 10k pull-up resistor on the module.
24	POWER_ENABLE_MOCI	O	Signal for the carrier board to enable the peripheral voltage rails	More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide

6.2 GPIOs

The Apalis form factor features eight dedicated general-purpose input-output (GPIO) pins. Besides these 8 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the eight dedicated GPIOs first.

Since some of the Tegra K1 signal pins feature a unidirectional level shifter, these pins can only be used as general-purpose input or output but not as regular GPIO. Other pins are provided by the companion MCU instead of the main SoC. Therefore, it is essential to check the type of pin before selecting it as GPIO. More information can be found in sections 4 and 5.

Table 6-4 Dedicated GPIO signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
1	GPIO1	GPIO_PFF2	GPIO3_PFF.02	I/O	
3	GPIO2	DP_HPD	GPIO3_PFF.00	I/O	
5	GPIO3	USB_VBUS_EN0	GPIO3_PN.04	I/O	
7	GPIO4	USB_VBUS_EN1	GPIO3_PN.05	I/O	
11	GPIO5	PEX_L1_RST_N	GPIO3_PDD.05	I/O	
13	GPIO6	PEX_L1_CLKREQ_N	GPIO3_PDD.06	I/O	Second SoC ball connected to this MXM3 pin
15	GPIO7	PEX_L0_RST_N	GPIO3_PDD.01	I/O	
17	GPIO8	PEX_L0_CLKREQ_N	GPIO3_PDD.02	I/O	

6.2.1 Wakeup Source

Several Tegra K1 pins can be used to wake up the Apalis module from a suspended state. In the Apalis module standard, pin 37 is the default wakeup source. Only this pin is guaranteed to be wakeup compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules.

Table 6-5 TK1 Wake-up Sources

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 GPIO Name	Wake Source
37	WAKE1_MICO	PEX_WAKE_N	GPIO3_PDD.03	wake14
1	GPIO1	GPIO_PFF2	GPIO3_PFF.02	wake59
35	SATA1_ACT#	DAP1_DOUT	GPIO3_PN.02	wake30
120	UART1_DSR	UART3_CTS_N	GPIO3_PA.01	wake55
162	MMC1_D1	SDMMC1_DAT1	GPIO3_PY.06	wake13
188	SD1_D1	SDMMC3_DAT1	GPIO3_PB.06	wake3
201	I2C3_SDA (CAM)	CAM_I2C_SDA	GPIO3_PBB.02	wake48
203	I2C3_SCL (CAM)	CAM_I2C_SCL	GPIO3_PBB.01	wake53
209	I2C1_SDA	GEN1_I2C_SDA	GPIO3_PC.05	wake44
217	SPDIF1_IN	SPDIF_IN	GPIO3_PK.06	wake57
220	HDMI1_CEC	HDMI_CEC	GPIO3_PEE.03	wake52
232	HDMI1_HPD	HDMI_INT	GPIO3_PN.07	wake4
239	BKL1_PWM	GPIO_PU6	GPIO3_PU.06	wake7

The wake signal of the Ethernet controller (pin 16, PE_WAKE_N) is connected to the ULPI_DATA4 ball of the TK1 (GPIO3_PO.05). This pin features wake source "wake0" and allow the Ethernet controller to wake up the Tegra K1.

6.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC/PHY is integrated on the module. Therefore only the magnetics are required on the carrier board. The Intel I210-AT Gigabit Ethernet Controller chip is connected over the PCIe port 1 (lane 2) of the Tegra K1. The Ethernet controller supports IEEE1588 and IEEE802.1AS time synchronization. There are up to three externally available pins available that can be used for the time synchronization.

Table 6-6 Ethernet Pins

X1 Pin #	Apalis Signal Name	I210-AT Signal Name	I/O	Description	Remarks
50	ETH1_MDI0+	MDI_0_P	I/O	Media Dependent Interface	100BASE-TX: Transmit +
48	ETH1_MDI0-	MDI_0_N	I/O	Media Dependent Interface	100BASE-TX: Transmit -
56	ETH1_MDI1+	MDI_1_P	I/O	Media Dependent Interface	100BASE-TX: Receive +
54	ETH1_MDI1-	MDI_1_N	I/O	Media Dependent Interface	100BASE-TX: Receive -
32	ETH1_MDI2+	MDI_2_P	I/O	Media Dependent Interface	100BASE-TX: Unused
34	ETH1_MDI2-	MDI_2_N	I/O	Media Dependent Interface	100BASE-TX: Unused
38	ETH1_MDI3+	MDI_3_P	I/O	Media Dependent Interface	100BASE-TX: Unused
40	ETH1_MDI3-	MDI_3_N	I/O	Media Dependent Interface	100BASE-TX: Unused
46	ETH+_CTREF	NC	O	Center tap supply	I210 does not need a center tap supply
42	ETH1_ACT	LED1	O	LED indication output	The mode can be configured individually
44	ETH1_LINK	LED2	O	LED indication output	The mode can be configured individually
99	TS_3	SDP0	I/O	Software-defined pin 0	The SDP can be individually configured to act as either standard input, General-Purpose Interrupt input, or output pin. Can be used for IEEE1588 time synchronization to auxiliary devices.
123	TS_4	SDP1	I/O	Software-defined pin 1	
135	TS_5	SDP2	I/O	Software-defined pin 2	

The Intel I210-AT does not require a central tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the magnetics center tap to pin 46 of the Apalis module. This guarantees the full compatibility to Apalis modules, which require a center tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only two lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

6.4 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.0 SuperSpeed (backward compatible), and two USB 2.0 High-Speed interfaces. The NVIDIA Tegra K1features only two USB 3.0 SuperSpeed (5Gbit/s) and one USB 2.0 High-Speed (480 Mbit/s) interfaces with an integrated physical layer. Therefore, USB_H3 cannot be provided by the TK1 SoC. The USBO1 is used for the USB recovery mode. See section 7 "Recovery Mode" for more information.

The USB 3.0 SuperSpeed feature of the USBO port can only be used in the host mode. In client mode, the OTG port supports only USB 2.0 High-Speed. Both USB 3.0 ports (USBO and USBH4) share one SuperSpeed Bus Instance. The 5Gb/s bandwidth is distributed across these ports.

The TK1 SoC does not provide the USB_H3 port of the Apalis module edge connector. It is provided by the Kinetis companion MCU, which communicates over SPI with the SoC. The K20 MCU follows the USB 2.0 specifications but is only Full Speed (12Mbit/s) and Low-Speed (1.5Mbit/s) capable. This limitation is colloquially called "limited to USB 1.1". The standard Toradex Linux BSP does not include K20 firmware and drivers for using this port.

6.4.1 USB Data Signal

Table 6-7 USBO1 Data Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
74	USBO1_D+	USB0_DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB0_DN	I/O	Negative Differential USB Signal, OTG capable
62	USBO1_SSRX+	PEX_USB3_RX1P	I	Positive differential receiving signal for USB3.0
64	USBO1_SSRX-	PEX_USB3_RX1N	I	Negative differential receiving signal for USB3.0
68	USBO1_SSTX+	PEX_USB3_TX1P	O	Positive differential transmission signal for USB3.0
70	USBO1_SSTX-	PEX_USB3_TX1N	O	Negative differential transmission signal for USB3.0

Table 6-8 USBH2 Data Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
80	USBH2_D+	USB1_DP	I/O	Positive Differential USB Signal
82	USBH2_D-	USB1_DN	I/O	Negative Differential USB Signal

Table 6-9 USBH3 Data Pins (K20 companion MCU)

X1 Pin#	Apalis Signal Name	K20 Ball Name	I/O	Description
86	USBH3_D+	USB0_DP	I/O	Positive Differential USB Signal, Interface of K20 companion MCU
88	USBH3_D-	USB0_DM	I/O	Negative Differential USB Signal, Interface of K20 companion MCU

Table 6-10 USBH4 Data Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
98	USBH4_D+	USB2_DP	I/O	Positive Differential USB Signal
100	USBH4_D-	USB2_DN	I/O	Negative Differential USB Signal
94	USBH4_SSRX+	USB3_RX0P	I	Positive differential receiving host signal for USB3.0
92	USBH4_SSRX-	USB3_RX0N	I	Negative differential receiving host signal for USB3.0
106	USBH4_SSTX+	USB3_TX0P	O	Positive differential transmission host signal for USB3.0
104	USBH4_SSTX-	USB3_TX0N	O	Negative differential transmission host signal for USB3.0

6.4.2 USB Control Signals

Table 6-11 USB OTG Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
72	USBO1_ID	USB0_ID	USB0_ID	I	Use this pin to detect the ID pin if you use USB OTG.
60	USBO1_VBUS	USB0_VBUS	USB0_VBUS	I	Use this pin to detect if VBUS is present.

If you use the USB Host function, you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis TK1 provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. However, if required, you can use other GPIOs or not use them at all. The USBH2, USBH3, and USBH4 interfaces share the bus power control signals, whereas USBO1 has its dedicated control signals.

Table 6-12 USB Power Control Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
274	USBO1_EN	GEN2_I2C_SCL	GPIO3_PT.05	O	This pin enables the external USB voltage supply for the USBO1 interface. A regular GPIO provides the function. There is an output level shifter on the module.
262	USBO1_OC#	GPIO_PBB4	GPIO3_PBB.04	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBO1 interface. The pin features an input level shifter on the module
84	USBH_EN	GEN2_I2C_SDA	GPIO3_PT.06	O	This pin enables the external USB voltage supply for the USBH2, USBH3, and USBH4 interfaces. A regular GPIO provides the function. There is an output level shifter on the module.
96	USBH_OC#	GPIO_PBB0	GPIO3_PBB.00	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBH2, USBH3, and USBH4 interfaces. The pin features an input level shifter on the module

The USBO1_OC# and USBH_OC# pins are level shifted on the module. Therefore, it is recommended to add pull-up or pull-down resistors to the non-used input pins to ensure they are not floating. See also section 4.1.5. The USBO1_EN and USBH_EN pins are featuring output level shifter and can be left floating if not used.

6.5 Display

The display controller subsystem of the Tegra K1 features two independent display controllers that support HDMI, LVDS, DSI, and eDP. The controller can support two independent display devices. Each display controller can run at different clock rates and drive different resolution panels.

6.5.1 Parallel RGB LCD interface

The Apalis TK1 does not feature a parallel RGB LCD interface. The K20 MCU pins located on the dedicated module edge pins do not feature any LCD interface. Nevertheless, it is possible to implement an LVDS or DSI to RGB converter on the carrier board to attach such a display.

6.5.2 LVDS

The LVDS interface (official name: FPD-Link/FlatLink) serializes the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to 7 parallel signals. For an 18-bit

RGB interface, including the control signals (Display Enable, Vertical, and Horizontal Synch), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional color bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two color mapping standards for the 24-bit interface. The less common "24-bit / 18-bit compatible" (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each color into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit color mapping standard (VESA format, Intel 24.1 LVDS data format) serializes each color's two most significant bits into the fourth LVDS pair. This mode is not backward compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this color mapping. The LVDS interface of Apalis TK1 is configurable to support different color mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of color mappings.

Figure 6 shows the LVDS output signals for the "24-bit /18-bit Compatible Color Mapping" (JEIDA format, Intel 24.0 LVDS data format). In order to enable this mode, the DOTDAT[2:0] needs to be set to 0 in the SOR_NV_PDISP_SOR_CSTM_0 register.

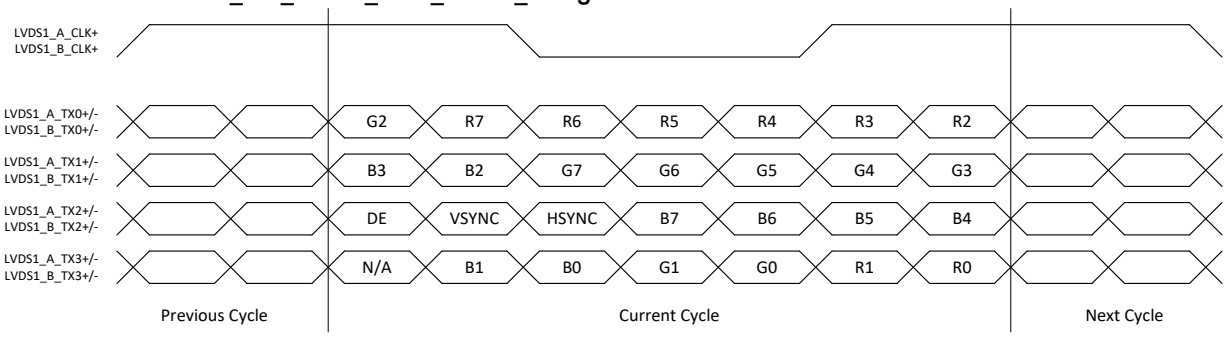


Figure 6: 24-bit / 18-bit Compatible Color Mapping (Intel 24.0 LVDS Data Format)

Figure 7 shows the LVDS output signals for the common 24-bit color mapping (VESA format, Intel 24.1 LVDS data format). To enable this mode the DOTDAT[2:0] needs to be set to 6 in the SOR_NV_PDISP_SOR_CSTM_0 register.

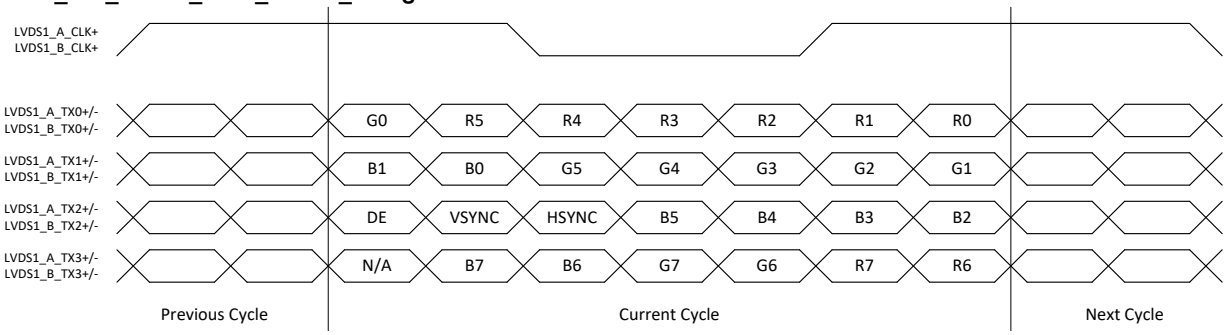


Figure 7: Common 24-bit VESA Color Mapping (Intel 24.1 LVDS Data Format)

Figure 8 shows the LVDS output signals for the 18-bit interface.

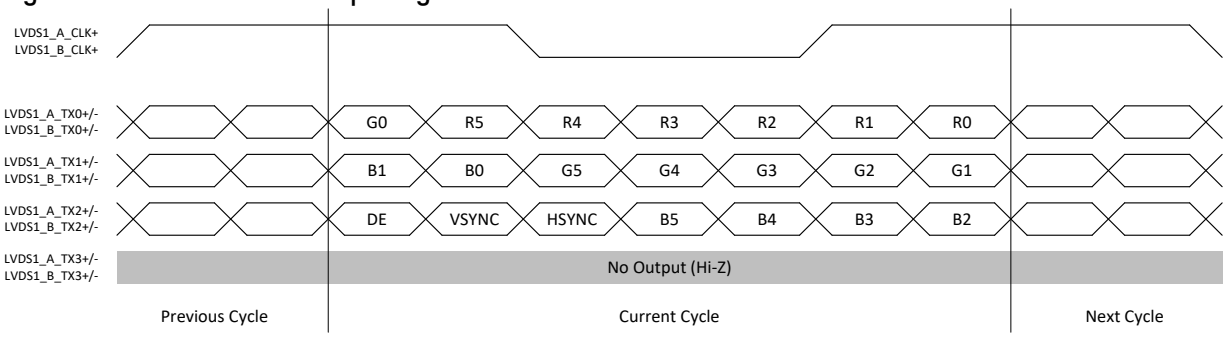


Figure 8: 18-bit Mode

The NVIDIA Tegra K1 features only single-channel LVDS; dual-channel is not supported. The interface features a maximum pixel clock frequency of 165MHz and can be used for display panels up to 1920x1200 pixels @60Hz. Most of the displays above 1366x768 pixels @60 usually interface with dual-channel LVDS. Some displays allow changing to single-channel mode. If the display does not support it, a single-to-dual-channel circuit on the carrier board is needed.

Table 6-13 LVDS interface signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
248	LVDS1_A_CLK+	LVDS0_TXD4P	O	LVDS Clock out for channel A
246	LVDS1_A_CLK-	LVDS0_TXD4N	O	
254	LVDS1_A_TX0+	LVDS0_TXD0P	O	LVDS data lane 0 for channel A
252	LVDS1_A_TX0-	LVDS0_TXD0N	O	
260	LVDS1_A_TX1+	LVDS0_TXD1P	O	LVDS data lane 1 for channel A
258	LVDS1_A_TX1-	LVDS0_TXD1N	O	
266	LVDS1_A_TX2+	LVDS0_TXD2P	O	LVDS data lane 2 for channel A
264	LVDS1_A_TX2-	LVDS0_TXD2N	O	
272	LVDS1_A_TX3+	LVDS0_TXD3P	O	LVDS data lane 3 for channel A (unused for 18bit)
270	LVDS1_A_TX3-	LVDS0_TXD3N	O	
278	LVDS1_B_CLK+		O	LVDS Clock out for channel B (Not available)
276	LVDS1_B_CLK-		O	
284	LVDS1_B_TX0+		O	LVDS data lane 0 for channel B (Not available)
282	LVDS1_B_TX0-		O	
290	LVDS1_B_TX1+		O	LVDS data lane 1 for channel B (Not available)
288	LVDS1_B_TX1-		O	
296	LVDS1_B_TX2+		O	LVDS data lane 2 for channel B (Not available)
294	LVDS1_B_TX2-		O	
302	LVDS1_B_TX3+		O	LVDS data lane 3 for channel B (Not available)
300	LVDS1_B_TX3-		O	

Table 6-14 Additional Display Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
239	BKL1_PWM	GPIO_PU6	PM3_PWM3	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	GPIO_PBB5	GPIO3_PBB.05	O	Enable signal for the backlight
205	I2C2_SDA (DDC)	DDC_SDA	I2C4_DAT	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL (DDC)	DDC_SCL	I2C4_CLK	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

6.5.3 HDMI

HDMI provides a unified method of transferring video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

Features

- HDMI 1.4b up to 4096x2160@24Hz, 3840x2160@30Hz, or 1920x1080@120Hz (3D)
- Pixel Clock from 25.2MHz up to 300MHz
- Supports digital sound
- High-bandwidth Content Protection (HDCP, separate license needed)
- CEC interface

Table 6-15 HDMI Interface Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
240	HDMI1_TXC+	HDMI_TXCP	O	HDMI Differential Clock
242	HDMI1_TXC-	HDMI_TXCN	O	
234	HDMI1_TXD0+	HDMI_TXD0P	O	HDMI Differential Data
236	HDMI1_TXD0-	HDMI_TXD0N	O	
228	HDMI1_TXD1+	HDMI_TXD1P	O	HDMI Differential Data
230	HDMI1_TXD1-	HDMI_TXD1N	O	
222	HDMI1_TXD2+	HDMI_TXD2P	O	HDMI Differential Data
224	HDMI1_TXD2-	HDMI_TXD2N	O	

Table 6-16 Additional Display Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
220	HDMI1_CEC	HDMI_CEC	CEC	I/O	HDMI Consumer Electronics Control.
232	HDMI1_HPD	HDMI_INT	GPIO3_PN.07	I	Hot Plug Detect
205	I2C2_SDA (DDC)	DDC_SDA	I2C4_DAT	I/O	Display Data Channel, shared with the other display interfaces
207	I2C2_SCL (DDC)	DDC_SCL	I2C4_CLK	O	Display Data Channel, shared with the other display interfaces

6.5.4 Analog VGA

The Apalis TK1 does not feature an analog VGA interface.

6.5.5 Embedded Display Port (eDP)

The LVDS interface pins of the Tegra K1 can be configured to be used as an embedded Display Port interface. The eDP interface can be used for driving local displays, but not external Display Port (DP) monitors. The interface is not compatible with the Display Port standard for external displays.

Since the eDP interface is not part of the Apalis module specifications, it is not guaranteed that other Apalis modules also can use the LVDS interface pins as eDP. Use this interface only if compatibility with other modules is not mandatory.

The eDP requires additional 10nF series capacitors to be placed in the data lines and the AUX channel. If the port is used as an LVDS interface, the capacitors are not allowed. Filters (for example, common-mode chokes) are not recommended. Be aware of the different numbering of the data lanes if the LVDS interface is used as an eDP port.

Features:

- 1, 2, and 4 lanes supported
- RBR, HBR, and HBR2 supported
- 18- or 24-bit color depth
- Pixel clock up to 450MHz
- Up to 3200x2000@60Hz (software limited for embedded devices)

The eDP signals are located as a secondary function of the LVDS interface. Therefore, other Apalis modules will be compatible with this interface. The routing requirements of the eDP signals are different from the LVDS interface.

Table 6-17 eDP Signal Routing Requirements

Parameter	Requirement
Max Frequency	1.62 Gb/s per lane (RBR) 2.7 Gb/s per lane (HBR) 5.4 Gb/s per lane (HBR2)
Configuration/Device Organization	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between different data pairs	<150ps ≈22.5mm
Max Trace Length from Module Connector	215mm (RBR and HBR) 127mm (HBR2)

The Apalis TK1 supports up to 4 lanes of embedded Display Port signals. The interface is backward compatible with one or two-lane displays. Simply use only lane 0 for a single lane display, respectively, lane 0 and 1 for a two-lane display. The eDP requires a different voltage level of the AVD_LVDS0_PLL rail. The PMIC on the module allows switching between 1.8V for LVDS (default) and 3.3V for eDP. Make sure the voltage is set correctly.

Table 6-18 eDP interface signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	eDP Signal Name	I/O	Description
266	LVDS1_A_TX2+	LVDS0_TXD2P	eDP_1_D0+	O	Link Lane 0
264	LVDS1_A_TX2-	LVDS0_TXD2N	eDP_1_D0-	O	
260	LVDS1_A_TX1+	LVDS0_TXD1P	eDP_1_D1+	O	Link Lane 1
258	LVDS1_A_TX1-	LVDS0_TXD1N	eDP_1_D1-	O	
254	LVDS1_A_TX0+	LVDS0_TXD0P	eDP_1_D2+	O	Link Lane 2
252	LVDS1_A_TX0-	LVDS0_TXD0N	eDP_1_D2-	O	
248	LVDS1_A_CLK+	LVDS0_TXD4P	eDP_1_D3+	O	Link Lane 3
246	LVDS1_A_CLK-	LVDS0_TXD4N	eDP_1_D3-	O	
73	TS_DIFF3+	DP_AUX_CH0_P	eDP_1_AUX_CH0_P	I/O	Aux channel contains control data such as EDID information
71	TS_DIFF3-	DP_AUX_CH0_N	eDP_1_AUX_CH0_N	I/O	
3	GPIO2	DP_HPD	eDP_1_HPD	I	Hot-plug detect

6.5.6 Display Serial Interface (DSI)

The Tegra K1 SoC supports two MIPI DSI interfaces to connect compatible displays. One port can be used with up to four data lanes, while the other is limited to a maximum of two lanes since not all signals are located on the module edge connector needed for quad lane mode. Each data lane is capable of up to 1.5Gbps data rate. Lane 1 of the interface is bidirectional (high-speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer. The maximum supported resolution is 2560x1440@60Hz.

The DSI signals are located in the type-specific area of the Apalis module. Therefore, it is not guaranteed that other Apalis modules will be compatible with this interface. If you plan on using the DSI interface, please be aware that other Apalis modules might not be compatible with your carrier board.

As the DSI is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Apalis Carrier Board Design Guide as the interface is type-specific.

Table 6-19 DSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 6-20 DSI interface signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	DSI Signal Name	I/O	Description
127	TS_DIFF12+	DSI_B_CLK_P	DSI1_CLK+	O	DSI Interface 1 clock
125	TS_DIFF12-	DSI_B_CLK_N	DSI1_CLK-	O	
121	TS_DIFF11+	DSI_B_D0_P	DSI1_D1+	I/O	DSI Interface 1 data lane 1
119	TS_DIFF11-	DSI_B_D0_N	DSI1_D1-	I/O	
115	TS_DIFF10+	DSI_B_D1_P	DSI1_D2+	O	DSI Interface 1 data lane 2
113	TS_DIFF10-	DSI_B_D1_N	DSI1_D2-	O	
109	TS_DIFF9+	DSI_B_D2_P	DSI1_D3+	O	DSI Interface 1 data lane 3
107	TS_DIFF9-	DSI_B_D2_N	DSI1_D3-	O	
103	TS_DIFF8+	DSI_B_D3_P	DSI1_D4+	O	DSI Interface 1 data lane 4
101	TS_DIFF8-	DSI_B_D3_N	DSI1_D4-	O	
91	TS_DIFF6+	DSI_A_CLK_P	DSI2_CLK+	O	DSI Interface 2 clock
89	TS_DIFF6-	DSI_A_CLK_N	DSI2_CLK-	O	
85	TS_DIFF5+	DSI_A_D0_P	DSI2_D1+	I/O	DSI Interface 2 data lane 1
83	TS_DIFF5-	DSI_A_D0_N	DSI2_D1-	I/O	
79	TS_DIFF4+	DSI_A_D1_P	DSI2_D2+	O	DSI Interface 2 data lane 2
77	TS_DIFF4-	DSI_A_D1_N	DSI2_D2-	O	

Table 6-21 Additional Display Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
239	BKL1_PWM	GPIO_PU6	PM3_PWM3	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	GPIO_PBB5	GPIO3_PBB.05	O	Enable signal for the backlight
205	I2C2_SDA (DDC)	DDC_SDA	I2C4_DAT	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL (DDC)	DDC_SCL	I2C4_CLK	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

6.6 PCI Express

The Tegra K1SoC features two PCI Express (PCIe) interfaces. One interface is available externally on the module edge connector. It is possible to use the interface with a maximum of two lanes. The other interface is used on the module for the Ethernet controller. Since it is possible to map the PCIe signals in different ways, it is also alternatively possible to use the second PCIe port externally as alternate functions of the USB 3.0 SuperSpeed signals of the USB_H4 port. The following table shows all possible PCIe signal mappings.

Table 6-22 PCIe mapping options

Use Case	Lane 0 USB3	Lane 1 PEX1_USB3	Lane 2 PEX2	Lane 3 PEX3	Lane 4 PEX4	SATA
Default	USB_H4	USB_O1	Ethernet	NA	PCIE_1	SATA_1
1	USB_H4	USB_O1	Ethernet	PCIE_1 L1	PCIE_1 L0	SATA_1
3	PCIE_2	USB_O1	NA	PCIE_1 L1	PCIE_1 L0	SATA_1
4	PCIE_2	NA	NA	PCIE_1 L1	PCIE_1 L0	USB_O1

The PCIe interface is compliant with the PCIe 2.0 specification and supports a 5 Gb/s data rate. It is backward compatible with the PCIe 1.1 standard, which supports 2.5 Gb/s. PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 6-23 PCIe Interface Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	PCIe Signal Name	I/O	Description
55	PCIE1_CLK+	PEX_CLK1P	PCIE1_CLK+		Reference clock differential pair
53	PCIE1_CLK-	PEX_CLK1N	PCIE1_CLK-		
49	PCIE1_TX+	PEX_TX4P	PCIE1_L0_TX+		Transmit data lane 0
47	PCIE1_TX-	PEX_TX4N	PCIE1_L0_TX-		
43	PCIE1_RX+	PEX_RX4P	PCIE1_L0_RX+		Receive data lane 0
41	PCIE1_RX-	PEX_RX4N	PCIE1_L0_RX-		
67	TS_DIFF2+	PEX_TX3P	PCIE1_L1_TX+		Transmit data lane 1, incompatible with other modules
65	TS_DIFF2-	PEX_TX3N	PCIE1_L1_TX-		
61	TS_DIFF1+	PEX_RX3P	PCIE1_L1_RX+		Receive data lane 1, incompatible with other modules
59	TS_DIFF1-	PEX_RX3N	PCIE1_L1_RX-		
106	USBH4_SSTX+	USB3_TX0P	PCIE2_L0_TX+		Transmit data, only available if Ethernet is unused, incompatible with other modules
104	USBH4_SSTX-	USB3_TX0N	PCIE2_L0_TX-		
94	USBH4_SSRX+	USB3_RX0P	PCIE2_L0_RX+		Receive data, only available if Ethernet is unused, incompatible with other modules
92	USBH4_SSRX-	USB3_RX0N	PCIE2_L0_RX-		

The second interface is only usable if the on-module Ethernet controller is not in use and does not feature a dedicated reference clock output. Use a zero-delay clock distributor to generate a copy of the reference clock of the first Ethernet port (Pin 55/53).

Table 6-24 Additional PCIe Control Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
37	WAKE1_MICO	PEX_WAKE_N	pe_wake_l	I	General-purpose wake signal
26	RESET_MOCI#			O	General reset output
209	I2C1_SDA	GEN1_I2C_SDA	I2C1_DAT	I/O	Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if the interface is necessary
211	I2C1_SCL	GEN1_I2C_SCL	I2C1_CLK	O	

6.7 SATA

The Serial ATA (SATA) interface can be used to attach, for example, an external hard drive, SSD, or an mSATA SSD. The interface is a single Gen 2 SATA link with a maximum transfer rate of 3 Gb/s. The interface is backward compatible with Gen 1 (1.5Gb/s). SATA is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 6-25 Apalis standard SATA Interface Signals (x1)

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
33	SATA1_TX+	SATA_L0_TXP	O	SATA transmit data Series decoupling capacitors are provided on the module
31	SATA1_TX-	SATA_L0_TXN	O	
25	SATA1_RX+	SATA_L0_RXP	I	SATA receive data Series decoupling capacitors are provided on the module
27	SATA1_RX-	SATA_L0_RXN	I	
35	SATA1_ACT#	DAP1_DOUT	O	SATA activity indicator

6.8 I²C

The NVIDIA Tegra K1 offers up to six I²C controllers. They implement the I²C V3.0 specification. All of them can be used in either master or slave mode. The port I2C5 is used for power management and is not available externally. Port I2C1 is known as general-purpose I²C on the module connector. Port I2C4 is intended to be used as a DDC interface for the displays, while port I2C3 is intended to be used in combination with the camera interface. Both I2C interfaces can also be used for other general-purpose.

One of the additional two I²C interfaces of the K1 SoC is available as an alternate function. The primary purpose of this port (I2C6) is to use it as an embedded display port aux channel. Due to the output level shifter, the I2C2 interface cannot be used externally.

The TK1 I²C ports Features:

- Supports standard and fast mode of operation (0-400KHz), Fm+ (1Mbit/s), as well as high-speed mode (3.4 MHz).
- Independent Master Controller and Slave Controller
- Master supports clock stretching by the slave
- Supports one to eight-bytes burst data transfers
- 7-bit or 10-bit addressing
- Fully programmable 7-bit or 10-bit address for the slave
- Supports general call addressing
- Supports Recognition and Transfer of data to peripherals that do not send an acknowledgment
- Master supports packet-based DMA
- Supports 4kByte of transfer in packet mode (can be extended by using multiple packets)

Table 6-26 I²C Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I2C Port	Description
209	I2C1_SDA	GEN1_I2C_SDA	I2C1_DAT	I2C1	Generic I²C
211	I2C1_SCL	GEN1_I2C_SCL	I2C1_CLK		
205	I2C2_SDA (DDC)	DDC_SDA	I2C4_DAT	I2C4	I²C port for the DDC interface
207	I2C2_SCL (DDC)	DDC_SCL	I2C4_CLK		
201	I2C3_SDA (CAM)	CAM_I2C_SDA	I2C3_DAT	I2C3	I²C port for the camera interface can also be used for other purposes
203	I2C3_SCL (CAM)	CAM_I2C_SCL	I2C3_CLK		

Table 6-27 Alternate TK1 I²C Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I2C Port	Description
71	TS_DIFF3-	DP_AUX_CH0_N	I2C6_DAT	I2C6	Aux channel for eDP
73	TS_DIFF3+	DP_AUX_CH0_P	I2C6_CLK		

Additional to the I²C interfaces that are provided by the main SoC, the companion MCU also features I²C interfaces. Please note that the standard Linux BSP does not support these I2C interfaces.

Table 6-28 Alternate K20 I²C Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I2C Port	Description
251	LCD1_R0	PTD9		I2C0 (K20)	Companion MCU I²C interface
307	AN1_ADC1	PTB1	I2C0_SDA		
311	AN1_TSWIP_ADC3	PTB3			
253	LCD1_R1	PTD8			
305	AN1_ADC0	PTB0/ LLWU_P5	I2C0_SCL		
309	AN1_ADC2	PTB2			
175	CAM1_D6	PTE0	I2C1_SDA	I2C1 (K20)	Companion MCU I²C interface
173	CAM1_D7	PTE1/ LLWU_P0	I2C1_SCL		

6.8.1 Real-Time Clock (RTC) recommendation

The Apalis module features an RTC circuit located inside the Power Management IC (PMIC). The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC needs to be retained even without the module's main voltage, a coin cell must be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 9.3). Therefore, a standard lithium coin cell battery can drain faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the module's I2C1 interface and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.

6.9 UART

The Apalis TK1 provides up to ten serial UART interfaces. Four of them are provided by the Nvidia Tegra K1 SoC and are available on dedicated UART pins as defined in the Apalis standard. The additional six UARTs are provided by the companion MCU. Please note that the standard Linux BSP does not support these six UART interfaces.

According to the Apalis specification, the Apalis UART1 (provided by the Tegra K1 UA3 interface) is a full-featured UART. Since the Tegra K1 does not feature the DTR, DSR, DCD, and RI signals, only RX/TX, as well as RTS/CTS, is available. The UART1 is used as a standard debug interface for the Toradex Linux operating systems. Therefore, it is desirable to keep this port accessible for system debugging

UART Features (TK1 signals only)

- Support 16450 and 16550 compatible modes
- 16-byte FIFO
- Up to 4.5 Mbaud
- Word length 5- to 8-bit, optional parity, one or two stop bits
- Auto sense baud detection

VFIR Features (TK1 signals only)

- Supports up to IrDA version 1.4 with 16Mbit/s
- 32bit x 16 deep FIFO

Table 6-29 UART1 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
118	UART1_RXD	GPIO_PU1	UA3_RXD	I	Received Data
112	UART1_TXD	GPIO_PU0	UA3_TXD	O	Transmitted Data
114	UART1_RTS	GPIO_PU3	UA3_RTS	O	Request to Send
116	UART1_CTS	GPIO_PU2	UA3_CTS	I	Clear to Send
110	UART1_DTR	UART3_RTS_N	GPIO3_PC.00	O	DTR function not available, only GPO
120	UART1_DSR	UART3_CTS_N	GPIO3_PA.01	I	CTS function not available, only GPI
122	UART1_RI	GPIO_PK7	GPIO3_PK.07	I	RI function not available, only GPI
124	UART1_DCD	GPIO_PB1	GPIO3_PB.01	I	DCD function not available, only GPI

Table 6-30 UART2 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
132	UART2_RXD	UART2_RXD	IR3_RXD	I	Received Data
126	UART2_TXD	UART2_TXD	IR3_TXD	O	Transmitted Data
128	UART2_RTS	UART2_RTS_N	UB3_RTS	O	Request to Send
130	UART2_CTS	UART2_CTS_N	UB3_CTS	I	Clear to Send

Table 6-31 UART3 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
136	UART3_RXD	UART3_RXD	UC3_RXD	I	Received Data
134	UART3_TXD	UART3_TXD	UC3_TXD	O	Transmitted Data

Table 6-32 UART4 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
140	UART4_RXD	GPIO_PB0	UD3_RXD	I	Received Data
138	UART4_TXD	GPIO_PJ7	UD3_TXD	O	Transmitted Data

For the UART3 and UART4 ports, there are additional hardware flow signals available. These signals are located on the DTR, DSR, and DCD signals of the UART1 port. The signals are not compatible with other Apalis modules.

Table 6-33 Additional UART3 and UART4 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
110	UART1_DTR	UART3_RTS_N	UC3_RTS	O	Additional Request to Send for UART 3
120	UART1_DSR	UART3_CTS_N	UC3_CTS	I	Additional Clear to Send UART 3
124	UART1_DCD	GPIO_PB1	UD3_CTS	I	Additional Clear to Send UART 4

The Apalis TK1 UART pins are level shifted on the module. Therefore, it is recommended to add pull-up or pull-down resistors to the non-used input pins (UART1_RXD, UART1_CTS, UART1_DSR, UART1_RI, UART1_DCD, UART2_RXD, UART2_CTS, UART3_RXD, UART4_RXD) to make sure they are not floating. See also section 4.1.5. The output pins can be left floating.
In addition to the four UARTs of the Tegra K1 SoC, the Kinetis K20 companion MCU provides up to six UART interfaces. These UARTs are not compatible with other Apalis modules. Please note that the standard Linux BSP does not support these UARTs.

Table 6-34 Additional K20 UART Signal Pins

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Description
255	LCD1_R2	PTD6/ LLWU_P15	UART0_RX	I	Received Data
265	LCD1_R7	PTB16			
177	CAM1_D5	PTB17	UART0_TX	O	Transmitted Data
243	LCD1_PCLK	PTD7			
187	CAM1_D0	PTA17	UART0_RTS_b	O	Request to Send
197	CAM1_HSYNC	PTA3			
247	LCD1_HSYNC	PTD4/ LLWU_P14			
309	AN1_ADC2	PTB2			
245	LCD1_VSYNC	PTD5	UART0_CTS_ b/ UART0_COL_b	I	Clear to Send
311	AN1_TSWIP_ADC3	PTB3			
173	CAM1_D7	PTE1/ LLWU_P0	UART1_RX	I	Received Data
261	LCD1_R5	PTC3/ LLWU_P7			
175	CAM1_D6	PTE0	UART1_TX	O	Transmitted Data
249	LCD1_DE	PTC4/ LLWU_P8			
179	CAM1_D4	PTE3	UART1_RTS_b	O	Request to Send
293	LCD1_B3	PTC1/ LLWU_P6			
277	LCD1_G4	PTC2	UART1_CTS_b	I	Clear to Send
301	LCD1_B7	PTE2/ LLWU_P1			

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Description
273	LCD1_G2	PTD2/ LLWU_P13	UART2_RX	I	Received Data
257	LCD1_R3	PTD3	UART2_TX	O	Transmitted Data
291	LCD1_B2	PTD0/ LLWU_P12	UART2_RTS_b	O	Request to Send
289	LCD1_B1	PTD1	UART2_CTS_b	I	Clear to Send
16	CAN2_RX	PTC16	UART3_RX	I	Received Data
181	CAM1_D3	PTE5			
297	LCD1_B5	PTB10			
18	CAN2_TX	PTC17	UART3_TX	O	Transmitted Data
185	CAM1_D1	PTE4/ LLWU_P2			
281	LCD1_G6	PTB11			
191	CAM1_PCLK	PTE25	UART4_RX	I	Received Data
183	CAM1_D2	PTE24	UART4_TX	O	Transmitted Data
253	LCD1_R1	PTD8	UART5_RX	I	Received Data
251	LCD1_R0	PTD9	UART5_TX	O	Transmitted Data
271	LCD1_G1	PTD11	UART5_CTS_b	I	Clear to Send

6.10 SPI

The Apalis module standard features two SPI ports. The NVIDIA Tegra K1 SoC provides the signals of the two ports. Since the corresponding Tegra pins are only 1.8V capable, level shifters are required on these pins. Therefore, the two primary SPI interfaces can only be used as master since the signal direction is fixed.

The Tegra K1 features an additional SPI port (SPI3) available as an alternate function of the SD1 interface. Since these pins do not need a level shifter, this interface can be used as master and slave. Please note that this interface is not compatible with other Apalis modules.

A fourth SPI port (TK1: SPI2C) of the Tegra K1 SoC is used to communicate with the companion MCU (K20: SPI2). The SoC is the master in this communication interface, while the MCU is the slave. More information on the interface between SoC and MCU can be found in section 5.

The SPI ports operate at up to 50 Mbps and provide full-duplex, synchronous, serial communication between the Apalis module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in, and data out. The third SPI port features some additional chip-select signals available as an alternate function to support multiple peripherals.

Features:

- Up to 50 Mbps
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable (SPI1 and SPI2 only Master)
- Simultaneous receive and transmit

Each SPI channel supports four different modes of the SPI protocol:

Table 6-35 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of SCK
4	1	1	The clock is negative polarity, and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCDs require configuration over SPI before being driven via the RGB or LVDS interface.

Table 6-36 Apalis SPI Port 1 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
225	SPI1_MOSI	ULPI_CLK	SPI1A_DOUT	O	Master Output, Slave Input
223	SPI1_MISO	ULPI_DIR	SPI1A_DIN	I	Master Input, Slave Output
227	SPI1_CS	ULPI_STP	SPI1A_CS0	O	Slave Select
221	SPI1_CLK	ULPI_NXT	SPI1A_SCK	O	Serial Clock

Table 6-37 Apalis SPI Port 2 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
231	SPI2_MOSI	GPIO_PG6	SPI4C_DOUT	O	Master Output, Slave Input
229	SPI2_MISO	GPIO_PG7	SPI4C_DIN	I	Master Input, Slave Output
233	SPI2_CS	GPIO_PI3	SPI4C_CS0	O	Slave Select
235	SPI2_CLK	GPIO_PG5	SPI4C_SCK	O	Serial Clock

The SPI1_MISO and SPI2_MISO input pins are level-shifted on the module. Therefore, it is recommended to add pull-up or pull-down resistors if they are not used to make sure they are not floating. See also section 4.1.5. The rest of the SPI pins can be left floating.

Table 6-38 Additional TK1 SPI port, incompatible with other modules

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
188	SD1_D1	SDMMC3_DAT1	SPI3D_DOUT	O	Master Output, Slave Input
186	SD1_D0	SDMMC3_DAT0	SPI3D_DIN	I	Master Input, Slave Output
176	SD1_D2	SDMMC3_DAT2	SPI3D_CS0	I/O	Slave Select 0
178	SD1_D3	SDMMC3_DAT3	SPI3D_CS1	O	Slave Select 1
180	SD1_CMD	SDMMC3_CMD	SPI3D_CS2	O	Slave Select 2
184	SD1_CLK	SDMMC3_CLK	SPI3D_SCK	I/O	Serial Clock

Additional to the three SPI ports provided by the main SoC, the companion MCU also features two SPI ports that can be used. Please note that the standard Linux BSP does not support these SPI ports.

Table 6-39 Additional K20 SPI port, not compatible with other modules

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Description
273	LCD1_G2	PTD2/ LLWU_P13	SPI0_SOUT	O	Master Output, Slave Input
275	LCD1_G3	PTC6/ LLWU_P10			
187	CAM1_D0	PTA17	SPI0_SIN	I	Master Input, Slave Output
257	LCD1_R3	PTD3			
259	LCD1_R4	PTC7			
249	LCD1_DE	PTC4/ LLWU_P8	SPI0_PCS0	I/O	Slave Select 0
291	LCD1_B2	PTD0/ LLWU_P12			
247	LCD1_HSYNC	PTD4/ LLWU_P14	SPI0_PCS1	O	Slave Select 1
261	LCD1_R5	PTC3/ LLWU_P7			
245	LCD1_VSYNC	PTD5	SPI0_PCS2	O	Slave Select 2
277	LCD1_G4	PTC2			
255	LCD1_R2	PTD6/ LLWU_P15	SPI0_PCS3	O	Slave Select 3
293	LCD1_B3	PTC1/ LLWU_P6			
263	LCD1_R6	PTC0	SPI0_PCS4	O	Slave Select 4
289	LCD1_B1	PTD1	SPI0_SCK	I/O	Serial Clock
173	CAM1_D7	PTE1/ LLWU_P0	SPI1_SOUT	O	Master Output, Slave Input
179	CAM1_D4	PTE3			
265	LCD1_R7	PTB16			
173	CAM1_D7	PTE1/ LLWU_P0	SPI1_SIN	I	Master Input, Slave Output
177	CAM1_D5	PTB17			
179	CAM1_D4	PTE3			
185	CAM1_D1	PTE4/ LLWU_P2	SPI1_PCS0	I/O	Slave Select 0
297	LCD1_B5	PTB10			
175	CAM1_D6	PTE0	SPI1_PCS1	O	Slave Select 1
181	CAM1_D3	PTE5	SPI1_PCS2	O	Slave Select 2
281	LCD1_G6	PTB11	SPI1_SCK	I/O	Serial Clock
301	LCD1_B7	PTE2/ LLWU_P1			

6.11 PWM (Pulse Width Modulation)

The NVIDIA Tegra K1 features a four-channel Pulse Width Modulator (PWM). The duty cycle has an 8-bit resolution (it can be set to a value between 0 and 255 in steps of 1/256). The maximum output frequency is 187.5 kHz.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights, or servo motors.

The Apalis standard defines a fifth dedicated PWM output for the display backlight. As the Tegra K1 features only four PWM controllers, the backlight PWM shares the Tegra K1 PM3_PWM3 output with the module edge connector pin 8 PWM4.

Table 6-40 PWM Interface Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Remarks
2	PWM1	GPIO_PH0	PM3_PWM0	O	
4	PWM2	GPIO_PH1	PM3_PWM1	O	
6	PWM3	GPIO_PH2	PM3_PWM2	O	
8	PWM4	GPIO_PH3	PM3_PWM3	O	Shared PWM output with BKL1_PWM
239	BKL1_PWM	GPIO_PU6			Shared PWM output with PWM4

In addition to the four PWM channels provided by the main SoC, the companion MCU features three FlexTimers with 12 output channels. Each channel can be configured for input capture, output compare, or PWM mode. Please note that the standard Linux BSP does not support these FlexTimers.

Table 6-41 TK20 FlexTimer Signals (not compatible with other Apalis modules)

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Remarks
197	CAM1_HSYNC	PTA3	FTM0_CH0	I/O	FlexTimer 0 Channel 0
293	LCD1_B3	PTC1/ LLWU_P6			
277	LCD1_G4	PTC2	FTM0_CH1	I/O	FlexTimer 0 Channel 1
195	CAM1_VSYNC	PTA5	FTM0_CH2	I/O	FlexTimer 0 Channel 2
261	LCD1_R5	PTC3/ LLWU_P7			
249	LCD1_DE	PTC4/ LLWU_P8	FTM0_CH3	I/O	FlexTimer 0 Channel 3
247	LCD1_HSYNC	PTD4/ LLWU_P14	FTM0_CH4	I/O	FlexTimer 0 Channel 4
245	LCD1_VSYNC	PTD5	FTM0_CH5	I/O	FlexTimer 0 Channel 5
255	LCD1_R2	PTD6/ LLWU_P15	FTM0_CH6	I/O	FlexTimer 0 Channel 6
243	LCD1_PCLK	PTD7	FTM0_CH7	I/O	FlexTimer 0 Channel 7
14	CAN1_TX	PTA12	FTM1_CH0	I/O	FlexTimer 1 Channel 0
305	AN1_ADC0	PTB0/ LLWU_P5			
12	CAN1_RX	PTA13/ LLWU_P4	FTM1_CH1	I/O	FlexTimer 1 Channel 1
307	AN1_ADC1	PTB1			
295	LCD1_B4	PTB18	FTM2_CH0	I/O	FlexTimer 2 Channel 0
279	LCD1_G5	PTB19	FTM2_CH1	I/O	FlexTimer 2 Channel 1

6.12 OWR (One Wire)

The One Wire Controller (OWR) implements a device communications bus system that provides low-speed data, signaling and power over a single wire. The OWR uses two signals for this - one for ground and the other for power and data.

On the Apalis TK1, the one-wire protocol is primarily intended for communication with battery controller chips. The OWR is multiplexed with the GPIO6 interface on the module and is not part of the Apalis module specification. Therefore, compatibility with other Apalis modules is not guaranteed.

Table 6-42 OWR Interface Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Remarks
13	GPIO6	OWR	OWR	I/O	Pay attention: the second SoC pin (PEX_L1_RST_N) is connected with the MXM pin.

6.13 SD/MMC

The NVIDIA Tegra K1 provides 4 SDIO interfaces; one is used internally for the eMMC Flash, and two are available on the module edge connector Pins. The fourth SD/MMC interface is neither available externally nor used internally. Even though the eMMC interface is specified in the Apalis standard with 8 data pins, on the Apalis TK1, only a 4-bit interface can be used.

The interfaces can interfere with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

Features

- Supports SD Memory Card Specification 4.0 (up to UHS-I, no UHS-II)
- Supports SDIO Card Specification Version 4.0 (up to UHS-I, no UHS-II)
- Supports MMC System Specification Version 4.51 (limited to 4-bit, no 8-bit)
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- Both interfaces support 3.3V and 1.8V IO voltage mode (Apalis standard is only 3.3V)

TK1 SDIO interface	Max Bus Width	Description
SDMMC1	4-bit	Apalis Standard MMC1 interface, only 4 bit
SDMMC2	8-bit	Unused, not available externally
SDMMC3	4-bit	Apalis Standard SD1 interface
SDMMC4	8-bit	Connected to the internal eMMC boot device. Not available at the module edge connector

According to the Apalis module specification, the SD/MMC interface's IO voltage level supports only a 3.3V logic level. Therefore, the SD interfaces are limited to default or high-speed mode; UHS-I modes are not supported. Nevertheless, the MMC1 interface (Tegra SDMMC1) and the SD1 interface (Tegra SDMMC3) can switch independently to the 1.8V IO level. This allows using the interface in UHS-I mode with higher speed. Please note that this IO voltage level is not mandatory in the Apalis module specification, and therefore other modules might not support this mode. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interfaces are used in the 1.8V mode, it is recommended to remove the carrier board's pull-up resistors. The Tegra features internal pull-up resistors, which can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage
Default Speed	25 MHz	12.5 MByte/s	3.3V
High Speed	50 MHz	25 MByte/s	3.3V
SDR12	25 MHz	12.5 MByte/s	1.8V
SDR25	50 MHz	25 MByte/s	1.8V
DDR50	50 MHz	50 MByte/s	1.8V
SDR50	100 MHz	50 MByte/s	1.8V
SDR104	208 MHz	104 MByte/s	1.8V

The I/O voltage of one power block can be changed independently from the other block, but all the corresponding block signals change their voltages together. The signals of the Apalis SD1 interface (TK1 function block SDMMC3) are located on one block while the signals of the Apalis MMC1 interface (TK1 function block SDMMC1) are on a different block. This means the SD1 and the MMC1 can change the I/O Voltage level independently. Since there are additional signals on each block that are not used for the interface, other pins will change the voltage. Ensure that these pins are not used if the I/O voltages of the SD/MMC interfaces are changed. More information can be found in section 4. The following tables show all pins that are in the SDMMC1 and SDMMC3 power blocks:

Table 6-43 SDMMC1 Power Block Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	Remarks
150	MMC1_CMD	SDMMC1_CMD	Used as standard MMC1 interface
160	MMC1_D0	SDMMC1_DAT0	
162	MMC1_D1	SDMMC1_DAT1	
144	MMC1_D2	SDMMC1_DAT2	
146	MMC1_D3	SDMMC1_DAT3	
154	MMC1_CLK	SDMMC1_CLK	
164	MMC1_CD#	SDMMC1_WP_N	Pay attention to these additional signals since they may not be used for the MMC1 interface
148	MMC1_D4	CLK2_REQ	
152	MMC1_D5	CLK2_OUT	

Table 6-44 TK1 SDMMC3 Power Block Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	Remarks
180	SD1_CMD	SDMMC3_CMD	Used as standard SD1 interface
186	SD1_D0	SDMMC3_DAT0	
188	SD1_D1	SDMMC3_DAT1	
176	SD1_D2	SDMMC3_DAT2	
178	SD1_D3	SDMMC3_DAT3	
184	SD1_CLK	SDMMC3_CLK	
156	MMC1_D6	SDMMC3_CLK_LB_IN	Pay attention to this additional signal since it may not be used for the SD1 interface

The I/O voltage of the Apalis SD1 interface (TK1 function block SDMMC3) is provided by the LDO6 output of the power management IC. The LDO1 output provides the I/O voltage of the Apalis MMC1 interface (TK1 function block SDMMC1). The voltages are changed by setting the according LDO output voltage register of the PMIC.

Table 6-45 Apalis MMC1 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
150	MMC1_CMD	SDMMC1_CMD	SDMMC1_CMD	I/O	Command
160	MMC1_D0	SDMMC1_DAT0	SDMMC1_DAT0	I/O	Serial Data 0
162	MMC1_D1	SDMMC1_DAT1	SDMMC1_DAT1	I/O	Serial Data 1
144	MMC1_D2	SDMMC1_DAT2	SDMMC1_DAT2	I/O	Serial Data 2
146	MMC1_D3	SDMMC1_DAT3	SDMMC1_DAT3	I/O	Serial Data 3
154	MMC1_CLK	SDMMC1_CLK	SDMMC1_CLK	O	Serial Clock
164	MMC1_CD#	SDMMC1_WP_N	GPIO3_PV.03	I	Card Detect (standard GPIO)

Table 6-46 SD1 Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
180	SD1_CMD	SDMMC3_CMD	SDMMC3_CMD	I/O	Command
186	SD1_D0	SDMMC3_DAT0	SDMMC3_DAT0	I/O	Serial Data 0
188	SD1_D1	SDMMC3_DAT1	SDMMC3_DAT1	I/O	Serial Data 1
176	SD1_D2	SDMMC3_DAT2	SDMMC3_DAT2	I/O	Serial Data 2
178	SD1_D3	SDMMC3_DAT3	SDMMC3_DAT3	I/O	Serial Data 3
184	SD1_CLK	SDMMC3_CLK	SDMMC3_CLK	O	Serial Clock
190	SD1_CD#	SDMMC3_CD_N	GPIO3_PV.02	I	Card Detect (standard GPIO with input level shifter)

Additional to the main SoC's two SD/MMC interfaces, the companion MCU features another SD/MMC interface. Please note that the standard Linux BSP does not support this interface.

Table 6-47 Additional K20 SD/MMC Interface Signal Pins (not compatible with other modules)

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Description
179	CAM1_D4	PTE3	SDHC0_CMD	I/O	Command
173	CAM1_D7	PTE1/ LLWU_P0	SDHC0_D0	I/O	Serial Data 0
175	CAM1_D6	PTE0	SDHC0_D1	I/O	Serial Data 1
181	CAM1_D3	PTE5	SDHC0_D2	I/O	Serial Data 2
185	CAM1_D1	PTE4/ LLWU_P2	SDHC0_D3	I/O	Serial Data 3
301	LCD1_B7	PTE2/ LLWU_P1	SDHC0_DCLK	O	Serial Clock

6.14 Analog Audio

The Apalis TK1 offers analog audio input and output channels. On the module, an NXP SGTL5000 chip handles the analog audio interface. The SGTL5000 is connected over I²S (I2S2) with the NVIDIA Tegra K1. Please consult the NXP SGTL5000 datasheet for more information.

Table 6-48 Analogue Audio Interface Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
306	AAP1_MICIN	Analog Input	Microphone input	10
310	AAP1_LIN_L	Analog Input	Left Line Input	9
312	AAP1_LIN_R	Analog Input	Right Line Input	8
316	AAP1_HP_L	Analog Output	Headphone Left Output	4
318	AAP1_HP_R	Analog Output	Headphone Right Output	1

6.15 Digital Audio

The Apalis module standard provides one digital audio interface. Even Though other Apalis modules might support Intel® Audio Codec '97 (also known as AC'97 or AC97) or Intel® High Definition Audio (also known as HD Audio, HDA or Azalia), the Apalis TK1 supports only I²S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS).

Depending on the used audio codec, the bit clock and the left-right-sync are sourced by the codec or by the processor. The Apalis TK1 module features bidirectional level shifters on these two signals to interface audio codecs of both variants. Please note, the direction of these two pins cannot be changed individually. Both pins are either inputs or outputs. The direction is controlled with the GPIO3_PS.03 of the SoC.

Table 6-49 Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
202	DAP1_D_IN	DAP2_DIN	I2S1_SDATA_IN	I	Data Input to TK1 (input level shifter)
196	DAP1_D_OUT	DAP2_DOUT	I2S1_SDATA_OUT	O	Data Output from TK1 (output level shifter)
204	DAP1_SYNC	DAP2_FS	I2S1_LRCK	I/O	Field Select (bidirectional level shifter)
200	DAP1_BIT_CLK	DAP2_SCLK	I2S1_SCLK	I/O	Serial Clock (bidirectional level shifter)
194	DAP1_MCLK	CLK3_OUT	extperiph3_clk	O	External Peripheral Clock (output level shifter)
198	DAP1_RESET#	GPIO_PBB3	GPIO3_PBB.03	O	Audio codec reset (regular GPO, output level shifter) Push-pull output, not open drain

The DAP1_D_IN pin is level shifted on the module. Therefore, it is recommended to add a pull-up or pull-down resistor if the pin is not used to make sure they are not floating. See also section 4.1.5. The rest of the digital audio pins can be left floating.

6.16 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

Features:

- Supports 5 data formats
  - 16-bit
  - 20-bit
  - 24-bit
  - Raw
  - 16-bit packed
- Supports "auto-lock" mode to automatically detect "spdifin" sample rate and lock onto the data stream.
- Supports override mode to provide a manual control to sample "spdifin" data stream.

Table 6-50 S/PDIF Data Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
215	SPDIF1_OUT	SPDIF_OUT	SPDIF_OUT	O	Serial data output
217	SPDIF1_IN	SPDIF_IN	SPDIF_IN	I	Serial data input

6.17 Touch Panel Interface

The Apalis TK1 offers a 4-wire resistive touch interface. The touch interface is implemented in the K20 companion MCU with a simple external circuit. The external circuit allows drawing more current than the standard GPIO of the K20 would allow. This is necessary since some resistive touch panels require a higher current. The standard Linux BSP contains the support of the resistive touch panel interface.

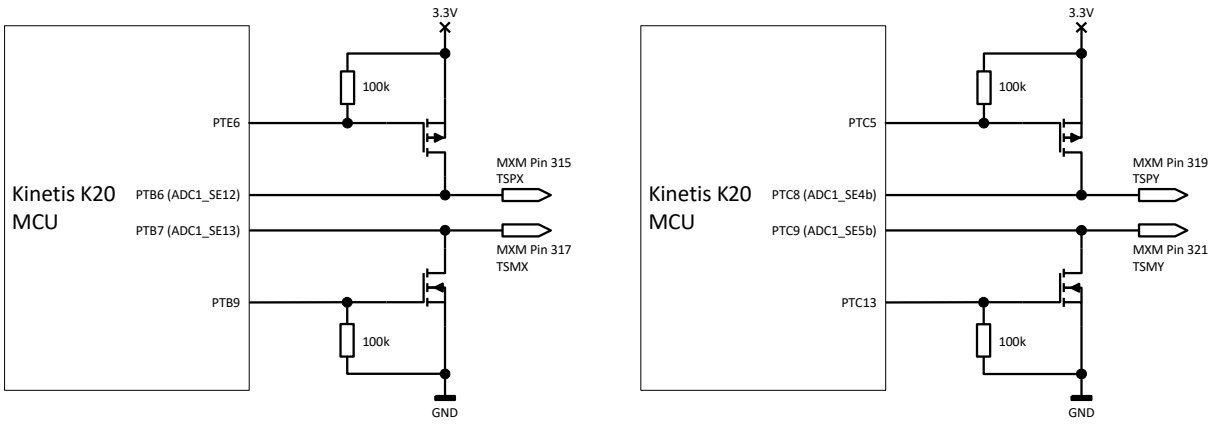


Figure 9: External Circuit for Touch Panel Interface

Table 6-51 Touch Interface Pins

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Remarks
315	AN1_TSPX	PTB6	ADC1_SE12	I	ADC input for X+ (ADC1_SE12)
		PTE6	PTE6	O	FET gate driver (GPIO PTE6)
317	AN1_TSMX	PTB7	ADC1_SE13	I	ADC input for X- (ADC1_SE13)
		PTB9	PTB9	O	FET gate driver (GPIO PTB9)
319	AN1_TSPY	PTC8	ADC1_SE4b/ CMP0_IN2	I	ADC input for Y+ (ADC1_SE4b)
		PTC5/ LLWU_P9	PTC5	O	FET gate driver (GPIO PTC5)
321	AN1_TSMY	PTC9	ADC1_SE5b/ CMP0_IN3	I	ADC input for Y- (ADC1_SE5b)
		PTC13	PTC13	O	FET gate driver (GPIO PTC13)

If the touch panel interface is unused, leave the pins unconnected and disable the driver. Connecting the pins to the ground (especially TSPX and TSPY) while having the driver still enabled could cause a short circuit if the driver turns on the high side FET.

6.18 Analog Inputs

The Apalis module standard features four dedicated pins for analog inputs. These analog inputs are read by the ADCs that are located in the Kinetis K20 companion MCU. The K20 features two ADC with totally up to 21 channels available at the module edge connector. Only four of these 21 channels are compatible with other Apalis modules. The other 17 channels are located as alternate functions of other pins. The standard Linux BSP supports the ADC inputs of the MCU.

Features

- Two independent converters
- 12-bit ADC
- 0 to 3.3V rail to rail
- Conversion rate up to 818 KS/s
- Input resistance typical 2kΩ

Table 6-52 Analog Inputs Pins

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Remarks
305	AN1_ADC0	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	I	Dedicated ADC input
307	AN1_ADC1	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	I	Dedicated ADC input
309	AN1_ADC2	PTB2	ADC0_SE12/ TSI0_CH7	I	Dedicated ADC input
311	AN1_TSWIP_ADC3	PTB3	ADC0_SE13/ TSI0_CH8	I	Dedicated ADC input

Table 6-53 Additional Analog Inputs Pins (not compatible with other modules)

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Remarks
315	AN1_TSPX	PTB6	ADC1_SE12	I	ADC input (primarily used as touch interface)
317	AN1_TSMX	PTB7	ADC1_SE13	I	ADC input (primarily used as touch interface)
319	AN1_TSPY	PTC8	ADC1_SE4b/ CMP0_IN2	I	ADC input (primarily used as touch interface)
321	AN1_TSMY	PTC9	ADC1_SE5b/ CMP0_IN3	I	ADC input (primarily used as touch interface)
277	LCD1_G4	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	I	Additional ADC input
289	LCD1_B1	PTD1	ADC0_SE5b	I	Additional ADC input
245	LCD1_VSYNC	PTD5	ADC0_SE6b	I	Additional ADC input
255	LCD1_R2	PTD6/ LLWU_P15	ADC0_SE7b	I	Additional ADC input
263	LCD1_R6	PTC0	ADC0_SE14/ TSI0_CH13	I	Additional ADC input
293	LCD1_B3	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	I	Additional ADC input
183	CAM1_D2	PTE24	ADC0_SE17	I	Additional ADC input
191	CAM1_PCLK	PTE25	ADC0_SE18	I	Additional ADC input
301	LCD1_B7	PTE2/ LLWU_P1	ADC1_SE6a	I	Additional ADC input
179	CAM1_D4	PTE3	ADC1_SE7a	I	Additional ADC input
297	LCD1_B5	PTB10	ADC1_SE14	I	Additional ADC input
281	LCD1_G6	PTB11	ADC1_SE15	I	Additional ADC input
187	CAM1_D0	PTA17	ADC1_SE17	I	Additional ADC input

6.19 Camera Interface

Even though the Apalis module standard reserves dedicated pins for parallel camera inputs, the Apalis TK1 module does not feature such an interface. Nevertheless, the Apalis TK1 features up to three MIPI/CSI-2 compatible camera inputs. The interfaces use the MIPI D-PHY as a physical layer.

The CSI signals are located in the type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules will be compatible with this interface. If you plan to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

As the CSI is a high-speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is type-specific. Please find the information in the table below.

Table 6-54 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 6-55 CSI interface signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	CSI_A_CLK_P	CSI1_CLK+	I	CSI interface 1 clock
161	TS_DIFF18-	CSI_A_CLK_N	CSI1_CLK-	I	
157	TS_DIFF17+	CSI_A_D0_P	CSI1_D1+	I/O	CSI interface 1 data lane 1
155	TS_DIFF17-	CSI_A_D0_N	CSI1_D1-	I/O	
151	TS_DIFF16+	CSI_A_D1_P	CSI1_D2+	I	CSI interface 1 data lane 2
149	TS_DIFF16-	CSI_A_D1_N	CSI1_D2-	I	
145	TS_DIFF15+	CSI_B_D0_P	CSI1_D3+	I	CSI interface 1 data lane 3
143	TS_DIFF15-	CSI_B_D0_N	CSI1_D3-	I	
139	TS_DIFF14+	CSI_B_D1_P	CSI1_D4+	I	CSI interface 1 data lane 4
137	TS_DIFF14-	CSI_B_D1_N	CSI1_D4-	I	
133	TS_DIFF13+	CSI_E_CLK_P	CSI2_CLK+	I	CSI interface 2 clock
131	TS_DIFF13-	CSI_E_CLK_N	CSI2_CLK-	I	
97	TS_DIFF7+	CSI_E_D0_P	CSI2_D1+	I/O	CSI interface 2 data lane 1
95	TS_DIFF7-	CSI_E_D0_N	CSI2_D1-	I/O	
127	TS_DIFF12+	DSI_B_CLK_P	CSI3_CLK+	I	CSI interface 3 clock
125	TS_DIFF12-	DSI_B_CLK_N	CSI3_CLK-	I	
121	TS_DIFF11+	DSI_B_D0_P	CSI3_D1+	I/O	CSI interface 3 data lane 1
119	TS_DIFF11-	DSI_B_D0_N	CSI3_D1-	I/O	
115	TS_DIFF10+	DSI_B_D1_P	CSI3_D2+	I	CSI interface 3 data lane 2
113	TS_DIFF10-	DSI_B_D1_N	CSI3_D2-	I	
109	TS_DIFF9+	DSI_B_D2_P	CSI3_D3+	I	CSI interface 3 data lane 3
107	TS_DIFF9-	DSI_B_D2_N	CSI3_D3-	I	
103	TS_DIFF8+	DSI_B_D3_P	CSI3_D4+	I	CSI interface 3 data lane 4
101	TS_DIFF8-	DSI_B_D3_N	CSI3_D4-	I	

Table 6-56 Additional Camera Interface Signals (Apalis Standard)

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
193	CAM1_MCLK	CAM_MCLK	vimclk_alt3	O	Master clock output for camera
201	I2C3_SDA (CAM)	CAM_I2C_SDA	I2C3_DAT	I/O	Camera control I^2C
203	I2C3_SCL (CAM)	CAM_I2C_SCL	I2C3_CLK	O	Camera control I^2C

6.20 Clock Output

The Apalis TK1 provides up to four external clock outputs on the module edge connector. One output is dedicated to the camera interface, while the other is reserved for the digital audio interface. If the clock outputs are not required for those interfaces, they can also be used as general-purpose clock outputs.

The on-module audio codec has its own master clock source (extperiph1_clk). This source is not shared with the externally available sources.

Table 6-57 Clock Output Signal Pins

X1 Pin#	Apalis Signal Name	TK1 Ball Name	TK1 Port Name	I/O	Description
194	DAP1_MCLK	CLK3_OUT	extperiph3_clk	O	Clock output for the digital audio interface, see section 0
193	CAM1_MCLK	CAM_MCLK	vimclk_alt3	O	Clock output for the parallel and serial camera interface, see section 6.19

Two additional clock outputs are located as an alternate function of pins. One of these two additional clock signals is sourced by the companion MCU. Please be aware that the standard Linux BSP does not support the MCU clock output.

Table 6-58 Additional Clock Output Signal Pins

X1 Pin#	Apalis Signal Name	TK1/K20 Ball Name	TK1/K20 Port Name	I/O	Description
152	MMC1_D5	CLK2_OUT	extperiph2_clk	O	Clock output, sourced by main SoC
261	LCD1_R5	PTC3/ LLWU_P7	CLKOUT	O	Clock output, sourced by companion MCU

The PCIe interface requires a 100MHz reference clock for all the peripherals and switches. The Apalis standard defines one differential pair for the reference clock. Zero delay clock buffers can be used if more than one reference clock sink is present on the carrier board.

Table 6-59 PCIe Reference clock Signals

X1 Pin#	Apalis Signal Name	TK1 Ball Name	I/O	Description
55	PCIE1_CLK+	PEX_CLK1P	O	Apalis standard reference clock differential pair
53	PCIE1_CLK-	PEX_CLK1N	O	

6.21 Keypad

The Apalis TK1 does not feature a dedicated keypad interface. However, you can use any free GPIOs to realize a matrix keypad interface.

6.22 Controller Area Network (CAN)

The two Flexible Controller Area Network (FlexCAN) interfaces are provided by the Kinetis K20 companion MCU. The CAN protocol complies with the CAN 2.0B specification. The interface supports the standard and extended message frame format. The standard Linux BSP supports the CAN interface.

Features

- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of zero to eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free-running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 6-60 CAN Signal Pins

X1 Pin#	Apalis Signal Name	K20 Ball Name	K20 Port Name	I/O	Description
14	CAN1_TX	PTA12	CAN0_TX	O	CAN port 1 transmit pin
12	CAN1_RX	PTA13/ LLWU_P4	CAN0_RX	I	CAN port 1 receive pin
18	CAN2_TX	PTC17	CAN1_TX	O	CAN port 2 transmit pin
16	CAN2_RX	PTC16	CAN1_RX	I	CAN port 2 receive pin

6.23 JTAG

The JTAG interface is usually not required for software development with the Apalis TK1. There is always the possibility of reprogramming the module using the Recovery Mode over USB. For flashing the module in recovery mode and debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The Apalis specification standardizes the location. Please be aware, the reference voltage for the interface is 1.8V.

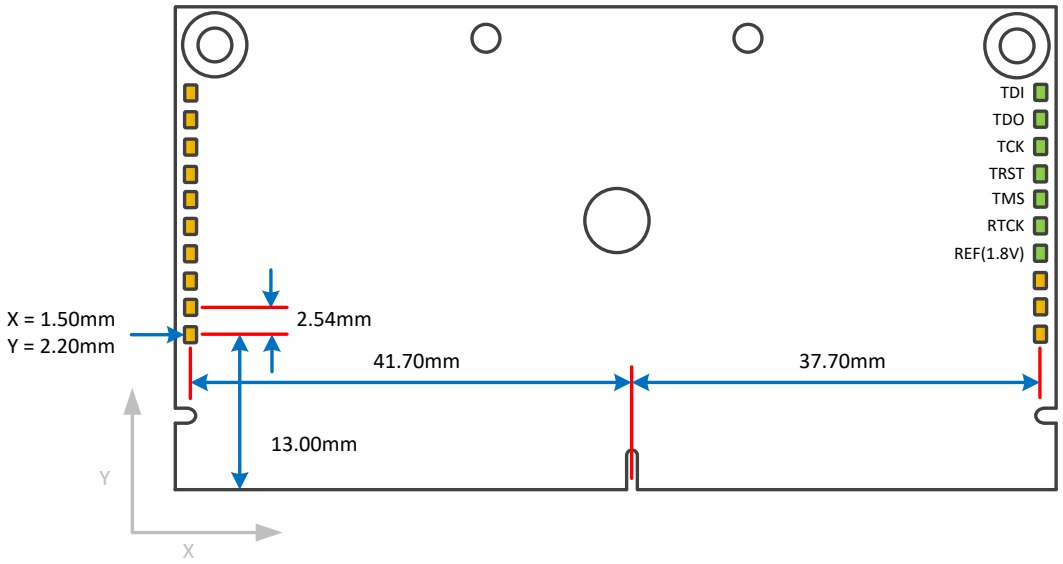


Figure 10 JTAG test point location on the bottom side of the module

7. Recovery Mode

The recovery mode (USB serial loader) can be used for downloading new software to the Apalis TK1 even if the bootloader is no longer capable of booting the module. In the standard development process, this mode is not needed. When the module is in recovery mode, the USBO1 interface connects it to a host computer. You will find additional information at our Developer Centre (http://developer.toradex.com).

The recovery mode pads need to be shorted during the initial power on or reset of the module to enter recovery mode. Figure 11 shows the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling down pin 63 of the module edge connector (TS_1) with a 1kΩ resistor while booting. This pin is located in the type-specific area. It is not guaranteed that other Apalis modules will be set into recovery mode in the same way.

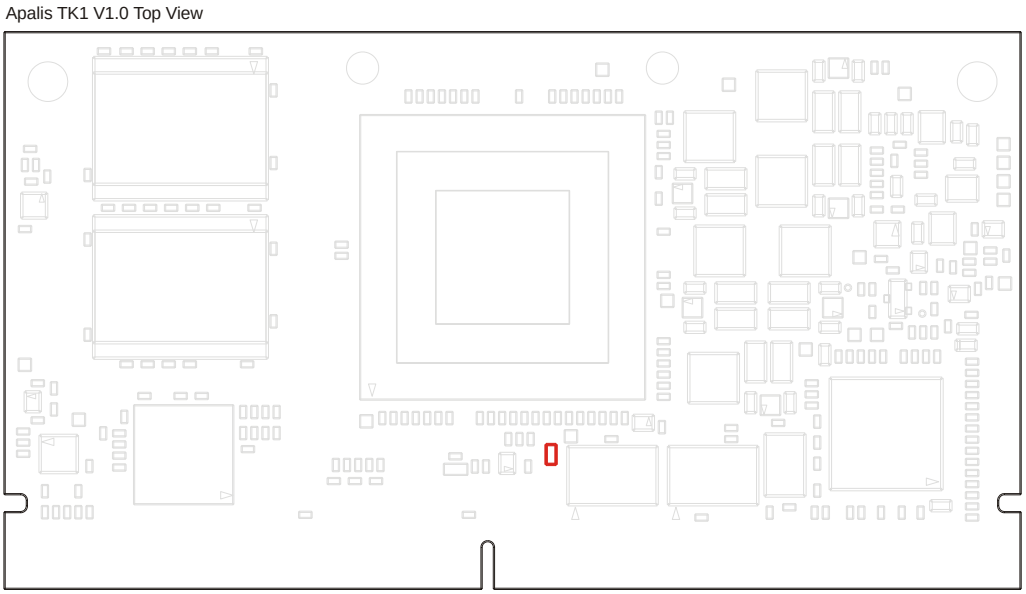


Figure 11 Location of recovery mode pads

8. Known Issues

Up-to-date information about all known hardware issues. can be found in the errata document, which can be downloaded on our website at:

http://docs.toradex.com/103358-apalis-tk1-errata.pdf

9. Technical Specifications

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC	Main power supply	-0.3	3.6	V
Vmax_AVCC	Analog power supply	-0.3	3.6	V
Vmax_VCC_BACKUP	RTC power supply	-0.5	3.6	V
Vmax_IO_3.3V	TK1 IO pins with 3.3V logic level	-0.5	3.6	V
Vmax_IO_1.8V_3.3V	TK1 IO pins with 1.8V/3.3V switchable logic level	-0.5	3.6	V
Vmax_IO_3.3V_Tol	TK1 1.8V IO pins which are 3.3V tolerant	-0.5	3.6	V
Vmax_IO_In_Shift	TK1 IO pins which feature an input level shifter	-0.5	3.6	V
Vmax_IO_Bi_Shift	TK1 IO pins which feature a bidirectional level shifter	-0.5	3.6	V
Vmax_IO_K20	IO pins of the K20 companion MCU	-0.3	3.6	V
Vmax_AN1	ADC and touch analog input	-0.3	3.6	V
Vmax USBO1_VBUS	Input voltage at USBO1_VBUS	-0.5	6.0	V

9.2 Recommended Operation Conditions

Table 9-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3	3.465	V
AVCC	Analogue power supply	3.0	3.3	3.465	V
VCC_BACKUP	RTC power supply	2.5	3.3	3.6	V

9.3 Electrical Characteristics

Table 9-3 Typical Power Consumption

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	0.46	A
IDD_HIGHCPU	Maximal CPU Load, 3D-graphic test	3.3	A
IDD_HD	Full HD Video on HDMI (h.264 decoding, CPU full load)	2.02	A
IDD_SUSPEND	Module in Suspend State	TBD	mA
IDD_BACKUP	Current consumption of internal RTC	8.9	µA

These typical values are just for indication. The actual consumption varies between different modules and is temperature-dependent. The current consumption can be higher than IDD_HIGHCPU, depending on the GPU load and the temperature.

9.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.

9.5 Mechanical Characteristics

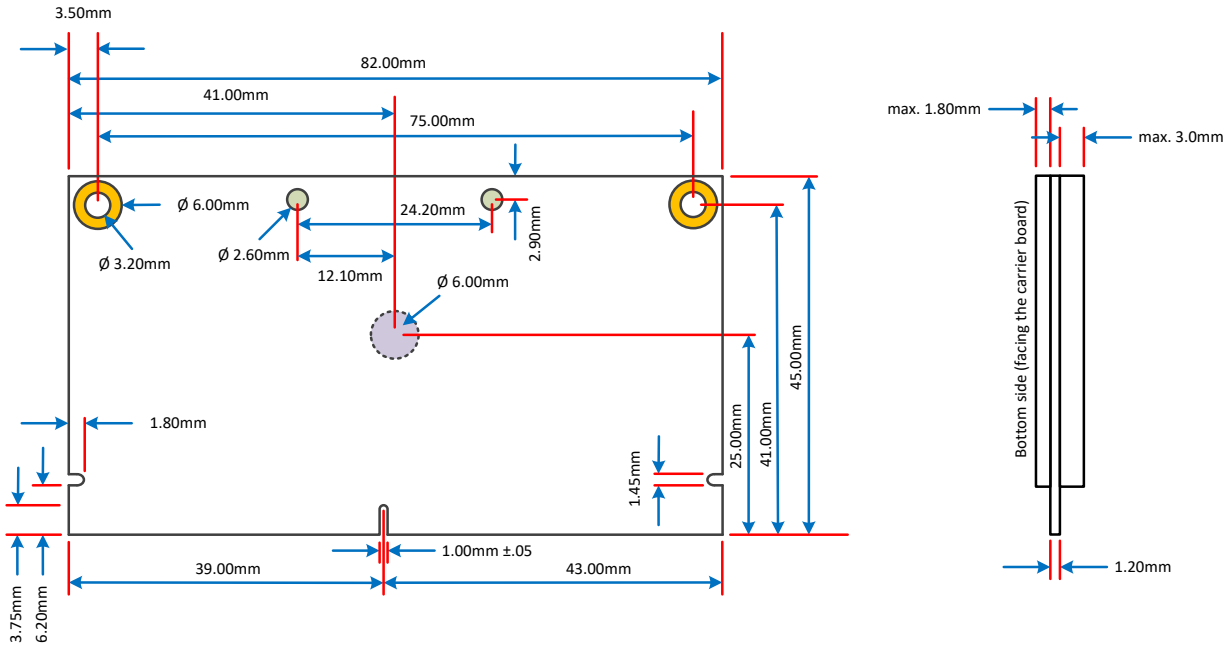


Figure 12 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

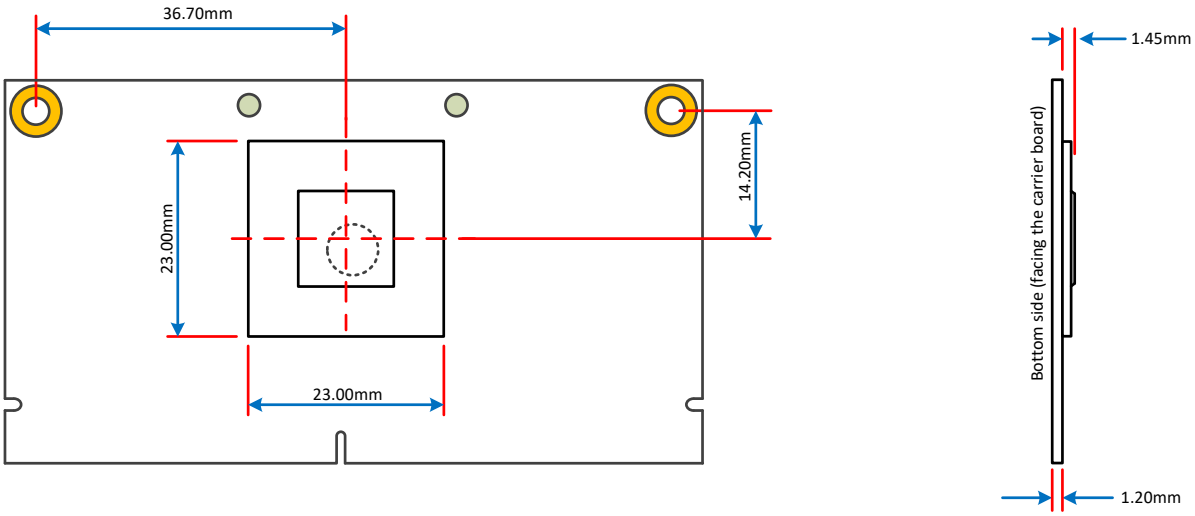


Figure 13 Mechanical position of NVIDIA Tegra K1 SoC (top view)
Tolerance for all measures: +/- 0.1mm

9.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board-to-board stacking heights from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314B1-2-R300, which has a board-to-board height of 3.0mm. This stacking height allows using the MXM SnapLock system for easy fixing of the module to the carrier board.

You can refer to a list of other MXM3 connectors on the developer website.

9.6 Thermal Specification

The Apalis TK1 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling, enabling the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The Tegra K1 SoC features DVFS on the CPU, GPU, as well as the Core voltage. This allows the Apalis TK1 to deliver higher performance at lower average power consumption compared to other solutions. The Apalis TK1 modules come with two temperature sensors that measure the CPU and the Apalis PCB temperature. If the Tegra K1 reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- It is generally advised to use a heat sink on the Apalis TK1
- If you need the full CPU/Graphics performance over a long time, we recommend well designing the whole heat dissipation solution of the system.
- Toradex provides a heatsink for the Apalis TK1. This solution can be used passively as well as in combination with a fan. The Apalis Heatsink Type 3 is compatible with the Apalis TK1. More information can be found here: http://developer.toradex.com/products/apalis-heatsink
- Suppose you only use the peak performance for a short time. In that case, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.

In general, the better the thermal solution is, the more performance you can get out of the Apalis TK1 Module.

Table 9-4 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Apalis TK1	Operating temperature range	-25		85[1]	°C
Apalis TK1	Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Apalis TK1	Junction temperature SoC (sensed from thermal diode)	-25		105	°C
Apalis TK1	Thermal Resistance Junction-to-Ambient, TK1 only. (Θ_{JA})[2]		12.3		°C/W
Apalis TK1	Thermal Resistance Junction-to-Top of TK1 chip case. (Ψ_{JCtop})[2]		0.02		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

9.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Computer-On-Modules - COM ***category:***

Click to view products by Toradex ***manufacturer:***

Other Similar products are found below :

CEM881PG-i7-5650U t2Express-HL-i5-4402E 34006-0000-99-2 34099-0000-99-2 38017-0000-00-0 34099-0000-99-0 36026-0000-99-1 36026-0000-99-0 38017-0000-00-5 36016-4000-19-4 VSTK-6ULL-NFC LEC-iMX8MP-Q-4G-32G-ER LEC-iMX8MP-Q-2G-32G-CT 38116-0000-00-5 34011-0832-16-7 36030-0000-18-2 t2cExpress-BT-E3845-LVDS 51011-0432-13-2-4 34011-0400-16-5 0016 0040 1970004870T001 0063 36030-0000-99-0 36028-0000-99-0 0055 QSMP-1510/SOCK 0034 PER-T720-M2AI-0801 PER-T720-M2AI-0421 0039 VCB-8MM-STD W612M3A600SC 24828-107 24571-309 30846-682 ET970K-X3G UPC-PLUSX5Q-A20-0464 UPC-PLUSX7-A20-08128 UPC-PLUSX5D-A20-0232 UPC-PLUSX7-A20-0864 UPX-WHLCR-A20-04064 cExpress-BL-i5-5350U cExpress-KL-i3-7100U Express-HLE-i3-4100E Express-IBR-i7-R-3612QE Express-KLE-E3-1505L v6 LEC-BT4-4G-8G-ER Q7-BT1-2G-8G-ER ROM-3310WS-MCA1E