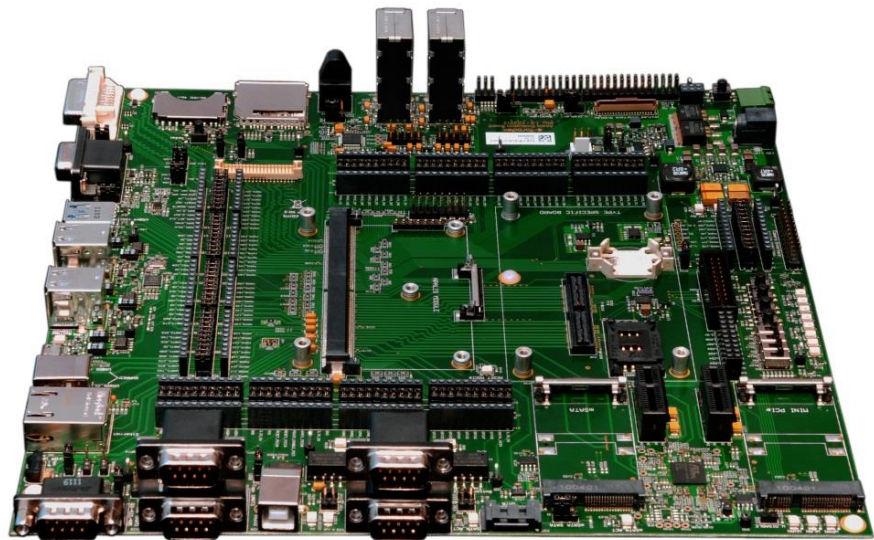


# Apalis Evaluation Board

## Datasheet



## Revision History

Date	Doc. Rev.	Board Version	Changes
03-Nov-15	Rev. 1.0	V1.1	Initial Release: Datasheet has been updated to the new format
30-Sept-16	Rev. 1.1	V1.1	Section 2.2, Hardware Architecture Block Diagram: Updated block diagram (fig. 1) Section 2.3.1, Top Side Connectors: Corrected input voltage range for the power supply connector X15 Section 3.9.7, Unified Interface Display (X31): Minor correction
09-June-17	Rev. 1.2	V1.1	Section 1.1, Reference Documents: Updated web-links Section 3.9.7, Unified Interface Display (X31): Updated web-links Section 3.11.1, Mezzanine Type Specific (X38): Minor Corrections Section 6, Design data: Updated web-link

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# 1 Introduction

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The Apalis Evaluation Board is a flexible development environment with which you can explore and evaluate the functionality and performance of the Apalis product family.

Complementing the existing Colibri module family, Apalis supports a huge variety of industry standard interfaces, while at the same time providing advanced multimedia and high speed connectivity making it suitable for an almost unlimited number of applications. Apalis interfaces can be easily accessed by means of physical connectors and standard pitch headers. The GPIO usage allows easy probing of a large number of Apalis interfaces and easy access to break and jumper signals as needed.

The Apalis Evaluation Board PCB is comprised of four layers, of which only one is used for high speed signal routing. This demonstrates how the Direct Breakout technology makes it incredibly easy to implement leading edge interfaces with minimal risk and effort. CAE data for the board, including schematics, layout and IPC-7351 compliant component libraries, are freely downloadable from Toradex developer website.

## 1.1 Reference Documents

For detailed technical information about suitable computer modules, please refer to the documents listed below.

### 1.1.1 Apalis Computer Modules

An overview of the Apalis product family:

<https://www.toradex.com/computer-on-modules/apalis-arm-family>

### 1.1.2 Pushbutton On/Off controller datasheet

<http://cds.linear.com/docs/en/datasheet/2954fb.pdf>

### 1.1.3 USB Hub datasheet

<http://ww1.microchip.com/downloads/en/DeviceDoc/00001692A.pdf>

### 1.1.4 PLX PEX 8605-AB product page

<http://www.plxtech.com/products/expresslane/pex8605>

### 1.1.5 Toradex Developer Website - Carrier Board Design

<http://developer.toradex.com/carrier-board-design>

## 2 Features

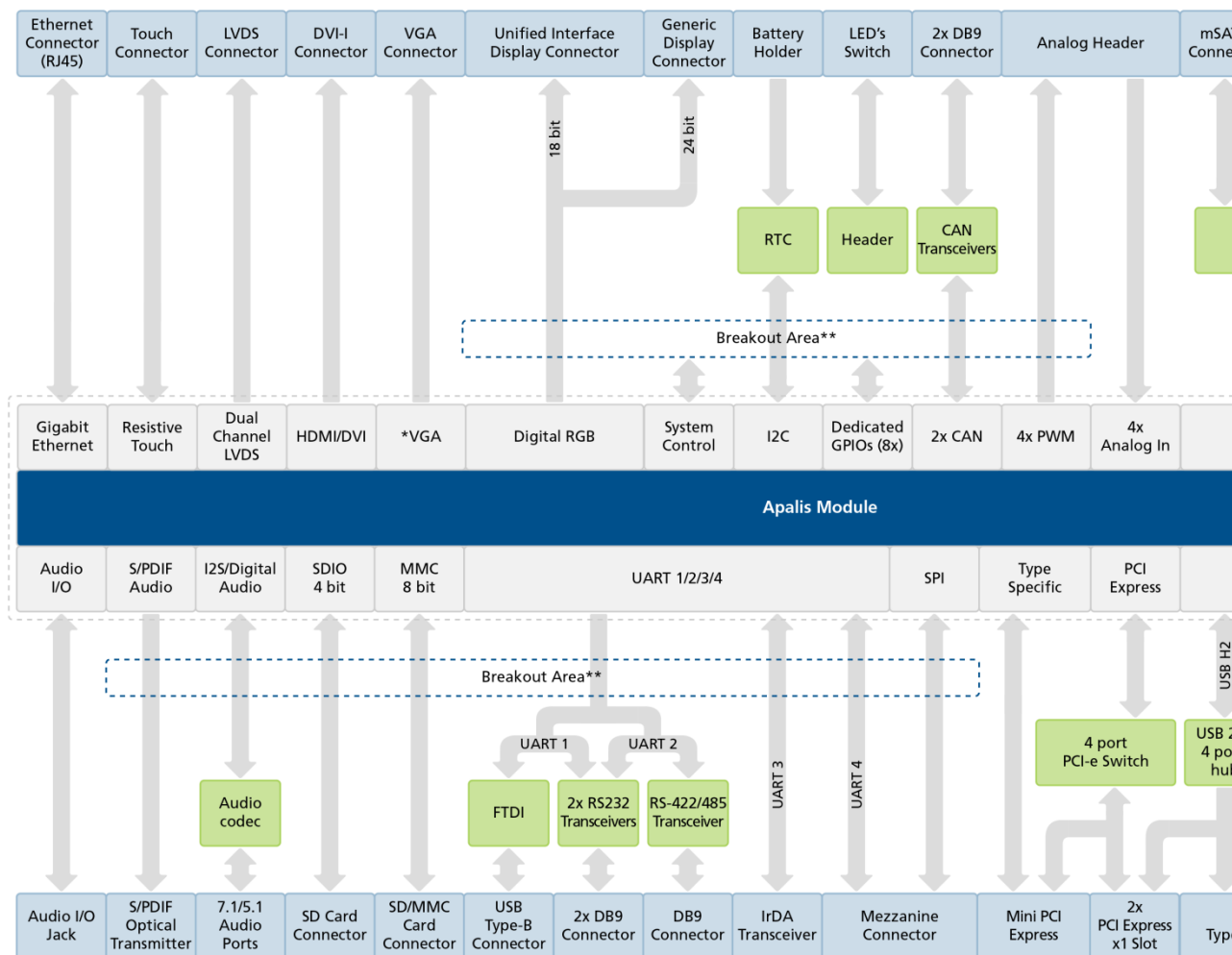
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### 2.1 Overview

The Apalis Evaluation Board provides the following features and communication interfaces:

- 4x USB 2.0 port through on board USB Hub
- 1x USB 3.0 port
- USB 3.0 OTG Micro-AB connector for host and host/client
- USB Client Type B port (shared with the OTG)
- USB Type B port (optionally connected to FF UART via USB to serial converter)
- RJ45 Ethernet (10/100/1000 Mbit)
- 1x SD/MMC 8 Bit
- 1x SD/MMC 4 Bit
- 1x Serial ATA/mSATA (Shared)
- Type Specific Board Connector
- 2x PCIe x1 slot
- Mini PCIe
- Digital (TDMS) interface on DVI-D connector
- Analog VGA interface on a 15 way D-type connector
- Dual channel LVDS interface (up to 24 bit colour)
- Digital RGB interface (up to 24 bit colour)
- Unified Display Interface with built in resistive touch for direct LCD panel connection
- Analog audio I/O on 3.5mm stereo jacks
- HDA 7.1 Codec (including analog connectors)
- 1x S/PDIF In/Out (Out also on TosLink)
- 2x RS232 Serial Interfaces
- IrDA
- 1x RS422/485 Serial Interface
- 3x I2C, 2x SPI, 4x PWM, 4x Analog inputs
- 2x CAN 2.0B Interface (up to 1Mbit/s)
- Real-time clock with battery backup
- Resistive touch screen connector 4/5-wire
- LEDs and Switches
- Extremely Flexible and easy to use GPIO breakout and jumper area allowing easy signal re-routing, external connection and measurement/probing
- JTAG
- Parallel Camera Interface

## 2.2 Hardware Architecture Block Diagram



\* This is a module-specific feature and may not be supported by all the computer-on-modules in the Apalis family. For more details, refer to the module's datasheet.

\*\* The breakout/jumper area provides a flexible mechanism for changing the hardware configuration or signal routing for any external circuit.

**Fig.1 Apalis Evaluation Board Hardware Architecture**

## 2.3 Physical Drawing

### 2.3.1 Top Side Connectors

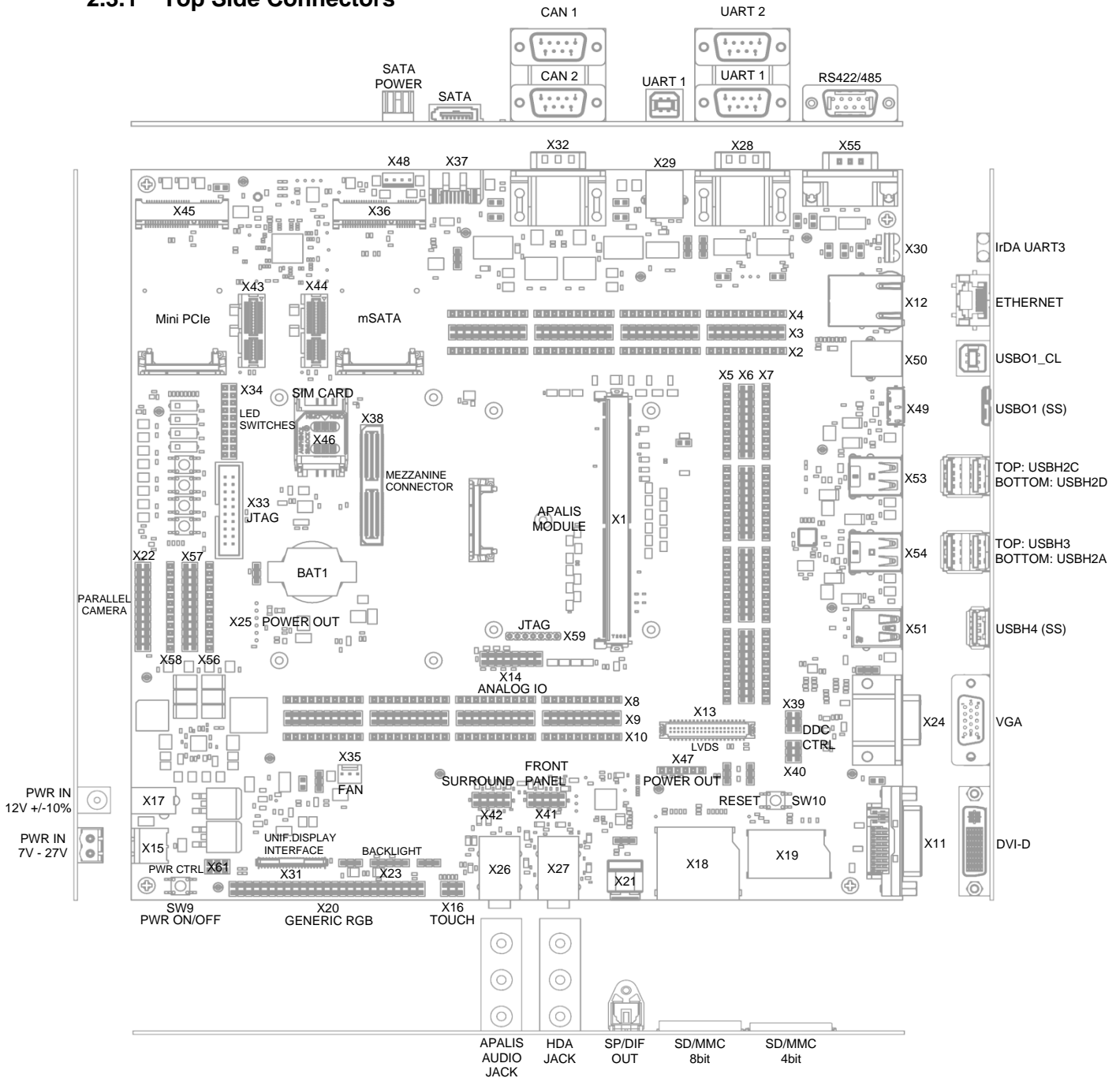


Fig.2 Apalis Evaluation Board connectors – Top Side



Ref	Description	Remarks
X1	Apalis MXM3	
X2	MXM3 breakout area 1	
X3	Jumper Array 1	
X4	Function Tap 1	
X5	MXM3 breakout area 2	
X6	Jumper Array 2	
X7	Function Tap 2	
X8	MXM3 breakout area 3	
X9	Jumper Array 3	
X10	Function Tap 3	
X11	DVI-D	
X12	Gigabit Ethernet	
X13	LVDS Connector	
X14	Analog IO	
X15	Terminal Block Power Supply Connector	Power Input: 7 – 27V
X16	Generic Touch-Screen	
X17	Barrel Power Supply Connector	Power Input: 12V±10%
X18	SD/MMC 8bit	
X19	SD/MMC 4bit	
X20	Generic Display Connector	
X21	SPDIF Out	
X22	Parallel Camera Interface	
X23	LCD Inverter	
X24	VGA	
X25	Power out	
X26	3x Audio Jack	Apalis Audio Codec Output
X27	3x HDA Audio Jack	HDA Codec Output
X28	2x UART	
X29	USB to UART converter	Optionally selectable shared with the connector X29 Bottom
X30	IrDA	
X31	Unified Display Interface	
X32	2x CAN	
X33	JTAG to Host	
X34	Switches/LEDs	
X35	FAN Connector	
X36	mSATA	Shared with the connector X37
X37	SATA	Shared with the connector X36
X38	Mezzanine Type Specific	
X39	DDC SCL Interface Selection	
X40	DDC SDA Interface Selection	
X41	HDA Front Panel	
X42	HDA Surround	

Ref	Description	Remarks
X43	PCIe x1	
X44	PCIe x1	
X45	Mini PCIe	
X46	SIM Card Holder	
X47	Power Out Connector	
X48	SATA Power Connector	
X49	USB OTG SS	USB01 - Shares the USB2.0 lane with the connector X50
X50	USB CLIENT	USB01 - Shares the USB2.0 lane with the connector X49
X51	USB HOST SS	USBH4 Super Speed
X53	2X USB HOST	TOP: USBH2C – BOTTOM:USBH2D
X54	2X USB HOST	TOP: USBH3 – BOTTOM:USBH2A
X55	RS422/485	
X56	Camera MXM3 Breakout Area	Some of these pins are routed through the Mezzanine Connector
X57	Camera Jumper Array	
X58	Camera Function Tap	Connected to X22
X59	JTAG to Apalis	
X61	Power Control Header	

## 3 Interface Description

### 3.1 Apalis Computer-On-Module

Type: MXM3 321 pin Socket

Manufacturer: JAE - MM70-314-310B1

For the pin-out of the Apalis module, please refer to the applicable Apalis module datasheet.

MXM3 SnapLock and Spacers are available on Apalis Evaluation Board for fixing the Apalis module with the carrier board. It is recommended to use M3 size screws to fasten Apalis module with the Spacers.

### 3.2 Power Supply

Apalis Evaluation Board has two different power connectors that can be used to power the board:

- The connector X15 which has a wide input voltage range of 7-27V DC.
- The connector X17 is a 12V +/-10% input. It must be used when the 12V voltage supply is required on the board (e.g. while using a cooling fan, a PCIe device or when this voltage is needed on the LVDS connector).

The 12V power supply is obtained directly from the connector X17; this means that, even though this voltage is protected by a 2A fuse, it is not regulated.

The on-board power supply provides the following supplies (maximum power).

- 5V / 5A (25W)
- 3.3V / 5A (16.5W)

The supply is protected against reverse input voltage polarity and short circuits, limiting the maximum current to about 5A. However, the protection diode in the input voltage path is thermally not designed to carry such a high current, especially at low input voltages. If your application dissipates more than 20W, please consider one of the following:

- Work with a high input voltage, close to 24V
- Add a heat-sink to the polarity protection diode
- Short the polarity protection diode with a wire (removes the reverse polarity protection!)

#### 3.2.1 Terminal Block Power Supply Connector (X15)

Connector type: AUK TB5102PRB-H

Pin	Description	Voltage / Range
1	GND_IN	
2	PWR_IN	7 – 27V

#### 3.2.2 Barrel Power Supply Connector (X17)

Connector type: Amtek DCJ20-0014TB-L

Pin	Description	Voltage / Range
1	12V_IN	7 -12V
2	GND_IN	

#### 3.2.3 Power Out Header (X25)

Connector type: 1x6Pin Header Male, 2.54mm, Not Assembled

Pin	Description	Remarks
1	3.3V_SW	
2	GND	
3	5V_SW	
4	GND	
5	12V_SW_UNREG_F	2A FUSE
6	V_SUPPLY_FILT_F	2A FUSE

Please note that the pins number 5 and 6 are not regulated because they are respectively directly connected to the power supply connectors X15 and X17.

### 3.2.4 Power Out Connector (X47)

Connector type: 1x6Pin Header Male, 2.54mm,

Pin	Description	Remarks
1	3.3V_SW	
2	3.3V_SW	
3	3.3V_SW	
4	GND	
5	GND	
6	GND	

### 3.2.5 Power Control

Power control of the Apalis Evaluation Board is implemented using the Linear LTC2954 Pushbutton On/Off controller and with the signal POWER\_ENABLE\_MOC1 which is used to enable the peripheral power supplies.

For further information about the signals provided by the controller LTC2954 please refer to the datasheet. For more information regarding the power up sequence which is implemented on the board please refer to the document “Apalis Carrier Board Design Guide”.

The Power CTRL connector X61 allows the Reset and Power Button control signals to be accessed externally.

#### 3.2.5.1 Power Control Header (X61)

Type: 2 x 3Pin Header Female, 2.54mm

Pin No.	Signal Name	IO Type	Voltage	Pullup/Pulldown
1	PWR_BTN#	I		100k to +1.9V
2	GND	PWR		
3	PWR_CTRL	I	+3.3V max	100k to GND
4	INT#	I		10k to +3.3V
5	FORCE_OFF#	I		100k to +3.3V
6	RESET_MICO#	IO	+3.3V	

The pin 3 of the connector X61 can be used in order to override the Pushbutton controller. The following table shows the behaviour of the board according to the level of the PWR\_CTRL signal:

PWR_CTRL Level	Description
0V	The Pushbutton controller is working normally
3.3V	The Apalis Evaluation Board is Always On when power is applied

#### 3.2.5.2 Always On Jumper (JP19)

Jumper JP19 can be used to obtain “Always On” behaviour.

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper position	Description
Open	Board power supply is controlled via Power On/Off Switch.
Closed	Board power supply will be in the “Always On” state. Apalis Evaluation Board will be powered-up as soon as external power is applied.

### 3.2.6 FAN Connector

The Apalis Evaluation board provides a FAN connector, X6. The 12V supply which is available at this connector is connected to the 12V regulated power supply using a transistor which is controlled by 3.3V\_SW or, optionally, using the GPIO8 signal for software control. Jumper JP20 determines this configuration:

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	Automatic ON
2 - 3	GPIO8 enabled

#### 3.2.6.1 FAN Connector (X35)

Connector type: 1x3 Pin Header Male with friction lock, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR	PWR_IN	
2	V_FAN_UNREG		PWR	+12V	
3	NC				

Please note that V\_FAN\_UNREG is not regulated power supply. It will be the same voltage that has been provided on the connectors X17. Use only 12V+/-10% power supply with connector X17.

### 3.3 Indications

There are four LEDs on the Apalis Evaluation Board to indicate the power supply status.

Ref.	Description
LED9	3.3V
LED10	5V_SW
LED11	3.3V_SW
LED30	12V_SW_UNREG_F

Refer to Apalis Evaluation Board schematics for more details.

### 3.4 Ethernet

The Apalis Evaluation Board provides an RJ45 connector with integrated magnetics for 10/100/1000Mb Ethernet.

#### 3.4.1 Ethernet (X12)

Connector type: RJ45, BEL L829-1J1T-43

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	ETH1_CTREF_2				
2	ETH1_MDI2_N	34			
3	ETH1_MDI2_P	32			
4	ETH1_MDI1_P	56			
5	ETH1_MDI1_N	54			
6	ETH1_CTREF_1				
7	ETH1_CTREF_3				
8	ETH1_MDI3_P	38			
9	ETH1_MDI3_N	40			
10	ETH1_MDI0_N	48			
11	ETH1_MDI0_P	50			
12	ETH1_CTREF_0				
13	ETH1_ACT_C	42 (via R5)		+3.3V	
14	3.3V_SW		PWR	+3.3V	
15	ETH1_LINK_GB	44 (via R293)			
16	3.3V_SW		PWR	+3.3V	
17	ETH1_LINK_C	44 (via R6)			
S1/S2	SHIELD		PWR		

## 3.5 USB

### 3.5.1 USB Host/Client Interface

The Apalis Evaluation Board integrates a USB 3.0 OTG Micro-AB (X49), which is shared with a USB Type B connector (X50) for an additional client/host interface.

#### 3.5.1.1 USB OTG SS (X49)

Connector type: USB OTG A/B, CNC Tech 1003-005-23100

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	VCC_USBO1		PWR	+5V	
2	USBO1_D_CON_N	76			
3	USBO1_D_CON_P	74			
4	USBO1_ID	72	I	+3.3V	
5	GND_USBO1		PWR		
6	USBO1_SSTX_N	70			
7	USBO1_SSTX_P	68			
8	GND_USBO1		PWR		
9	USBO1_SSRX_N	64			
10	USBO1_SSRX_P	62			
S1/S2	SHIELD		PWR		

#### 3.5.1.2 USB Client (X50)

Connector type: USB Type B, FCI 61729-0010BLF

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	VCC_USBO1		PWR	+5V	
2	USBO1_D_CL_N	76 (via R288)			
3	USBO1_D_CL_P	74 (via R287)			
4	GND_USBO1		PWR		
S1/S2	SHIELD		PWR		

### 3.5.2 USB Host Interface

The Apalis Evaluation Board integrates a 4 port USB Hub (SMSC USB2514B-AEZC) to provide 4x USB 2.0 host interfaces.

For further information about the USB Hub please refer to the SMSC website.

In addition the Apalis Evaluation board features one USB 3.0 Type A (X51) port which can be used with the modules that support USB Super Speed interface.

#### 3.5.2.1 2xUSB Host (X53)

Connector type: Stacked USB 2.0 Type-A, Mill-Max 896-43-008-90-000000

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
U1	VCC_USBH2C		PWR	+5V	
U2	USBH2C_D_CON_N				
U3	USBH2C_D_CON_P				
U4	GND_USBH2C		PWR		
L1	VCC_USBH2D		PWR	+5V	
L2	USBH2D_D_CON_N				
L3	USBH2D_D_CON_P				

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
L4	GND_USBH2D		PWR		
S1/S2	SHIELD		PWR		
S3/S4	SHIELD		PWR		

### 3.5.2.2 2xUSB Host (X54)

Connector type: Stacked USB 2.0 Type-A, Mill-Max 896-43-008-90-000000

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
U1	VCC_USBH3		PWR	+5V	
U2	USBH3_D_CON_N	88			
U3	USBH3_D_CON_P	86			
U4	GND_USBH3		PWR		
L1	VCC_USBH2A		PWR	+5V	
L2	USBH2A_D_CON_N				
L3	USBH2A_D_CON_P				
L4	GND_USBH2A		PWR		
S1/S2	SHIELD		PWR		
S3/S4	SHIELD		PWR		

### 3.5.2.3 USB Host SS (X51)

Connector type: USB 3.0 Type-A, Tyco 1932258-1

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	VCC_USBH4		PWR	+5V	
2	USBH4_D_CON_N	100			
3	USBH4_D_CON_P	98			
4	GND_USBH4		PWR		
5	USBH4_SSRX_N	92			
6	USBH4_SSRX_P	94			
7	GND_USBH4		PWR		
8	USBH4_SSTX_N	104			
9	USBH4_SSTX_P	106			
S1/S2	SHIELD		PWR		



### 3.6 PCIe

The Apalis Evaluation Board features the ExpressLane™ PEX 8605-AB 4-Lane, 4-Port PCI Express Gen2 Switch from PLX. It is used to connect the standard PCIe interface on the Apalis Module to 2 PCIe x1 connectors and a mini PCIe slot.

For further information about the PEX 8605-AB, please refer to the PLX data book.

#### 3.6.1 PCIe x1 (X43)

Connector type: Sullins NWE18DHHN-T931

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	GND		PWR		
A2	12V_SW_UNREG_F		PWR	+12V	
A3	12V_SW_UNREG_F		PWR	+12V	
A4	GND		PWR		
A5	NC				
A6	NC				
A7	NC				
A8	NC				
A9	3.3V_SW		PWR	+3.3V	
A10	3.3V_SW		PWR	+3.3V	
A11	PCIE1_RESET#			+3.3V	
A12	GND		PWR		
A13	PCIE1C_CLK_P			+3.3V	
A14	PCIE1C_CLK_N			+3.3V	
A15	GND		PWR		
A16	PCIE1C_RX_P		I	+3.3V	
A17	PCIE1C_RX_N		I	+3.3V	
A18	GND		PWR		
B1	12V_SW_UNREG_F		PWR	+12V	
B2	12V_SW_UNREG_F		PWR	+12V	
B3	NC				
B4	GND		PWR		
B5	PCIE1_C_SMCLK		IO	+3.3V	
B6	PCIE1_C_SMBDAT		IO	+3.3V	
B7	GND		PWR		
B8	3.3V_SW_		PWR	+3.3V	
B9	NC				
B10	3.3V_SW_		PWR	+3.3V	
B11	PCIE1_C_WAKE#				
B12	NC				
B13	GND		PWR		
B14	PCIE1C_TX_P		O	+3.3V	
B15	PCIE1C_TX_N		O	+3.3V	
B16	GND		PWR		
B17	PCIE1_C_PRSENT2#		IO	+3.3V	
B18	GND		PWR		

Please note that 12V\_SW\_UNREG\_F is not regulated power supply. It will be the same voltage that has been provided on the connectors X17. Use only 12V+/-10% power supply with connector X17.

### 3.6.2 PCIe x1 (X44)

Connector type: Sullins NWE18DHHN-T931

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	GND		PWR		
A2	12V_SW_UNREG_F		PWR	+12V	
A3	12V_SW_UNREG_F		PWR	+12V	
A4	GND		PWR		
A5	NC				
A6	NC				
A7	NC				
A8	NC				
A9	3.3V_SW		PWR	+3.3V	
A10	3.3V_SW		PWR	+3.3V	
A11	PCIE1_RESET#			+3.3V	
A12	GND		PWR		
A13	PCIE1A_CLK_P			+3.3V	
A14	PCIE1A_CLK_N			+3.3V	
A15	GND		PWR		
A16	PCIE1A_RX_P		I	+3.3V	
A17	PCIE1A_RX_N		I	+3.3V	
A18	GND		PWR		
B1	12V_SW_UNREG_F		PWR	+12V	
B2	12V_SW_UNREG_F		PWR	+12V	
B3	NC				
B4	GND		PWR		
B5	PCIE1_A_SMCLK		IO	+3.3V	
B6	PCIE1_A_SMBDAT		IO	+3.3V	
B7	GND		PWR		
B8	3.3V_SW_		PWR	+3.3V	
B9	NC				
B10	3.3V_SW_		PWR	+3.3V	
B11	PCIE1_A_WAKE#				
B12	NC				
B13	GND		PWR		
B14	PCIE1A_TX_P		O	+3.3V	
B15	PCIE1A_TX_N		O	+3.3V	
B16	GND		PWR		
B17	PCIE1_A_PRSENT2#		IO	+3.3V	
B18	GND		PWR		

Please note that 12V\_SW\_UNREG\_F is not regulated power supply. It will be the same voltage that has been provided on the connectors X17. Use only 12V+/-10% power supply with connector X17.

### 3.6.3 Mini PCIe (X45)

Connector type: Mini PCIe Card Connector and Latch, Molex 67910-5700, 48099-5701

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	PCIE1_B_WAKE#	37 (via R267)			4.7K to 3.3V_SW
2	3.3V_PCIE1_B		PWR	+3.3V	
3	NC				
4	GND		PWR		
5	NC				
6	1.5V_PCIE1_B		PWR	+1.5V	
7	NC				
8	PCIE1_B_UIM_PWR				
9	GND		PWR		
10	PCIE1_B_UIM_DATA				
11	PCIE1B_CLK_N				
12	PCIE1_B_UIM_CLK				
13	PCIE1B_CLK_N				
14	PCIE1_B_UIM_RESET		O		
15	GND		PWR		
16	PCIE1_B_UIM_VPP		PWR		
17	NC				
18	GND		PWR		
19	NC				
20	PCIE1_B_WDISABLE#	JP23	I		47K to 3.3V_PCIE1_B
21	GND		PWR		
22	RESET_MOCI#	26	I		
23	PCIE1B_RX_N		I		
24	3.3V_PCIE1_B		PWR	+3.3V	
25	PCIE1B_RX_P		I		
26	GND		PWR		
27	GND		PWR		
28	1.5V_MSATA1		PWR	+1.5V	
29	GND		PWR		
30	PCIE1_B_SMCLK	211 (via R265)			
31	PCIE1B_TX_N		O		
32	PCIE1_B_SMDAT	209 (via R266)	IO		
33	PCIE1B_TX_P		O		
34	GND		PWR		
35	GND		PWR		
36	USBH2B_D_N				
37	GND		PWR		
38	USBH2B_D_P				
39	3.3V_PCIE1_B		PWR	+3.3V	
40	GND		PWR		
41	3.3V_PCIE1_B		PWR	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
42	PCIE1_B_WWLAN#				
43	GND		PWR		
44	PCIE1_B_WLAN#				
45	NC				
46	PCIE1_B_WPAN#				
47	NC				
48	1.5V_MSATA1		PWR	+1.5V	
49	NC				
50	GND		PWR		
51	NC				
52	3.3V_PCIE1_B		PWR	+3.3V	

### 3.6.4 SIM Card Holder (X46)

Connector type: FCI 7111S2015X02LF

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	PCIE1_B_UIM_PWR		PWR		
2	PCIE1_B_UIM_RESET		IO		
3	PCIE1_B_UIM_CLK		IO		
5	GND		PWR		
6	PCIE1_B_UIM_VPP		PWR		
7	PCIE1_B_UIM_DATA		IO		

### 3.7 SATA

The Apalis Evaluation board supports the Serial ATA (SATA) interface on the Apalis module and allows peripherals such as external hard drives, SSDs and mSATA SSDs to be connected.

Jumper JP21 control the routing of the SATA signals to connector X37 or to the mSATA slot X36. Use of these interfaces is mutually exclusive:

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	mSATA connector (X36) is active
2 - 3	SATA connector (X37) is active

#### 3.7.1 mSATA (X35)

Connector type: Mini PCIe Card Connector and Latch, Molex 67910-5700, 48099-5701

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	NC				
2	3.3V_MSATA1		PWR	+3.3V	
3	NC				
4	GND		PWR		
5	NC				
6	1.5V_MSATA1		PWR	+1.5V	
7	NC				
8	NC				
9	GND		PWR		
10	NC				
11	NC				
12	NC				
13	NC				
14	NC				
15	GND		PWR		
16	NC				
17	NC				
18	GND		PWR		
19	NC				
20	NC				
21	GND		PWR		
22	NC				
23	SATA1_MSATA_RX_P	25 (via IC19)	I		
24	3.3V_MSATA1		PWR	+3.3V	
25	SATA1_MSATA_RX_N	27 (via IC19)	I		
26	GND		PWR		
27	GND		PWR		
28	1.5V_MSATA1		PWR	+1.5V	
29	GND		PWR		
30	SATA1_MSATA_SCL	211 (via R159)	O	+3.3V	
31	SATA1_MSATA_TX_N	31 (via IC19)	O		
32	SATA1_MSATA_SDA	209 (via R160)	IO	+3.3V	
33	SATA1_MSATA_TX_P	33 (via IC19)	O		
34	GND		PWR		
35	GND		PWR		

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
36	NC				
37	GND		PWR		
38	NC				
39	3.3V_MSATA1		PWR	+3.3V	
40	GND		PWR		
41	3.3V_MSATA1		PWR	+3.3V	
42	NC				
43	NC				
44	NC				
45	NC				
46	NC				
47	NC				
48	1.5V_MSATA1		PWR	+1.5V	
49	SATA1_MSATA_ACT#				100K to 3.3V_SW
50	GND		PWR		
51	SATA1_MSATA_PREDET#	(TP35)			
52	3.3V_MSATA1		PWR	+3.3V	

For further information regarding the mSATA interface, please refer to Serial ATA Specification Rev. 3.1 Gold

### 3.7.2 SATA (X37)

Type: mini PCIe Card Holder and latch: Molex 67910-5700, 48099-5701

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR		
2	SATA1_SATA_TX_P	33 (via IC19)	O		
3	SATA1_SATA_TX_N	31 (via IC19)	O		
4	GND		PWR		
5	SATA1_SATA_RX_N	27 (via IC19)	I		
6	SATA1_SATA_RX_P	25 (via IC19)	I		
7	GND		PWR		

### 3.7.3 SATA Power Connector (X48)

Type: 172732-4

Pin	Description	Voltage / Range
1	12V_SW_SATA	+12V
2	GND	
3	GND	
4	5V_SW_SATA	+5V

Please note that 12V\_SW\_SATA is not regulated power supply. It will be the same voltage that has been provided on the connectors X17. Use only 12V+/-10% power supply with connector X17.

### 3.8 SD Card / MMC

The Apalis Evaluation Board features 4bit SDIO and 8bit MMC interfaces. The hardware supported card detect function is implemented. It is possible to read the write protect status by using a test point present on the PCB.

#### 3.8.1 SD Card / MMC 8bit (X18)

Connector type: SD/MMC Card Holder, Amphenol 101-00565-64

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	MMC1_WP	(TP14)	O		
2	MMC1_CD#	164	I	+3.3V	10k to 3.3V_SW
3	MMC1_D1	162	IO	+3.3V	68k to 3.3V_SW
4	MMC1_D0	160	IO	+3.3V	68k to 3.3V_SW
5	MMC1_D7	158	IO	+3.3V	68k to 3.3V_SW
6	GND		PWR		
7	MMC1_D6	156	IO	+3.3V	68k to 3.3V_SW
8	MMC1_CLK	154	I	+3.3V	
9	3.3V_MMC		PWR		
10	GND		PWR		
11	MMC1_D5	152	IO	+3.3V	68k to 3.3V_SW
12	MMC1_CMD	150	I	+3.3V	33k to 3.3V_SW
13	MMC1_D4	148	IO	+3.3V	68k to 3.3V_SW
14	MMC1_D3	146	IO	+3.3V	68k to 3.3V_SW
15	MMC1_D2	144	IO	+3.3V	68k to 3.3V_SW

#### 3.8.2 SD Card / MMC 4bit (X19)

Connector type: SD/MMC Card Holder, CENLINK M90-03011-03YD

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	SD1_D3	178	IO	+3.3V	68k to 3.3V_SW
2	SD1_CMD	180	I	+3.3V	33k to 3.3V_SW
3	GND		PWR		
4	3.3V_SD		PWR	+3.3V	
5	SD1_CLK	184	I	+3.3V	
6	GND		PWR		
7	SD1_D0	186	IO	+3.3V	68k to 3.3V_SW
8	SD1_D1	188	IO	+3.3V	68k to 3.3V_SW
9	SD1_D2	176	IO	+3.3V	68k to 3.3V_SW
10	SD1_CD#	190	O	+3.3V	10k to 3.3V_SW
11	SD1_WP	(TP13)	O		

### 3.9 Display Interface

The Apalis Evaluation Board provides many options for connecting LCD panels and monitors, with the following four interfaces supported:

- 24 bit digital RGB
- Dual Channel 24 bit LVDS
- DVI-D
- VGA

Almost any TFT or STN display can be connected to the LCD port of the Apalis module by simply connecting the necessary signals from connectors X16 and X20 (which provide standard 2.54mm pitch) to the display.

Toradex provides a range of different tools and utilities to help with the easy configuration of different LCD panels. For details please refer to: <http://developer.toradex.com>

#### 3.9.1 DVI-I Connector (X11)

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	HDMI1_TXD2_N	224	O		
2	HDMI1_TXD2_P	222	O		
3	GND		PWR		
4	NC				
5	NC				
6	I2C2_DDC_SCL_DVI (Refer Section 3.9.8)		O		
7	I2C2_DDC_SDA_DVI (Refer Section 3.9.8)		IO		
8	NC				
9	HDMI1_TXD1_N	230	O		
10	HDMI1_TXD1_P	228	O		
11	GND		PWR		
12	NC				
13	NC				
14	V_DISP		PWR	+5V	
15	GND		PWR		
16	HDMI1_HPD	232 (via JP1)	I		
17	HDMI1_TXD0_N	236	O		
18	HDMI1_TXD0_P	234	O		
19	GND		PWR		
20	NC				
21	NC				
22	GND		PWR		
23	HDMI1_TXC_P	240	O		
24	HDMI1_TXC_N	242	O		
C1	NC				
C2	NC				
C3	NC				
C4	NC				
C5	GND		PWR		



### 3.9.2 LVDS Connector (X13)

Connector type: Hirose DF13A-40DP-1.25V(55)

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	LVDS1_A_TX3_P	272			
2	GND		PWR		
3	LVDS1_A_TX3_N	270			
4	LVDS1_B_CLK_N	276			
5	GND		PWR		
6	LVDS1_B_CLK_P	278			
7	LVDS1_A_TX2_P	266			
8	GND		PWR		
9	LVDS1_A_TX2_N	264			
10	LVDS1_B_TX0_N	282			
11	GND		PWR		
12	LVDS1_B_TX0_P	284			
13	LVDS1_A_TX1_P	260			
14	GND		PWR		
15	LVDS1_A_TX1_N	258			
16	LVDS1_B_TX1_N	288			
17	GND		PWR		
18	LVDS1_B_TX1_P	290			
19	LVDS1_A_TX0_P	254			
20	GND		PWR		
21	LVDS1_A_TX0_N	252			
22	LVDS1_B_TX2_N	294			
23	GND		PWR		
24	LVDS1_B_TX2_P	296			
25	LVDS1_A_CLK_P	248			
26	GND		PWR		
27	LVDS1_A_CLK_N	246			
28	LVDS1_B_TX3_N	300			
29	GND		PWR		
30	LVDS1_B_TX3_P	302			
31	LVDS1_SEL_1	JP2	PWR		
32	LVDS1_3.3V_SW		PWR	+3.3V	
33	LVDS1_SEL_2	JP3	PWR		
34	LVDS1_5V_SW		PWR	+5V	
35	PWM_BKL1	239	O		
36	I2C2_DDC_SDA_LVDS <a href="#">(Refer Section 3.9.8)</a>		IO		
37	BKL1_ON	286			
38	I2C2_DDC_SCL_LVDS <a href="#">(Refer Section 3.9.8)</a>		O		
39	LVDS1_12V_SW_UNREG		PWR	+12V	
40	LVDS1_12V_SW_UNREG		PWR	+12V	

Please note that LVDS1\_12V\_SW\_UNREG is not regulated power supply. It will be the same voltage that has been provided on the connectors X17. Use only 12V+/-10% power supply with connector X17.

Toradex provides a range of different tools and utilities to help with the easy configuration of different LCD panels. For details please refer to: <http://developer.toradex.com>

By using the jumpers JP2 and JP3 it is possible to configure the values of the pins 31 and 33 of the connector X13. The following table shows how these voltages can be changed.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper Position JP2, JP3	Description
1 - 2	LVDS1_SEL_1 / LVDS1_SEL_2 set to 3.3V_SW
2 - 3	LVDS1_SEL_1 / LVDS1_SEL_2 set to 5V_SW
OPEN	LVDS1_SEL_1 / LVDS1_SEL_2 set to GND

### 3.9.3 Generic Touch-Screen (X16)

Connector type: 2x3 Pin Header Male, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR		
2	AN1_TSMY	321	O	+3.3V	
3	AN1_TSMX	317	O	+3.3V	
4	AN1_TSPY	319	O	+3.3V	
5	AN1_TSPX	315	O	+3.3V	
6	AN1_TSWIP	311 (via R89)	O	+3.3V	

### 3.9.4 Generic Display (X20)

Connector type: 2x25 Pin Header Male, 2.54 mm

Pin	Signal Name	Color Mapping 18bpp	MXM3 Number	I/O Type	Voltage	Pull-up/ Pull-down
1	GND			PWR		
2	LCD1_PCLK		243	OI	+3.3V	
3	LCD1_HSYNC		247	O	+3.3V	
4	LCD1_VSYNC		245	O	+3.3V	
5	GND			PWR	+3.3V	
6	LCD1_R2	RED 0	255	O	+3.3V	
7	LCD1_R3	RED 1	257	O	+3.3V	
8	LCD1_R4	RED 2	259	O	+3.3V	
9	LCD1_R5	RED 3	261	O	+3.3V	
10	LCD1_R6	RED 4	263	O	+3.3V	
11	LCD1_R7	RED 5	265	O	+3.3V	
12	GND			PWR		
13	LCD1_G2	GREEN 0	273	O	+3.3V	
14	LCD1_G3	GREEN 1	275	O	+3.3V	
15	LCD1_G4	GREEN 2	277	O	+3.3V	
16	LCD1_G5	GREEN 3	279	O	+3.3V	
17	LCD1_G6	GREEN 4	281	O	+3.3V	
18	LCD1_G7	GREEN 5	283	O	+3.3V	
19	GND			PWR		
20	LCD1_B2	BLUE 0	291	O	+3.3V	
21	LCD1_B3	BLUE 1	293	O	+3.3V	
22	LCD1_B4	BLUE 2	295	O	+3.3V	

Pin	Signal Name	Color Mapping 18bpp	MXM3 Number	I/O Type	Voltage	Pull-up/ Pull-down
23	LCD1_B5	BLUE 3	297	O	+3.3V	
24	LCD1_B6	BLUE 4	299	O	+3.3V	
25	LCD1_B7	BLUE 5	301	O	+3.3V	
26	GND			PWR		
27	LCD1_DE		249	I	+3.3V	
28	+V_DISPLAY			PWR	JP14 selectable	
29	+V_DISPLAY			PWR	JP14 selectable	
30	I2C1_SCL_GEN		209 (via R273)	IO		
31	I2C1_SDA_GEN		211 (via R274)	IO		
32	GND			PWR		
33	AN1_TSMY		321	O		
34	AN1_TSMX		317	O		
35	AN1_TSPY		319	O		
36	AN1_TSPX		315	O		
37	BKL1_ON		286	O	+3.3V	100k to GND
38	GND_DISPINV			PWR		
39	5V_DISPINV			PWR	+5V	
40	GND_DISPINV			PWR		
41	GND			PWR		
42	GND			PWR		
43	LCD1_R0		251	O	+3.3V	
44	LCD1_R1		253	O	+3.3V	
45	LCD1_G0		269	O	+3.3V	
46	LCD1_G1		271	O	+3.3V	
47	LCD1_B0		287	O	+3.3V	
48	LCD1_B1		289	O	+3.3V	
49	3.3V_DISP			PWR		
50	AN1_TSWIP - GPIO6			O	JP26 selectable	

By using the jumpers JP14, it is possible to configure the values of the pins 28 and 29 of the connector X20. The following table shows how these voltages can be changed.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	+V_DISPLAY set to 3.3V_SW
2 - 3	+V_DISPLAY set to 5V_SW

By using the jumper JP26 it is possible to configure the function of pin 50 on the connector X20 in order to use this pin to implement a multi touch interface. The following table shows the JP26 connection possibilities.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	Connector pin 50 connected to AN1_TSWIP signal
2 - 3	Connector pin 50 connected to GPIO6 (MXM pin 13) signal

### 3.9.5 LCD Inverter (X23)

Connector type: 1x5 Pin Header Male, 2.54 mm, Not Assembled

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	5V_DISPINV		PWR	+5V	
2	GND_DISPINV		PWR		
3	BKL1_ON	286	O	+3.3V	100K to GND
4	GND_DISPINV		PWR		
5	NC				

### 3.9.6 VGA (X24)

Connector type: DSUB15 Female, AUK HDR15SN-H

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	VGA1_R_C	208	O	+3.3V	
2	VGA1_G_C	210	O	+3.3V	
3	VGA1_B_C	212	O	+3.3V	
4	NC				
5	GND		PWR		
6	GND		PWR		
7	GND		PWR		
8	GND		PWR		
9	GND - VDISP		PWR	JP24 selectable	
10	GND		PWR		
11	NC				
12	I2C2_DDC_SDA_VGA (Refer Section 3.9.8)		VGA EDID Data		
13	VGA1_HSYNC_C		O	+5V	
14	VGA1_VSYNC_C		O	+5V	
15	I2C2_DDC_SCL_VGA (Refer Section 3.9.8)		VGA EDID CLK		

By using the jumpers JP24, it is possible to configure the values of the pins 9 of the connector X24. The following table shows how these voltages can be changed.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	GND - VDISP set to GND
2 - 3	GND - VDISP set to V_DISP (5V_SW)

### 3.9.7 Unified Interface Display (X31)

Apalis Evaluation Board provides a digital RGB interface port (18-bpp) to interface with the LCD panels using a 40-way, Unified Interface Display connector (X15). It also includes a 4-wire resistive touch screen interface on the same FFC connector.

The Unified Interface Display connector (X31) is compatible with the EDT Unified TFT Interface. A variety of LCD panels with integrated touch support for evaluation purposes are available at the Toradex Webshop.

- <http://developer.toradex.com/products/edt-display>

For customers looking for capacitive touch display solution, Apalis evaluation board is fully compatible with the Toradex Capacitive Multi-Touch Display solution. Please refer to the following developer page link for more details:

- <http://developer.toradex.com/products/capacitive-multi-touch-display>

For more TFT display solutions, refer to the following developer webpage articles:

- <http://developer.toradex.com/knowledge-base/supported-displays>
- <http://developer.toradex.com/knowledge-base/tianma-rgb-display-adapter-board>
- <http://developer.toradex.com/knowledge-base/generic-rgb-display-adapter-board>

Connector type: Hirose FH12-40S-0.5SV(55)

Pin	Signal Name	Color Mapping 18bpp	MXM3 Number	I/O Type	Voltage	Pull-up/ Pull-down
1	GND			PWR		
2	GND			PWR		
3	3.3V_SW			PWR	+3.3V	
4	3.3V_SW			PWR	+3.3V	
5	BKL1_ON		286	O	+3.3V	
6	PWM_BKL1		239	O	+3.3V	
7	RESET_MOCI_EDT#		26 (via R82)	O	+3.3V	
8	LCD1_B7	BLUE 5	301	O	+3.3V	
9	LCD1_B6	BLUE 4	299	O	+3.3V	
10	LCD1_B5	BLUE 3	297	O	+3.3V	
11	LCD1_B4	BLUE 2	295	O	+3.3V	
12	LCD1_B3	BLUE 1	293	O	+3.3V	
13	LCD1_B2	BLUE 0	291	O	+3.3V	
14	GND			PWR		
15	LCD1_G7	GREEN 5	283	O	+3.3V	
16	LCD1_G6	GREEN 4	281	O	+3.3V	
17	LCD1_G5	GREEN 3	279	O	+3.3V	
18	LCD1_G4	GREEN 2	277	O	+3.3V	
19	LCD1_G3	GREEN 1	275	O	+3.3V	
20	LCD1_G2	GREEN 0	273	O	+3.3V	
21	GND			PWR		
22	LCD1_R7	RED 5	265	O	+3.3V	
23	LCD1_R6	RED 4	263	O	+3.3V	
24	LCD1_R5	RED 3	261	O	+3.3V	
25	LCD1_R4	RED 2	259	O	+3.3V	
26	LCD1_R3	RED 1	257	O	+3.3V	
27	LCD1_R2	RED 0	255	O	+3.3V	

Pin	Signal Name	Color Mapping 18bpp	MXM3 Number	I/O Type	Voltage	Pull-up/ Pull-down
28	LCD1_PCLK		243	O	+3.3V	
29	GND			PWR		
30	LCD1_HSYNC		247	O	+3.3V	
31	LCD1_VSYNC		245	O	+3.3V	
32	LCD1_DE			O	+3.3V	
33	LCD1_CONF1: Connected to 3.3V or GND via assembly option. The default assembly is GND			O	+3.3V/GND	
34	LCD1_CONF2: Connected to 3.3V or GND via assembly option. The default assembly is GND			O	+3.3V/GND	
35	GND			PWR		
36	3.3V_SW			PWR	+3.3V	
37	AN1_TSPY		319	O	+3.3V	
38	AN1_TSMX		317	O	+3.3V	
39	AN1_TSMY		321	O	+3.3V	
40	AN1_TSPX		315	O	+3.3V	

The following table describes the assembly options available on the Apalis Evaluation Board with respect to the Unified Interface Display:

Solution Selected	Assembly Options	Assembled Components on Apalis Eval. Board V1.1	PCB Side
Unified Interface Display , Rotate display	Assemble appropriate 0R resistors R83, R84, R85, and R86. Refer to LCD TFT datasheet for configuration details.	R85, R86	Top

Please refer to Apalis Evaluation Board assembly drawing for the position of the resistors available on the Toradex Developer Website: <http://developer.toradex.com>

### 3.9.8 Extended Display Identification Data (EDID)

The I2C2 interface of the Apalis module is used as EDID interface in order to allow the module to query the video capabilities of the connected display.

Through the connectors X39 and X40, it is possible to configure which display interface is connected to the EDID port of the Apalis module.

Since X39 and X40 are standard 2.54mm pitch header, it is possible, using shunt jumpers, to select one or more interfaces that will be connected to the EDID port of the module.

The following table describes how the connectors X39 and X40 should be configured when using different display interfaces.

Connector type: 2x3 Pin Header Male, 2.54 mm

Jumper position X39, X40	Description
1 - 2	VGA (X24)
3 - 4	DVI-I (X11)
5 - 6	LVDS (X13)

### 3.10 Audio

The Apalis Evaluation Board offers two audio interfaces. The analogue interface which is provided by the Apalis Module is available on connector X26.

The stacked connector offers standard jacks for active loudspeakers or headphones, for line-in and microphone input.

The digital interface which uses the on-board HD Audio Codec ALC898 from Realtek features a 7.1 channel output through the audio jack connector X27 and the headers X41 and X42. Please consult the Realtek ALC898 datasheet for more information.

Before using the digital audio interface on the Apalis Evaluation Board V1.0, please check the NOTE 7 in the Apalis Schematic file. This document is available on the Toradex developer website, in the Carrier Board Design page.

#### 3.10.1 3xAudio Jack (X26)

Connector type: Stacked 3 x 3.5mm Jack, Foxconn JA3333L-D11P-4F

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	AGND		PWR		
2	AAP1_MICIN	306	I	+3.3V	
3	NC				
4	NC				
5	AUDIO_AVCC		PWR	+3.3V	
22	AAP1_HP_AC_L	316	O	+3.3V	
23	NC				
24	NC				
25	AAP1_HP_AC_R	318	O	+3.3V	
32	AAP1_LIN_L	310	I	+3.3V	
33	NC				
34	NC				
35	AAP1_LIN_R	312	I	+3.3V	

#### 3.10.2 3x HDA Audio Jack (X27)

Connector type: Stacked 3 x 3.5mm Jack, Foxconn JA3333L-D11P-4F

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	AGND2		PWR		
2	DAP1_HDA_MIC1_C_L		I	+3.3V	
3	DAP1_HDA_MIC1-JD		I		
4	AGND2		PWR		
5	DAP1_HDA_MIC1_C_R		I	+3.3V	
22	DAP1_HDA_FRONT_C_L		O	+3.3V	
23	DAP1_HDA_FRONT-JD		I		
24	AGND2		PWR		
25	DAP1_HDA_FRONT_C_R		O	+3.3V	
32	DAP1_HDA_LINE1_C_L		I	+3.3V	
33	DAP1_HDA_LINE1-JD		I		
34	AGND2		PWR		
35	DAP1_HDA_LINE1_C_R		I	+3.3V	

### 3.10.3 3x HDA Front Panel (X41)

Connector type: 2x5 Pin Header Male, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	DAP1_HDA_MIC2_H_L		I	+3.3V	
2	AGND2		PWR		
3	DAP1_HDA_MIC2_H_R		I	+3.3V	
4	DAP1_F_HEAD_PRES#		I		
5	DAP1_HDA_LINE2_H_R		I	+3.3V	
6	DAP1_HDA_MIC2-JD		I		
7	AGND2		PWR		
8	NC		Not connected		
9	DAP1_HDA_LINE2_H_L		I	+3.3V	
10	DAP1_HDA_LINE2-JD		I		

### 3.10.4 3x HDA Surround (X42)

Connector type: 2x5 Pin Header Male, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	DAP1_HDA_LOW_FREQ_H		O	+3.3V	
2	AGND2		PWR		
3	DAP1_HDA_CENTER_H		O	+3.3V	
4	DAP1_HDA_SIDESURROUND_H_R		O	+3.3V	
5	DAP1_HDA_SIDESURROUND_H_L		O	+3.3V	
6	DAP1_HDA_SURROUND_H_R		O	+3.3V	
7	DAP1_HDA_SURROUND_H_L		O	+3.3V	
8	DAP1_HDA_CEN-JD		I		
9	DAP1_HDA_SURR-JD		I		
10	DAP1_HDA_SIDESURR-JD		I		

### 3.10.5 SPDIF Out

The Apalis Evaluation Board features an S/PDIF Optical Transmitter which can be optionally connected to the Apalis S/PDIF output or to the HDA Codec S/PDIF output, by changing the position of the jumper JP25:

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper position	Description
1 - 2	Apalis S/PDIF Out
2 - 3	HDA S/PDIF Out

#### 3.10.5.1 S/PDIF Out (X21)

Connector type: PLT133/T9 Transmitter,

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND				
2	5V_SW				
3	SPDIF1_OUT_OPT				



### 3.11 Mezzanine Type Specific

The type specific mezzanine connector provides access to the type specific interfaces on the Apalis module. These interfaces differ between different Apalis modules. Different type specific mezzanine boards are available for each Apalis module and are connected to this interface to provide access to the type specific features. Customers are free to develop their own type specific mezzanine board for prototyping and development purposes. Please refer to the datasheets for the individual type specific mezzanine boards and respective Apalis module for more information.

#### 3.11.1 Mezzanine Type Specific (X38)

Connector type: Samtec QSH-060-01-L-D-A

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR		
2	VSTB		PWR	+5V	
3	TS_DIFF18_P	163	IO		
4	GND		PWR		
5	TS_DIFF18_N	161	IO		
6	SPI2_CLK	235	O		
7	TS6	159	IO		
8	SPI2_CS	233	O		
9	TS_DIFF17_P	157	IO		
10	SPI2_MOSI	231	O		
11	TS_DIFF17_N	155	IO		
12	SPI2_MISO	229	I		
13	GND		PWR		
14	SPI1_CS	227	O		
15	TS_DIFF16_P	151	IO		
16	SPI1_MOSI	225	O		
17	TS_DIFF16_N	149	IO		
18	SPI1_MISO	223	I		
19	GND		PWR		
20	SPI1_CLK	221	O		
21	TS_DIFF15_P	145	IO		
22	GND		PWR		
23	TS_DIFF15_N	143	IO		
24	CAM_MEZ_PIN24	(X56, pin 9)	I		
25	GND		PWR		
26	CAM_MEZ_PIN26	(X56, pin 10)	I		
27	TS_DIFF14_P	139	IO		
28	CAM_MEZ_PIN28	(X56, pin 11)	I		
29	TS_DIFF14_N	137	IO		
30	CAM_MEZ_PIN30	(X56, pin 12)	I		
31	GND		PWR		
32	GND		PWR		
33	TS5	135	IO		
34	CAM1_MCLK	193			
35	TS_DIFF13_P	133	IO		
36	GND		PWR		
37	TS_DIFF13_N	131	IO		
38	I2C_CAM1_SCL	203	O		+1.8K to 3.3V_SW

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
39	GND		PWR		
40	GND		PWR		
41	TS_DIFF12_P	127	IO		
42	I2C_CAM1_SDA	201	IO		+1.8K to 3.3V_SW
43	TS_DIFF12_N	125	IO		
44	5V_SW		PWR	+5V	
45	GND		PWR		
46	5V_SW		PWR	+5V	
47	TS4	123	IO		
48	5V_SW		PWR	+5V	
49	TS_DIFF11_P	121	IO		
50	5V_SW		PWR	+5V	
51	TS_DIFF11_N	119	IO		
52	5V_SW		PWR	+5V	
53	GND		PWR		
54	NC				
55	TS_DIFF10_P	115	IO		
56	V_SUPPLY_FILT_F		PWR	PWR_IN	
57	TS_DIFF10_N	113	IO		
58	V_SUPPLY_FILT_F		PWR	PWR_IN	
59	GND		PWR		
60	V_SUPPLY_FILT_F		PWR	PWR_IN	
61	TS_DIFF9_P	109	IO		
62	3.3V		PWR	+3.3V	
63	TS_DIFF9_N	107	IO		
64	3.3V		PWR	+3.3V	
65	GND		PWR		
66	3.3V		PWR	+3.3V	
67	TS_DIFF8_P	103	IO		
68	3.3V		PWR	+3.3V	
69	TS_DIFF8_N	101	IO		
70	NC				
71	GND		PWR		
72	3.3V_SW		PWR	+3.3V	
73	TS3	99	IO		
74	3.3V_SW		PWR	+3.3V	
75	TS_DIFF7_P	97	IO		
76	3.3V_SW		PWR	+3.3V	
77	TS_DIFF7_N	95	IO		
78	3.3V_SW		PWR	+3.3V	
79	GND		PWR		
80	NC				
81	TS_DIFF6_P	91	IO		
82	12V_SW_UNREG_F		PWR	+12V	
83	TS_DIFF6_N	89	IO		
84	12V_SW_UNREG_F		PWR	+12V	
85	GND		PWR		

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
86	12V_SW_UNREG_F		PWR	+12V	
87	TS2	87	IO		
88	GND		PWR		
89	TS_DIFF5_P	85	IO		
90	I2C1_SCL	211	O		
91	TS_DIFF5_N	83	IO		
92	I2C1_SDA	209	IO		
93	GND		PWR		
94	UART4_TXD	138	O		
95	TS_DIFF4_P	79	IO		
96	UART4_RXD	140	I		
97	TS_DIFF4_N	77	IO		
98	WAKE1_MICO#	37			
99	GND		PWR		
100	POWER_ENABLE_MOCI	24			
101	TS_DIFF3_P	73	IO		
102	RESET_MOCI#	26			
103	TS_DIFF3_N	71	IO		
104	RESET_MICO#	28			
105	GND		PWR		
106	GPIO1	1	IO		
107	TS_DIFF2_P	67	IO		
108	GPIO2	3	IO		
109	TS_DIFF2_N	65	IO		
110	GPIO3	5	IO		
111	GND		PWR		
112	GPIO4	7	IO		
113	TS1	63	IO		
114	GPIO5	11	IO		
115	TS_DIFF1_P	61	IO		
116	GPIO6	13	IO		
117	TS_DIFF1_N	59	IO		
118	GPIO7	15	IO		
119	GND		PWR		
120	GPIO8	17	IO		
121	GND		PWR		

### 3.12 Parallel Camera Interface

The Parallel Camera Interface on connector X22 is intended for applications requiring image capture capability from CMOS or CDD image sensors. This interface supports a wide variety of operating modes, data widths, formats, and clocking schemes. For details please see the relevant Apalis module datasheet.

In order provide compatibility with the variety of different parallel camera interface standards, the data signals of this interface have been routed through a reconfigurable jumper area.

Please note that only 8 of the 12 data bit are directly connected to the module. The other 4 data bit need to be connected through the Type Specific connector.

#### 3.12.1 Parallel Camera (X22)

Connector type: 2x12 Pin Header Male, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	+3.3		PWR	+3.3V	
2	+3.3		PWR	+3.3V	
3	CAM1_MCLK	193	IO	+3.3V	
4	CAM1_PCLK	191	IO	+3.3V	
5	CAM1_HSYNC	197	IO	+3.3V	
6	CAM1_VSYNC	195	IO	+3.3V	
7	CAM1_D0	187	IO	+3.3V	
8	CAM1_D1	185	IO	+3.3V	
9	CAM1_D2	183	IO	+3.3V	
10	CAM1_D3	181	IO	+3.3V	
11	CAM1_D4	179	IO	+3.3V	
12	CAM1_D5	177	IO	+3.3V	
13	CAM1_D6	175	IO	+3.3V	
14	CAM1_D7	173	IO	+3.3V	
15	I2C_CAM1_SCL	203	IO	+3.3V	1.8K to 3.3_SW
16	I2C_CAM1_SDA	201	IO	+3.3V	1.8K to 3.3_SW
17	CAM1_D8	(X38, pin 24)	IO	+3.3V	
18	CAM1_D9	(X38, pin 26)	IO	+3.3V	
19	GND		PWR		
20	GND		PWR		
21	CAM1_D10	(X38, pin 28)	IO	+3.3V	
22	CAM1_D11	(X38, pin 30)	IO	+3.3V	
23	+3.3V		PWR	+3.3V	
24	+5V		PWR	+5V	

#### 3.12.2 Camera Jumper Array (X57)

Connector type: 2x12 Pin Header Male, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	MXM3_187	187	IO	+3.3V	
A2	MXM3_185	185	IO	+3.3V	
A3	MXM3_183	183	IO	+3.3V	
A4	MXM3_181	181	IO	+3.3V	
A5	MXM3_179	179	IO	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A6	MXM3_177	177	IO	+3.3V	
A7	MXM3_175	175	IO	+3.3V	
A8	MXM3_173	173	IO	+3.3V	
A9	MEZZANINE_24	(X38, pin 24)	IO	+3.3V	
A10	MEZZANINE_26	(X38, pin 26)	IO	+3.3V	
A11	MEZZANINE_28	(X38, pin 28)	IO	+3.3V	
A12	MEZZANINE_30	(X38, pin 30)	IO	+3.3V	
B1	X22 pin 7	(X22, pin 7)	IO	+3.3V	
B2	X22 pin 8	(X22, pin 8)	IO	+3.3V	
B3	X22 pin 9	(X22, pin 9)	IO	+3.3V	
B4	X22 pin 10	(X22, pin 10)	IO	+3.3V	
B5	X22 pin 11	(X22, pin 11)	IO	+3.3V	
B6	X22 pin 12	(X22, pin 12)	IO	+3.3V	
B7	X22 pin 13	(X22, pin 13)	IO	+3.3V	
B8	X22 pin 14	(X22, pin 14)	IO	+3.3V	
B9	X22 pin 17	(X22, pin 17)	IO	+3.3V	
B10	X22 pin 18	(X22, pin 18)	IO	+3.3V	
B11	X22 pin 21	(X22, pin 21)	IO	+3.3V	
B12	X22 pin 22	(X22, pin 22)	IO	+3.3V	

### 3.12.3 Camera Function Tap (X58)

Connector type: 1x12 Pin Header Female, 2.54 mm

Pin-out identical to X57 Pins B1 to B12

### 3.12.4 Camera MXM3 Breakout Area (X56)

Connector type: 1x12 Pin Header Female, 2.54 mm

Pin-out identical to X57 Pins A1 to A12

### 3.13 Digital and Analog I/O

#### 3.13.1 Communication Interface

##### 3.13.1.1 CAN

The Apalis Evaluation Board uses the Microchip MCP2551T-I/SN CAN transceiver to implement two CAN 2.0b interfaces in conjunction with the two CAN interfaces on the Apalis module. The CAN ports are electrically isolated from the system power supply.

The CAN interfaces are available on connector X32.

The CAN connector provides the ability to optionally connect the isolated power supplies to connector pins in order to provide power to external CAN nodes.

Jumper assembled	X2 pin number	Power on X2
JP15	U6	CAN1_PGND
JP16	U9	CAN1_PW
JP17	L6	CAN2_PGND
JP18	L9	CAN2_PW

##### 3.13.1.1.1 CAN1 (X32 - Top)

Connector type: Stacked DSUB9 Male, NorComp 178-009-613R571

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
U1	NC				
U2	CAN1_L		IO	+5V	
U3	CAN1_GND		PWR		
U4	NC				
U5	NC				
U6	CAN1_PGND		PWR		
U7	CAN1_H		IO	+5V	
U8	NC				
U9	CAN1_V+		PWR	+5V	

##### 3.13.1.1.2 CAN2 (X32 - Bottom)

Connector type: Stacked DSUB9 Male, NorComp 178-009-613R571

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
U1	NC				
U2	CAN2_L		IO	+5V	
U3	CAN2_GND		PWR		
U4	NC				
U5	NC				
U6	CAN2_PGND		PWR		
U7	CAN2_H		IO	+5V	
U8	NC				
U9	CAN2_V+		PWR	+5V	

### 3.13.1.2 UART Interfaces

The Apalis Evaluation Board features 4 UART interfaces that are connected to the following connectors:

- UART 1 to the connector X28 (Bottom) through an RS232 transceiver. It can be also optionally connected to a built in USB to Serial transceiver;
- UART2 to the connector X28 (Top) through an RS232 transceiver. It can be also optionally connected to a RS422/485 transceiver.
- UART 3 to an IrDA transceiver X30
- UART 4 to the mezzanine connector X38. Refer [Section 3.11](#).

#### 3.13.1.2.1 RS232 (X28 – Top and Bottom)

Connector type: Stacked DSUB9 Male, NorComp 178-009-613R571

Pin	Signal Name	Description	I/O Type	Voltage	Remarks
U1	UART2_RS232_U_DCD		I		A dedicated pin is not available on the Apalis standard pin-out. Signal is only connected to test-point (TP15).
U2	UART2_RS232_U_RXD		I		
U3	UART2_RS232_U_TXD		O		
U4	UART2_RS232_U_DTR		O		A dedicated pin is not available on the Apalis standard pin-out. Signal is pulled-up to 3.3V using 100K resistor.
U5	GND		PWR		
U6	UART2_RS232_U_DSR		I		A dedicated pin is not available on the Apalis standard pin-out. Signal is only connected to test-point (TP17).
U7	UART2_RS232_U_RTS		O		
U8	UART2_RS232_U_CTS		I		
U9	UART2_RS232_U_RI		I		A dedicated pin is not available on the Apalis standard pin-out. Signal is only connected to test-point (TP16).
L1	UART1_RS232_L_DCD		I		
L2	UART1_RS232_L_RXD		I		
L3	UART1_RS232_L_TXD		O		
L4	UART1_RS232_L_DTR		O		
L5	GND		PWR		
L6	UART1_RS232_L_DSR		I		
L7	UART1_RS232_L_RTS		O		
L8	UART1_RS232_L_CTS		I		
L9	UART1_RS232_L_RI		I		

By changing the position of the Jumpers JP10, and JP12, it is possible to route the signals UART1\_TXD and UART1\_RXD to the connector X28 (Bottom) instead of the connector X29 and vice versa.

Connector type: 1x3 Pin Header Male, 2.54 mm

JP10, JP12	Description
1 - 2	UART1_TXD / UART1_RXD are routed to RS232 Interface. Connector X28 (Bottom) will be active.
2 - 3	UART1_TXD / UART1_RXD are routed to USB to Serial Interface. Connector X29 will be active.

### 3.13.1.2.2 USB to Serial Connector (X29)

The Apalis Evaluation Board features a built in USB to Serial UART converter (FTDI FT232RL) which can be used to interface with the serial debug Full Function (FF) UART via the USB Type B connector X29.

Connector type: USB Type B, FCI 61729-0010BLF

Pin	Signal Name	Description	I/O Type	Voltage	Remarks
1	5V_USB_D		PWR	+5V	
2	USBD_N		I/O		
3	USBD_P		I/O		
4	GND		PWR		
S1/S2	SHIELD		PWR		

Please note that the UART-1 signal are shared with RS232 interface. By changing the position of the Jumpers JP10 and JP12, it is possible to route the signals UART1\_TXD and UART1\_RXD to the connector X29 instead of the connector X28 (Bottom) and vice versa as mentioned in [Section 3.13.1.2.1, RS232 \(X28- Top and Bottom\)](#).

### 3.13.1.2.3 RS422/485 (X55)

Connector type: DSUB9 Male, Tyco 1734351-1

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR		
2	NC				
3	NC				
4	RXD+		IO		
5	RXD-		IO		
6	NC				
7	NC				
8	TXD+		IO		
9	TXD-		IO		

The jumpers JP5, JP6, JP7, JP8, JP9 and JP11 provide hardware configuration for this interface:

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper	Status	Function
JP7	CLOSED	ECHO disabled (the sender cannot read the message just sent)
JP5, JP8	CLOSED	Insert the 120ohm bus termination (for RS422)
JP6, JP9	OPEN	Full Duplex Configuration
JP11	CLOSED	The upper RS232 is disable



### 3.13.2 Digital Interface

#### 3.13.2.1 Switches / LEDs

The Apalis Evaluation Board features eight LEDs (four green and four red), four switches and four buttons.

Interfaces to and from these devices are available on connector X34. They can be directly connected to the GPIO breakout connectors or to additional custom specific hardware.

Please note that the buttons and switches are not de-bounced.

##### 3.13.2.1.1 LED/Switches (X34)

Connector type: 2x10 Pin Header Female, 2.54 mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	GND		PWR	+3.3V	
2	+3.3V		PWR	+3.3V	
3	SWITCH_1		O	+3.3V	100K to GND
4	LED_1		I	+3.3V	100K to GND
5	SWITCH_2		O	+3.3V	100K to GND
6	LED_2		I	+3.3V	100K to GND
7	SWITCH_3		O	+3.3V	100K to GND
8	LED_3		I	+3.3V	100K to GND
9	SWITCH_4		O	+3.3V	100K to GND
10	LED_4		I	+3.3V	100K to GND
11	BUTTON_1		O	+3.3V	10K to GND
12	LED_5		I	+3.3V	100K to GND
13	BUTTON_2		O	+3.3V	10K to GND
14	LED_6		I	+3.3V	100K to GND
15	BUTTON_3		O	+3.3V	10K to GND
16	LED_7		I	+3.3V	100K to GND
17	BUTTON_4		O	+3.3V	10K to GND
18	LED_8		I	+3.3V	100K to GND
19	GND		PWR	+3.3V	
20	+3.3V		PWR	+3.3V	+3.3V

### 3.13.3 Analog Interface

The Analog outputs are implemented as Pulse Width Modulate (PWM) signals feeding discrete RC filters with a time constant of 3.3ms.

The Analog inputs are directly connected to the GPIO breakout area.

#### 3.13.3.1 Analog IO (X14)

Type: 2x8Pin Header Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	AN1_ADC0	305	I	+3.3V	
2	AGND		PWR		
3	AN1_ADC1	307	I	+3.3V	
4	AGND		PWR		
5	AN1_ADC2	309	I	+3.3V	
6	AGND		PWR		
7	AN1_TSWIP_ADC3	311	I	+3.3V	
8	AGND		PWR		
9	ANALOG_OUT4	8	O	+3.3V	RC-filter (3.3ms)
10	GND		PWR		
11	ANALOG_OUT3	6	O	+3.3V	RC-filter (3.3ms)
12	GND		PWR		
13	ANALOG_OUT2	4	O	+3.3V	RC-filter (3.3ms)
14	GND		PWR		
15	ANALOG_OUT1	2	O	+3.3V	
16	GND		PWR		

### 3.14 Real-Time Clock (RTC)

The Apalis Evaluation Board uses the STMicroelectronics, M41T0M6 chip as external RTC. A battery holder (BAT1) is available on the Apalis Evaluation Board for RTC power backup.

Jumper (JP22) is used to selection of the internal RTC or external RTC. Backup battery power can be diverted to either internal RTC or external RTC based on the jumper JP22 setting.

Connector type: 1x3 Pin Header Male, 2.54 mm Pitch

Jumper position	Description
1 - 2	Internal RTC (available on Apalis Module)
2 - 3	External RTC (available on Evaluation Board)

For more details about internal RTC, please refer Apalis computer-on-module datasheet.

#### 3.14.1 Battery Holder (BAT1)

A 20 mm (diameter) coin cell/battery should be used with the Battery Holder (BAT1). Coin cell can be used to provide power backup to the external RTC circuits when external power supply is not available.

Supported batteries: CR2032 or similar coin cells..

Connector type: Renata HU2032-LF

Pin	Description	Voltage
1	VCC_BATT	+3.0V
2	GND	

### 3.15 JTAG

The Apalis Evaluation Board provides a JTAG interface to the JTAG port available on Apalis modules.

Connector X33 provides an interface to an external JTAG device via a standard 2.54mm shrouded and keyed header.

In addition, the Apalis evaluation Board features a spring loaded Pogo-pin connector X59 which is positioned directly underneath the installed Apalis module, allowing direct connection with the Apalis module JTAG test points.

Before using the JTAG interface on the Apalis Evaluation Board V1.0, please check the NOTE 9 in the Apalis Schematic file. This document is available on the Toradex developer website, in the Carrier Board Design page.

#### 3.15.1 JTAG to Host (X33)

Type: 2x10Pin Shrouded and Keyed Header Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	VREF_JTAG		PWR		
2	VREF_JTAG		PWR		
3	JTAG_TRST#		I	+3.3V	
4	GND		PWR		
5	JTAG_TDI		I	+3.3V	
6	GND		PWR		
7	JTAG_TMS		I	+3.3V	
8	GND		PWR		
9	JTAG_TCK		I	+3.3V	
10	GND		PWR		
11	JTAG_RTCK_R		O	+3.3V	
12	GND		PWR		
13	JTAG_TDO_R		I	+3.3V	
14	GND		PWR		
15	JTAG_SYSRESET#		I	+3.3V	
16	GND		PWR		
17	NC				
18	GND		PWR		
19	NC				
20	GND		PWR		

#### 3.15.2 JTAG to Apalis (X59)

Type: Mill-Max 821-22-007-10-000101

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
1	JTAG_TDI		I	+3.3V	
2	JTAG_TDO		I	+3.3V	
3	JTAG_TCK		I	+3.3V	
4	JTAG_TRST#		O	+3.3V	
5	JTAG_TMS		I	+3.3V	
6	JTAG_RTCK		O-	+3.3V-	
7	VREF_JTAG		I		

### 3.16 GPIO Usage

The GPIO breakout connectors offer the flexibility to map the GPIOs of the Apalis module to either the on-board function or to external hardware.

The factory setting is a straight through jumper setting, meaning that the X3-A row is connected straight to the X3-B row. This is also true for the connectors X6 and X9.

To allowing easy measurement, probing, and re-routing, all signals residing on the male header are also available on a female connector in parallel.

To map MXM3 pin with the corresponding GPIO numbers which are specific to individual Apalis modules, please refer to the applicable Apalis module datasheet.

#### 3.16.1 GPIO 1 Male (X3 Row A)

Type: 2x40Pin Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	+3.3V_SW		PWR	+3.3V	
A2	MXM3_35	35	IO	+3.3V	
A3	MXM3_17	17	IO		
A4	MXM3_15	15	IO	+3.3V	
A5	MXM3_13	13	IO	+3.3V	
A6	MXM3_11	11	IO	+3.3V	
A7	MXM3_7	7	IO	+3.3V	
A8	MXM3_5	5	IO		
A9	MXM3_3	3	IO	+3.3V	
A10	MXM3_1	1	IO	+3.3V	
A11	GND		PWR		
A12	MXM3_8	8	IO	+3.3V	
A13	MXM3_6	6	IO	+3.3V	
A14	MXM3_4	4	IO	+3.3V	
A15	MXM3_2	2	IO	+3.3V	
A16	+3.3V_SW		PWR		
A17	MXM3_12	12	IO	+3.3V	
A18	MXM3_14	14	IO	+3.3V	
A19	MXM3_16	16	IO	+3.3V	
A20	MXM3_18	18	IO	+3.3V	
A21	GND		PWR		
A22	3.3V_SW		PWR		
A23	GND		PWR		
A24	MXM3_37	37	IO	+3.3V	
A25	MXM3_24	24	IO	+3.3V	
A26	MXM3_26	26	IO	+3.3V	
A27	MXM3_28	28	IO	+3.3V	
A28	GND		PWR		
A29	+3.3V_SW		PWR		
A30	GND		PWR		
A31	MXM3_84	84	IO	+3.3V	
A32	MXM3_96	96	IO	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A33	MXM3_262	262	IO	+3.3V	
A34	MXM3_274	274	IO	+3.3V	
A35	+3.3V_SW		PWR		
A36	MXM3_138	138	IO	+3.3V	
A37	MXM3_140	140	IO	+3.3V	
A38	MXM3_134	134	IO	+3.3V	
A39	MXM3_136	136	IO	+3.3V	
A40	GND		PWR		

### 3.16.2 Function 1 Male (X3 Row B)

Type: 2x40Pin Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B1	+3.3V_SW		PWR	+3.3V	
B2	SATA1_ACT#		IO	+3.3V	100k to +3.3V
B3	GPIO_8		IO		
B4	GPIO_7		IO	+3.3V	
B5	GPIO_6		IO	+3.3V	
B6	GPIO_5		IO	+3.3V	
B7	GPIO_4		IO	+3.3V	
B8	GPIO_3		IO		
B9	GPIO_2		IO	+3.3V	
B10	GPIO_1		IO	+3.3V	
B11	GND		PWR	+3.3V	
B12	PWM4		IO	+3.3V	
B13	PWM3		IO	+3.3V	
B14	PWM2		IO	+3.3V	
B15	PWM1		IO	+3.3V	
B16	+3.3V_SW		PWR		
B17	CAN1_RX		IO	+3.3V	
B18	CAN1_TX		IO	+3.3V	
B19	CAN2_RX		IO	+3.3V	
B20	CAN2_TX		IO	+3.3V	
B21	GND		PWR		
B22	3.3V_SW		PWR		
B23	GND		PWR		
B24	WAKE1_MICO#		IO	+3.3V	4.7k to +3.3V
B25	POWER_ENABLE_MOCI		IO	+3.3V	100k to GND
B26	RESET_MOCI#		IO	+3.3V	
B27	RESET_MICO#		IO	+3.3V	
B28	GND		PWR		
B29	+3.3V_SW		PWR		
B30	GND		PWR		
B31	USBH_EN		IO	+3.3V	100k to GND

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B32	USBH_OC#		IO	+3.3V	100k to +3.3V
B33	USBO1_OC#		IO	+3.3V	100k to +3.3V
B34	USBO1_EN		IO	+3.3V	
B35	+3.3V_SW		PWR		
B36	UART4_TXD		IO	+3.3V	
B37	UART4_RXD		IO	+3.3V	
B38	UART3_TXD		IO	+3.3V	
B39	UART3_RXD		IO	+3.3V	
B40	GND		PWR		

### 3.16.3 GPIO 1 Female (X2)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X3 Pins A1 to A40

### 3.16.4 Function 1 Female (X4)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X3 Pins B1 to B40

### 3.16.5 GPIO 2 Male (X6 Row B)

Type: 2x40Pin Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B1	MXM3_207	207	IO	+3.3V	
B2	MXM3_205	205	IO	+3.3V	
B3	MXM3_217	217	IO	+3.3V	
B4	MXM3_215	215	IO	+3.3V	
B5	MXM3_204	204	IO	+3.3V	
B6	MXM3_202	202	IO	+3.3V	
B7	MXM3_200	200	IO	+3.3V	
B8	MXM3_198	198	IO	+3.3V	
B9	MXM3_196	196	IO	+3.3V	
B10	MXM3_194	194	IO	+3.3V	
B11	MXM3_190	190	IO	+3.3V	
B12	MXM3_188	188	IO	+3.3V	
B13	MXM3_186	186	IO	+3.3V	
B14	MXM3_184	184	IO	+3.3V	
B15	MXM3_180	180	IO	+3.3V	
B16	MXM3_178	178	IO	+3.3V	
B17	MXM3_176	176	IO	+3.3V	
B18	MXM3_164	164	IO	+3.3V	
B19	MXM3_162	162	IO	+3.3V	
B20	MXM3_160	160	IO	+3.3V	
B21	MXM3_158	158	IO	+3.3V	
B22	MXM3_156	156	IO	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B23	MXM3_154	154	IO	+3.3V	
B24	MXM3_152	152	IO	+3.3V	
B25	MXM3_150	150	IO	+3.3V	
B26	MXM3_148	148	IO	+3.3V	
B27	MXM3_146	146	IO	+3.3V	
B28	MXM3_144	144	IO	+3.3V	
B29	MXM3_132	132	IO	+3.3V	
B30	MXM3_130	130	IO	+3.3V	
B31	MXM3_128	128	IO	+3.3V	
B32	MXM3_126	126	IO	+3.3V	
B33	MXM3_124	124	IO	+3.3V	
B34	MXM3_122	122	IO	+3.3V	
B35	MXM3_120	120	IO	+3.3V	
B36	MXM3_118	118	IO	+3.3V	
B37	MXM3_116	116	IO	+3.3V	
B38	MXM3_114	114	IO	+3.3V	
B39	MXM3_112	112	IO	+3.3V	
B40	MXM3_110	110	IO	+3.3V	

### 3.16.6 Function 2 Male (X6 Row A)

Type: 2x40Pin Male

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	I2C2_DDC_SCL		IO	+3.3V	1.8k to +3.3V
A2	I2C2_DDC_SDA		IO	+3.3V	1.8k to +3.3V
A3	SPDIF_IN		IO	+3.3V	
A4	SPDIF_OUT		IO	+3.3V	
A5	DAP1_SYNC		IO	+3.3V	
A6	DAP1_D_IN		IO	+3.3V	
A7	DAP1_BIT_CLK		IO	+3.3V	
A8	DAP1_RESET#		IO	+3.3V	
A9	DAP1_D_OUT		IO	+3.3V	
A10	DAP1_MCLK		IO	+3.3V	
A11	SD1_CD#		IO	+3.3V	10k to +3.3V
A12	SD1_D1		IO	+3.3V	68k to +3.3V
A13	SD1_D0		IO	+3.3V	68k to +3.3V
A14	SD1_CLK		IO	+3.3V	
A15	SD1_CMD		IO	+3.3V	33k to +3.3V
A16	SD1_D3		IO	+3.3V	68k to +3.3V
A17	SD1_D2		IO	+3.3V	68k to +3.3V
A18	MMC1_CD#		IO	+3.3V	10k to +3.3V
A19	MMC1_D1		IO	+3.3V	68k to +3.3V
A20	MMC1_D0		IO	+3.3V	68k to +3.3V
A21	MMC1_D7		IO	+3.3V	68k to +3.3V



Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A22	MMC1_D6		IO	+3.3V	68k to +3.3V
A23	MMC1_CLK		IO	+3.3V	
A24	MMC1_D5		IO	+3.3V	68k to +3.3V
A25	MMC1_CMD		IO	+3.3V	33k to +3.3V
A26	MMC1_D4		IO	+3.3V	68k to +3.3V
A27	MMC1_D3		IO	+3.3V	68k to +3.3V
A28	MMC1_D2		IO	+3.3V	68k to +3.3V
A29	UART2_RXD		IO	+3.3V	
A30	UART2_CTS		IO	+3.3V	
A31	UART2_RTS		IO	+3.3V	
A32	UART2_TXD		IO	+3.3V	
A33	UART1_DCD		IO	+3.3V	
A34	UART1_RI		IO	+3.3V	
A35	UART1_DSR		IO	+3.3V	
A36	UART1_RXD		IO	+3.3V	
A37	UART1_CTS		IO	+3.3V	
A38	UART1_RTS		IO	+3.3V	
A39	UART1_TXD		IO	+3.3V	
A40	UART1_DTR		IO	+3.3V	

### 3.16.7 GPIO 2 Female (X5)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X6 Pins B1 to B40

### 3.16.8 Function 2 Female (X7)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X6 Pins A1 to A40

### 3.16.9 GPIO 3 Male (X9 Row A)

Type: 2x40Pin Male, 2.54mm

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A1	MXM3_301	301	IO	+3.3V	
A2	MXM3_299	299	IO	+3.3V	
A3	MXM3_297	297	IO	+3.3V	
A4	MXM3_295	295	IO	+3.3V	
A5	MXM3_293	293	IO	+3.3V	
A6	MXM3_291	291	IO	+3.3V	
A7	MXM3_289	289	IO	+3.3V	
A8	MXM3_287	287	IO	+3.3V	
A9	MXM3_283	283	IO	+3.3V	
A10	MXM3_281	281	IO	+3.3V	
A11	MXM3_279	279	IO	+3.3V	
A12	MXM3_277	277	IO	+3.3V	
A13	MXM3_275	275	IO	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
A14	MXM3_273	273	IO	+3.3V	
A15	MXM3_271	271	IO	+3.3V	
A16	MXM3_269	269	IO	+3.3V	
A17	MXM3_265	265	IO	+3.3V	
A18	MXM3_263	263	IO	+3.3V	
A19	MXM3_261	261	IO	+3.3V	
A20	MXM3_259	259	IO	+3.3V	
A21	MXM3_257	257	IO	+3.3V	
A22	MXM3_255	255	IO	+3.3V	
A23	MXM3_253	253	IO	+3.3V	
A24	MXM3_251	251	IO	+3.3V	
A25	MXM3_249	249	IO	+3.3V	
A26	MXM3_247	247	IO	+3.3V	
A27	MXM3_245	245	IO	+3.3V	
A28	MXM3_243	243	IO	+3.3V	
A29	MXM3_239	239	IO	+3.3V	
A30	MXM3_286	286	IO	+3.3V	
A31	MXM3_235	235	IO	+3.3V	
A32	MXM3_233	233	IO	+3.3V	
A33	MXM3_231	231	IO	+3.3V	
A34	MXM3_229	229	IO	+3.3V	
A35	MXM3_227	227	IO	+3.3V	
A36	MXM3_225	225	IO	+3.3V	
A37	MXM3_223	223	IO	+3.3V	
A38	MXM3_221	221	IO	+3.3V	
A39	MXM3_211	211	IO	+3.3V	
A40	MXM3_209	209	IO	+3.3V	

### 3.16.10 Function 3 Male (X9 Row B)

Type: 2x40Pin Male

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B1	LCD1_B7		IO	+3.3V	
B2	LCD1_B6		IO	+3.3V	
B3	LCD1_B5		IO	+3.3V	
B4	LCD1_B4		IO	+3.3V	
B5	LCD1_B3		IO	+3.3V	
B6	LCD1_B2		IO	+3.3V	
B7	LCD1_B1		IO	+3.3V	
B8	LCD1_B0		IO	+3.3V	
B9	LCD1_G7		IO	+3.3V	
B10	LCD1_G6		IO	+3.3V	
B11	LCD1_G5		IO	+3.3V	
B12	LCD1_G4		IO	+3.3V	

Pin	Signal Name	MXM3 Pin Number	I/O Type	Voltage	Pull-up/Pull-down
B13	LCD1_G3		IO	+3.3V	
B14	LCD1_G2		IO	+3.3V	
B15	LCD1_G1		IO	+3.3V	
B16	LCD1_G0		IO	+3.3V	
B17	LCD1_R7		IO	+3.3V	
B18	LCD1_R6		IO	+3.3V	
B19	LCD1_R5		IO	+3.3V	
B20	LCD1_R4		IO	+3.3V	
B21	LCD1_R3		IO	+3.3V	
B22	LCD1_R2		IO	+3.3V	
B23	LCD1_R1		IO	+3.3V	
B24	LCD1_R0		IO	+3.3V	
B25	LCD1_DE		IO	+3.3V	
B26	LCD1_HSYNC		IO	+3.3V	
B27	LCD1_VSYNC		IO	+3.3V	
B28	LCD1_PCLK		IO	+3.3V	
B29	PWM_BKL1		IO	+3.3V	
B30	BKL1_ON		IO	+3.3V	
B31	SPI2_CLK		IO	+3.3V	
B32	SPI2_CS		IO	+3.3V	
B33	SPI2_MOSI		IO	+3.3V	
B34	SPI2_MISO		IO	+3.3V	
B35	SPI1_CS		IO	+3.3V	
B36	SPI1_MOSI		IO	+3.3V	
B37	SPI1_MISO		IO	+3.3V	
B38	SPI1_CLK		IO	+3.3V	
B39	I2C1_SCL		IO	+3.3V	1.8K to +3.3V
B40	I2C1_SDA		IO	+3.3V	1.8K to +3.3V

### 3.16.11 Function 3 Female (X10)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X9 Pins A1 to A40

### 3.16.12 GPIO 3 Female (X8)

Type: 1x40Pin Female, 2.54mm

Pin-out identical to X9 Pins B1 to B40

## 4 Default Signal Mapping

The table below lists the default signal mapping (factory setting). Every row of the table shows the mapping of an Apalis pin to the function or connector on the Evaluation Board.

Legend:

Signal name:	GPIO number on the Apalis module
X3 Row A, X6 Row B, X9 Row A	Pin number on the patch panel connector X2/X5/X8 Apalis side (one end of the jumper)
X3 Row B, X6 Row A, X9 Row B	Pin number on the patch panel connector X4/X7/X10, Evaluation Board side (the other end of the jumper)
External Connector	If the signal is available on an external connector the connector's pin number is listed here
Conn. Type	Lists, if a signal is level shifted between the patch panel connector X4/X7/X10 and the external connector
Internal Function	if a signal is not directly accessible on an external connector, but is used to control an on-board function, the function is listed here. For details please refer to the schematics of the Evaluation Board.
Function	Description of the signal

### 4.1 GPIO1 mapping

Apalis Side of the Patch Panel		Evaluation Board Side of the Patch Panel				
Signal Name	X3	X3	Conn. Type	Internal function	External Connector	Function
MXM3_35	A2	B2				SATA1_ACT#
MXM3_17	A3	B3			X38-120	GPIO_8
MXM3_15	A4	B4			X38-118	GPIO_7
MXM3_13	A5	B5			X38-116	GPIO_6
MXM3_11	A6	B6			X38-114	GPIO_5
MXM3_7	A7	B7			X38-112	GPIO_4
MXM3_5	A8	B8			X38-110	GPIO_3
MXM3_3	A9	B9			X38-108	GPIO_2
MXM3_1	A10	B10			X38-106	GPIO_1
MXM3_8	A12	B12		Analog I/O		PWM4
MXM3_6	A13	B13		Analog I/O		PWM3
MXM3_4	A14	B14		Analog I/O		PWM2
MXM3_2	A15	B15		Analog I/O		PWM1
MXM3_12	A17	B17		CAN		CAN1_RX
MXM3_14	A18	B18		CAN		CAN1_TX
MXM3_16	A19	B19		CAN		CAN2_RX
MXM3_18	A20	B20		CAN		CAN2_TX
MXM3_37	A24	B24			X38-98	WAKE1_MICO#
MXM3_24	A25	B25			X38-100	POWER_ENABLE_MOCI
MXM3_26	A26	B26			X38-102	RESET_MOCI#
MXM3_28	A27	B27			X38-104	RESET_MICO#

Apalis Side of the Patch Panel		Evaluation Board Side of the Patch Panel		
MXM3_84	A31	B31	USB Host	USBH_EN
MXM3_96	A32	B32	USB Host	USBH_OC#
MXM3_262	A33	B33	USB Client	USBO1_OC#
MXM3_274	A34	B34	USB Client	USBO1_EN
MXM3_138	A36	B36	X38-94	UART4_TXD
MXM3_140	A37	B37	X38-96	UART4_RXD
MXM3_134	A38	B38	X30-3	UART3_TXD
MXM3_136	A39	B39	X30-4	UART3_RXD

## 4.2 GPIO2 mapping

Signal Name	X6	X6	Conn. Type	Internal function	External Connector	Function
MXM3_207	A1	B1			X39-1/3/5	I2C2_DDC_SCL
MXM3_205	A2	B2			X40-1/3/5	I2C2_DDC_SDA
MXM3_217	A3	B3				SPDIF_IN
MXM3_215	A4	B4			X21-3	SPDIF_OUT
MXM3_204	A5	B5				DAP1_SYNC
MXM3_202	A6	B6				DAP1_D_IN
MXM3_200	A7	B7				DAP1_BIT_CLK
MXM3_198	A8	B8				DAP1_RESET#
MXM3_196	A9	B9				DAP1_DOUT
MXM3_194	A10	B10				DAP1_MCLK
MXM3_190	A11	B11			X19-10	SD1_CD#
MXM3_188	A12	B12			X19-8	SD1_D1
MXM3_186	A13	B13			X19-7	SD1_D0
MXM3_184	A14	B14			X19-5	SD1_CLK
MXM3_180	A15	B15			X19-2	SD1_CMD
MXM3_178	A16	B16			X19-1	SD1_D3
MXM3_176	A17	B17			X19-9	SD1_D2
MXM3_164	A18	B18			X18-2	MMC1_CD#
MXM3_162	A19	B19			X18-3	MMC1_D1
MXM3_160	A20	B20			X18-4	MMC1_D0
MXM3_158	A21	B21			X18-5	MMC1_D7
MXM3_156	A22	B22			X18-7	MMC1_D6
MXM3_154	A23	B23			X18-8	MMC1_CLK
MXM3_152	A24	B24			X18-11	MMC1_D5
MXM3_150	A25	B25			X18-12	MMC1_CMD
MXM3_148	A26	B26			X18-13	MMC1_D4
MXM3_146	A27	B27			X18-14	MMC1_D3
MXM3_144	A28	B28			X18-15	MMC1_D2
MXM3_132	A29	B29	Level shifted		X28-U2	UART2_RXD
MXM3_130	A30	B30	Level shifted		X28-U8	UART2_CTS
MXM3_128	A31	B31	Level shifted		X28-U7	UART2_RTS
MXM3_126	A32	B32	Level shifted		X28-U3	UART2_TXD

Signal Name	X6	X6	Conn. Type	Internal function	External Connector	Function
MXM3_124	A33	B33	Level shifted		X28-L1	UART1_DCD
MXM3_122	A34	B34	Level shifted		X28-L9	UART1_RI
MXM3_120	A35	B35	Level shifted		X28-L6	UART1_DSR
MXM3_118	A36	B36	Level shifted		X28-L2	UART1_RXD
MXM3_116	A37	B37	Level shifted		X28-L8	UART1_CTS
MXM3_114	A38	B38	Level shifted		X28-L7	UART1_RTS
MXM3_112	A39	B39	Level shifted		X28-L3	UART1_TXD
MXM3_110	A40	B40	Level shifted		X28-L4	UART1_DTR

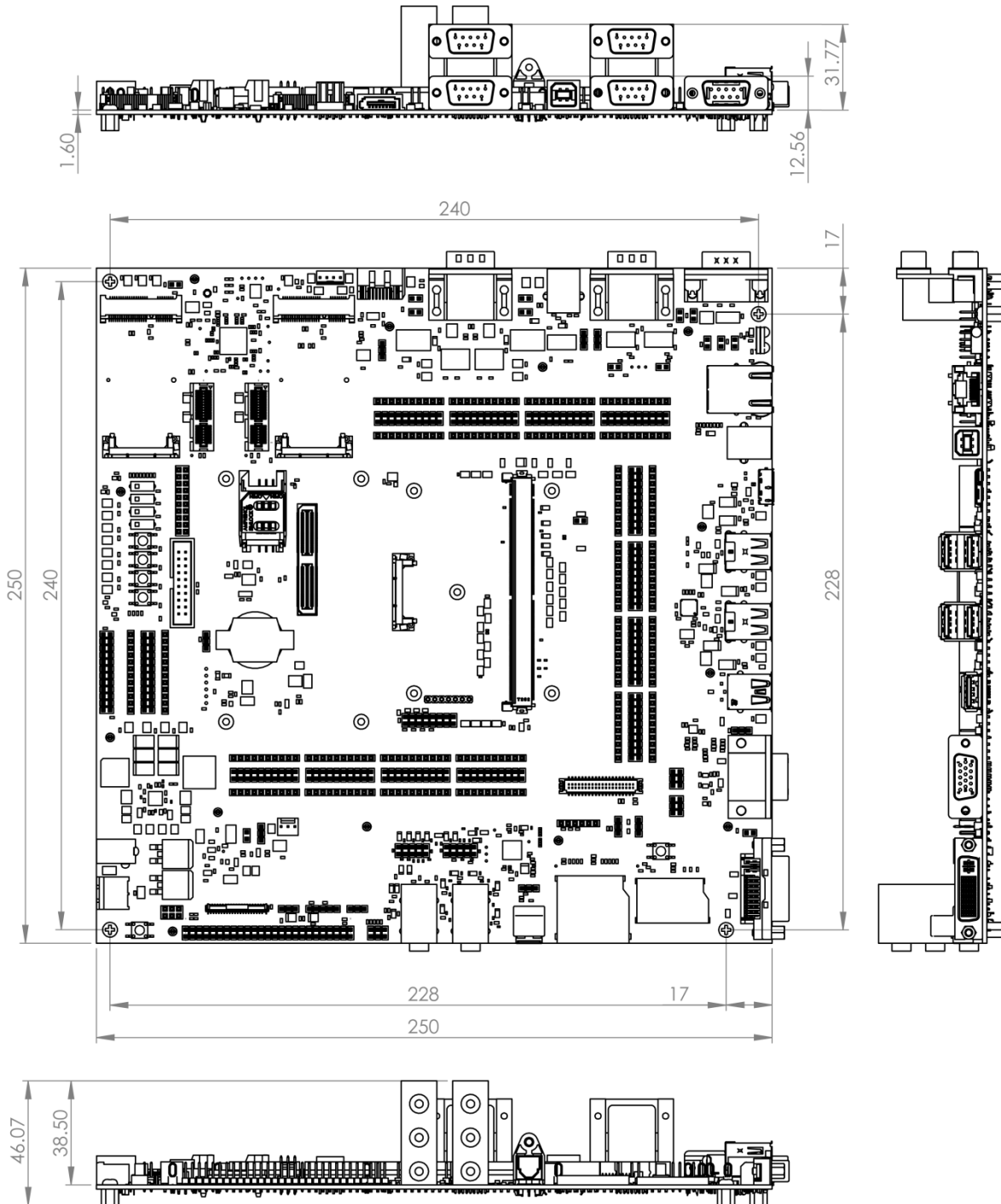
### 4.3 GPIO3 mapping

Apalis Side of the Patch Panel		Evaluation Board Side of the Patch Panel				
Signal Name	X9	X9	Conn. Type	Internal function	External Connector	Function
MXM3_301	A1	B1		RGB TTL	X31-8/ X20-25	LCD1_B7
MXM3_299	A2	B2		RGB TTL	X31-9 / X20-24	LCD1_B6
MXM3_297	A3	B3		RGB TTL	X31-10 / X20-23	LCD1_B5
MXM3_295	A4	B4		RGB TTL	X31-11 / X20-22	LCD1_B4
MXM3_293	A5	B5		RGB TTL	X31-12 / X20-21	LCD1_B3
MXM3_291	A6	B6		RGB TTL	X31-13 / X20-20	LCD1_B2
MXM3_289	A7	B7		RGB TTL	X20-48	LCD1_B1
MXM3_287	A8	B8		RGB TTL	X20-47	LCD1_B0
MXM3_283	A9	B9		RGB TTL	X31-15 / X20-18	LCD1_G7
MXM3_281	A10	B10		RGB TTL	X31-16 / X20-17	LCD1_G6
MXM3_279	A11	B11		RGB TTL	X31-17 / X20-16	LCD1_G5
MXM3_277	A12	B12		RGB TTL	X31-18 / X20-15	LCD1_G4
MXM3_275	A13	B13		RGB TTL	X31-19 / X20-14	LCD1_G3
MXM3_273	A14	B14		RGB TTL	X31-20 / X20-13	LCD1_G2
MXM3_271	A15	B15		RGB TTL	X31-46	LCD1_G1
MXM3_269	A16	B16		RGB TTL	X31-45	LCD1_G0
MXM3_265	A17	B17		RGB TTL	X31-22 / X20-11	LCD1_R7
MXM3_263	A18	B18		RGB TTL	X31-23 / X20-10	LCD1_R6
MXM3_261	A19	B19		RGB TTL	X31-24 / X20-9	LCD1_R5
MXM3_259	A20	B20		RGB TTL	X31-25 / X20-8	LCD1_R4
MXM3_257	A21	B21		RGB TTL	X31-26 / X20-7	LCD1_R3
MXM3_255	A22	B22		RGB TTL	X34-27 / X20-6	LCD1_R2
MXM3_253	A23	B23		RGB TTL	X20-44	LCD1_R1
MXM3_251	A24	B24		RGB TTL	X20-43	LCD1_R0
MXM3_249	A25	B25		RGB TTL	X31-32 / X20-27	LCD1_DE
MXM3_247	A26	B26		RGB TTL	X31-30 / X20-3	LCD1_HSYNC
MXM3_245	A27	B27		RGB TTL	X31-31 / X20-4	LCD1_VSYNC
MXM3_243	A28	B28		RGB TTL	X31-28 / X20-2	LCD1_PCLK
MXM3_239	A29	B29			X31-6	PWM_BKL1
MXM3_286	A30	B30			X31-5 / X20-37	BKL1_ON

Apalis Side of the Patch Panel		Evaluation Board Side of the Patch Panel		
MXM3_235	A31	B31	X38-6	SPI2_CLK
MXM3_233	A32	B32	X38-8	SPI2_CS
MXM3_231	A33	B33	X38-10	SPI2_MOSI
MXM3_229	A34	B34	X38-12	SPI2_MISO
MXM3_227	A35	B35	X38-14	SPI1_CS
MXM3_225	A36	B36	X38-16	SPI1_MOSI
MXM3_223	A37	B37	X38-18	SPI1_MISO
MXM3_221	A38	B38	X38-20	SPI1_CLK
MXM3_211	A39	B39		I2C1_SCL
MXM3_209	A40	B40		I2C1_SDA

## 5 Mechanical Data

### 5.1 Apalis Evaluation Board Dimensions - Top Side



**Fig.3 Apalis Evaluation Board Mechanical Drawing – Top Side**  
**(All dimensions are in Millimetres)**



## 6 Design Data

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The design data for Toradex carrier boards are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the carrier board design data, please use the web-link below:

<http://developer.toradex.com/carrier-board-design>

## 7 Product Compliance

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Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: <http://www.toradex.com/support/product-compliance>

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