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Verdin AM62

HW Datasheet

Preliminary – Subject to Change

Revision History

Date	Doc. Rev.	Module Version	Changes
08-March-2023	Rev. 0.1	V1.0	Initial documentation

Contents

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Verdin AM62. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website: `https://developer.toradex.com/hardware/verdin-som-family/modules/verdin-am62`.

1.2 Verdin SoM Family

The Verdin System on Module (SoM) family eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology is encapsulated on the SoM. This allows the customer to create a carrier board that focuses solely on application- specific electronics, making the project substantially less complex. The Verdin module takes this one step further and implements an interface pinout that allows direct connection of real-world I/O ports without the need to cross traces or traverse layers, referred to as Direct BreakoutTM. This becomes increasingly important for customers as more interfaces move toward high-speed serial technologies that require impedance-controlled differential pairs. Direct BreakoutTM allows them to easily route such interfaces to common connectors in a simple, robust fashion.

The Verdin SoM features a wide input voltage range that allows it to be powered from a broad range of power sources (e.g., directly from a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, the I/O voltage level is trending to decrease from 3.3V to 1.8V. For this reason, the Verdin family of SoMs supports a 1.8V I/O voltage level only. Both the wide input voltage range and the 1.8V I/O voltage make the power supply designs for a Verdin carrier board simple, easy, and cost-efficient. These features altogether make the Verdin family of SoMs perfectly suited for battery-powered applications as well.

More information: `https://docs.toradex.com/109262-verdin-family-specification.pdf`

1.3 TI AM62 SoC

`https://www.ti.com/lit/gpn/am623`

`https://www.ti.com/lit/gpn/am625`

1.4 Verdin AM62 SoM

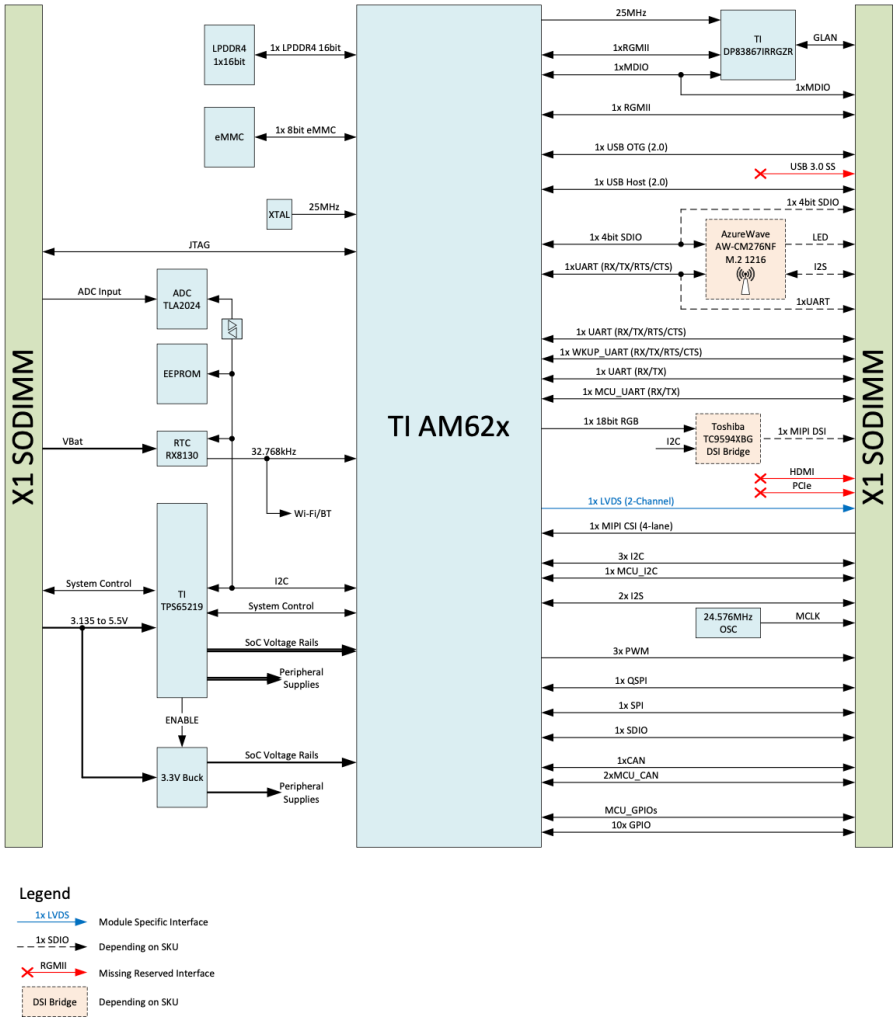
The Verdin AM62 targets a wide range of applications, including Industrial Automation, Medical, Transportation, Smart Cities, Test and Measurement, and many more.

The SoM is available with an optional Wi-Fi and Bluetooth interface.

The module offers a wide range of interfaces ranging from simple GPIOs, industry-standard I2C, SPI, USB, CAN FD, and UART buses to MIPI CSI camera interfaces. An optional MIPI DSI display interface is available on some SoM configurations. The Verdin AM62 module features a Gigabit Ethernet PHY with IEEE1588 support on the module. The SoC features

a second Ethernet MAC with an RGMII interface for adding a Gigabit Ethernet PHY on the carrier board for dual Ethernet applications.

1.5 Block Diagram



1.6 Interface Overview

Features of the Verdin module are split into three distinct categories: “Always Compatible”, “Reserved”, and “Module-specific”. The “Always Compatible” and “Reserved” pins are also referred to as the “Verdin Standard” pins.

Additionally to this definition, the AM62 SoC allows for alternate functions. As an example, many pins can, apart from their primary function, also work as GPIOs.

“Always Compatible” interfaces are features that shall be present on each SoM in the Verdin Family. Customers can count on upgradeability and maximum scalability regarding these interfaces.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoM models due to lack of availability. It could be that a particular SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces

for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any Verdin SoM can be reliably inserted into any Verdin carrier board without causing damage due to incompatible “Reserved” pins.

A “Module-specific” feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules that are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

The alternate functions group means that an interface is provided as an additional function on an “Always Compatible”, “Reserved”, or “Module-specific” pin. These functions can only be used if the primary function of the pin is not used.

The table below shows the interfaces that are supported on the Verdin AM62 module along with the group in which that feature is provided: “Always Compatible”, “Reserved”, “Module- specific”, or alternate function.

Feature	Total	“Always Compatible”	“Reserved”	“Module-specific” or Alternate Function
USB 2.0 OTG	1	1		
USB 2.0 Host	1	1		
Gigabit Ethernet	1	1		
I2C	4	1	3	
SPI	4	1		3
UART	9	3	1	5
PWM	6	1	2	3
SD/SDIO/MMC	2[1]	1		1[1]
GPIO	104[5]	4	6	94[5]
JTAG	1	1		
MIPI DSI	1[2]		1[2]	
RGMII (for 2nd Gigabit Ethernet)	1		1	
QSPI	1[3]		1[3]	
CAN FD	3[4]		2[4]	1
MIPI CSI-2	1		1	
I2S	2		2	
ADC	4		4	
LVDS (dual channel)	1			1

1 One less on configurations featuring Wi-Fi/Bluetooth

2 On some configurations

3 Can be used as OSPI if complemented by additional interface pins using their related alternative functions

4 Some of the instances are only accessible by the M4 core (and not by the A53 cores)

5 Depending on configuration

1.7 Configuration Overview

The table below provides information about different concept configurations for the Verdin AM62. This means that these configurations are not yet committed to launch, but we intend to provide our customers with the most valuable selection of configurations. If you are interested in such a concept configuration, please get in touch with us.

	Verdin AM62 Solo 512MB	Verdin AM62 Solo 512MB IT	Verdin AM62 Dual 1GB WT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB WB WT	Verdin AM62 Dual 1GB WB IT
CPU Details						
CPU Name	TI AM623	TI AM623	TI AM623	TI AM623	TI AM623	TI AM623
CPU Type	1x Arm® Cortex®-A53	1x Arm® Cortex®-A53	2x Arm® Cortex®-A53	2x Arm® Cortex®-A53	2x Arm® Cortex®-A53	2x Arm® Cortex®-A53
Microcontroller	1x Arm® Cortex®-M4F	1x Arm® Cortex®-M4F	1x Arm® Cortex®-M4F	1x Arm® Cortex®-M4F	1x Arm® Cortex®-M4F	1x Arm® Cortex®-M4F
CPU Clock	800MHz (A53) 400MHz (M4F)	1GHz (A53) 400MHz (M4F)	1GHz (A53) 400MHz (M4F)	1GHz (A53) 400MHz (M4F)	1.4GHz (A53) 400MHz (M4F)	1.4GHz (A53) 400MHz (M4F)
Memory						
RAM	512MB LPDDR4 (16 Bit)	512MB LPDDR4 (16 Bit)	1GB LPDDR4 (16 Bit)	1GB LPDDR4 (16 Bit)	1GB LPDDR4 (16 Bit)	1GB LPDDR4 (16 Bit)
Flash	4GB eMMC	4GB eMMC	4GB eMMC	4GB eMMC	4GB eMMC	4GB eMMC
Connectivity						
USB 3.1	-	-	-	-	-	-
USB 2.0	1x Host / 1x OTG	1x Host / 1x OTG	1x Host / 1x OTG	1x Host / 1x OTG	1x Host / 1x OTG	1x Host / 1x OTG
Gigabit Ethernet	1x (+2nd RGMII)	1x (+2nd RGMII)	1x (+2nd RGMII)	1x (+2nd RGMII)	1x (+2nd RGMII)	1x (+2nd RGMII)
RGMII (for 2nd Gigabit Ethernet)	1x	1x	1x	1x	1x	1x
Wi-Fi	-	-	-	-	Yes	Yes
Bluetooth	-	-	-	-	Yes	Yes
PCIe	-	-	-	-	-	-
I2C	4x	4x	4x	4x	4x	4x
SPI	1x + 3x[1]	1x + 3x[1]	1x + 3x[1]	1x + 3x[1]	1x + 3x[1]	1x + 3x[1]
QSPI	1x[2]	1x[2]	1x[2]	1x[2]	1x[2]	1x[2]
UART	4x + 5x[1]	4x + 5x[1]	4x + 5x[1]	4x + 5x[1]	4x + 5x[1]	4x + 5x[1]
PWM	3x + 3x[1]	3x + 3x[1]	3x + 3x[1]	3x + 3x[1]	3x + 3x[1]	3x + 3x[1]
GPIO	10x + 94x[1]	10x + 94x[1]	10x + 94x[1]	10x + 94x[1]	10x + 94x[1]	10x + 94x[1]

	Verdin AM62 Solo 512MB	Verdin AM62 Solo 512MB IT	Verdin AM62 Dual 1GB WT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB WB WT	Verdin AM62 Dual 1GB WB IT
Analog Input	4x	4x	4x	4x	4x	4x
SDIO/SD/MMC	1x + 1x[1]	1x + 1x[1]	1x + 1x[1]	1x + 1x[1]	1x	1x
CAN FD	2x[3] + 1x[1,3]	2x[3] + 1x[1,3]	2x[3] + 1x[1,3]	2x[3] + 1x[1,3]	2x[3] + 1x[1,3]	2x[3] + 1x[1,3]
JTAG	1x	1x	1x	1x	1x	1x
Multimedia						
Display Controllers	Dual	Dual	Dual	Dual	Dual	Dual
Video Decoder	-	-	-	-	-	-
Video Encoder	-	-	-	-	-	-
Display Serial Interface	-	-	1x Quad Lane MIPI DSI	1x Quad Lane MIPI DSI	1x Quad Lane MIPI DSI	1x Quad Lane MIPI DSI
LVDS	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)
Digital Audio	2x McASP: I2S or TDM	2x McASP: I2S or TDM	2x McASP: I2S or TDM	2x McASP: I2S or TDM	2x McASP: I2S or TDM	2x McASP: I2S or TDM
2D Acceleration	Yes	Yes	Yes	Yes	Yes	Yes
3D Acceleration	-	-	-	-	-	-
HDMI	-	-	-	-	-	-
Camera Serial Interface	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2
Physical						
Size	69.6 x 35.0 x 6.0 mm	69.6 x 35.0 x 6.0 mm	69.6 x 35.0 x 6.0 mm	69.6 x 35.0 x 6.0 mm	69.6 x 35.0 x 6.0 mm	69.6 x 35.0 x 6.0 mm
Temperature	0°C to 70°C	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C
Shock / Vibration	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms
Power Dissipation	TBD	TBD	TBD	TBD	TBD	TBD

1 “Module-specific” or alternate function

2 Can be used as OSPI if complemented by additional interface pins using their related alternative functions

3 Some of the instances are only accessible by the M4 core (and not by the A53 cores)

1.8 Pin Assignment

The following table describes the SODIMM connector pinout. Some pins are shaded dark grey as “Module-specific” interfaces. These pins might not be compatible with other modules in the Verdin family. Please be aware that you might lose compatibility when using other Verdin modules on your carrier board if you use these interfaces. It should be noted that “Module-specific” interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both modules A and module B have an

LVDS interface available in the same configurations as a “Module-specific” interface, they shall be assigned to the same pins in the “Module-specific” interface area of the connector. Hence, both module A and module B shall share compatibility between these parts of the “Module-specific” interface.

- X1 Pin: pin number on the SODIMM edge connector (X1).
- Verdin Signal Name: the name of the signal according to the Verdin form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have an alternate function. However, to be compatible with other Verdin modules, only the default function should be used, and the carrier board should be implemented according to the Verdin Carrier Board Design Guide.
- SoC Ball Name: the name of the pin of the SoC.
- Non-SoC Ball Name: Connections to non-SoC balls such as peripherals and power supply.

Module Top Side

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
1	JTAG_1_TDI	TDI		
3	JTAG_1_TRST#	TRSTn		
5	JTAG_1_TDO	TDO		
7	JTAG_1_VREF		1.8V	
9	JTAG_1_TCK	TCK		
11	GND		GND	
13	JTAG_1_TMS	TMS		
15	PWM_1	SPI0_CS0		
17	GPIO_9_DSI	MMC1_SDWP		
19	PWM_3_DSI	SPI0_CLK		
21	GPIO_10_DSI	GPMC0_AD15		
23	DSI_1_D3_N		DSI Bridge	TBA
25	DSI_1_D3_P		DSI Bridge	TBA
27	GND		GND	
29	DSI_1_D2_N		DSI Bridge	TBA
31	DSI_1_D2_P		DSI Bridge	TBA
33	GND		GND	
35	DSI_1_CLK_N		DSI Bridge	TBA
37	DSI_1_CLK_P		DSI Bridge	TBA
39	GND		GND	
41	DSI_1_D1_N		DSI Bridge	TBA
43	DSI_1_D1_P		DSI Bridge	TBA

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
45	GND		GND	
47	DSI_1_D0_N		DSI Bridge	TBA
49	DSI_1_D0_P		DSI Bridge	TBA
51	GND		GND	
53	I2C_2_DSI_SDA	GPMC0_CSn3		
55	I2C_2_DSI_SCL	GPMC0_CSn2		
57	I2C_3_HDMI_SDA	MCU_I2C0_SDA		
59	I2C_3_HDMI_SCL	MCU_I2C0_SCL		
61	HDMI_1_HPD	MCU_UART0_CTSn		
63	HDMI_1_CEC	MCU_UART0_RTSn		
65	GND		GND	
67	HDMI_1_TXC_N	NC		
69	HDMI_1_TXC_P	NC		
71	GND		GND	
73	HDMI_1_TXD0_N	NC		
75	HDMI_1_TXD0_P	NC		
77	GND		GND	
79	HDMI_1_TXD1_N	NC		
81	HDMI_1_TXD1_P	NC		
83	GND		GND	
85	HDMI_1_TXD2_N	NC		
87	HDMI_1_TXD2_P	NC		
89	GND		GND	
91	CSI_1_MCLK	WKUP_CLKOUT0		
93	I2C_4_CSI_SDA	UART0_RTSn		
95	I2C_4_CSI_SCL	UART0_CTSn		
97	GND		GND	
99	CSI_1_D3_P	CSI0_RXP3		
101	CSI_1_D3_N	CSI0_RXN3		
103	GND		GND	
105	CSI_1_D2_P	CSI0_RXP2		
107	CSI_1_D2_N	CSI0_RXN2		
109	GND		GND	
111	CSI_1_CLK_P	CSI0_RXCLKP		
113	CSI_1_CLK_N	CSI0_RXCLKN		

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
115	GND		GND	
117	CSI_1_D1_P	CSI0_RXP1		
119	CSI_1_D1_N	CSI0_RXN1		
121	GND		GND	
123	CSI_1_D0_P	CSI0_RXP0		
125	CSI_1_D0_N	CSI0_RXN0		
127	GND		GND	
129	UART_1_RXD	MCASP0_AFSR		
131	UART_1_TXD	MCASP0_ACLKR		
133	UART_1_RTS	MCASP0_AXR2		
135	UART_1_CTS	MCASP0_AXR3		
137	UART_2_RXD	WKUP_UART0_RXD		
139	UART_2_TXD	WKUP_UART0_TXD		
141	UART_2_RTS	WKUP_UART0_RTSn		
143	UART_2_CTS	WKUP_UART0_CTSn		
145	GND		GND	
147	UART_3_RXD	UART0_RXD		
149	UART_3_TXD	UART0_TXD		
151	UART_4_RXD	MCU_UART0_RXD		
153	UART_4_TXD	MCU_UART0_TXD		
155	USB_1_EN	USB0_DRVVBUS		
157	USB_1_OC#	MMC2_SDCD		
159	USB_1_VBUS	USB0_VBUS		Voltage Divider on the Module
161	USB_1_ID	SPI0_D1		
163	USB_1_D_N	USB0_DM		
165	USB_1_D_P	USB0_DP		
167	GND		GND	
169	USB_2_SSTX_N	NC		
171	USB_2_SSTX_P	NC		
173	GND		GND	
175	USB_2_SSRX_N	NC		
177	USB_2_SSRX_P	NC		
179	GND		GND	
181	USB_2_D_N	USB1_DM		
183	USB_2_D_P	USB1_DP		

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
185	USB_2_EN	USB1_DRVVBUS		
187	USB_2_OC#	MMC2_SDWP		
189	ETH_2_RGMII_INT#	GPMC0_WAIT1		
191	ETH_2_RGMII_MDIO	MDIO0_MDIO		Shared with on-module PHY
193	ETH_2_RGMII_MDC	MDIO0_MDC		Shared with on-module PHY
195	GND		GND	
197	ETH_2_RGMII_RXC	RGMII2_RXC		
199	ETH_2_RGMII_RX_CTI	RGMII2_RX_CTL		
201	ETH_2_RGMII_RXD_0	RGMII2_RD0		
203	ETH_2_RGMII_RXD_1	RGMII2_RD1		
205	ETH_2_RGMII_RXD_2	RGMII2_RD2		
207	ETH_2_RGMII_RXD_3	RGMII2_RD3		
209	GND		GND	
211	ETH_2_RGMII_TX_CTI	RGMII2_TX_CTL		
213	ETH_2_RGMII_TXC	RGMII2_TXC		
215	ETH_2_RGMII_TXD_3	RGMII2_TD3		
217	ETH_2_RGMII_TXD_2	RGMII2_TD2		
219	ETH_2_RGMII_TXD_1	RGMII2_TD1		
221	ETH_2_RGMII_TXD_0	RGMII2_TD0		
223	GND		GND	
225	ETH_1_MDI0_P		Ethernet PHY	TBA
227	ETH_1_MDI0_N		Ethernet PHY	TBA
229	GND		GND	
231	ETH_1_MDI1_N		Ethernet PHY	TBA
233	ETH_1_MDI1_P		Ethernet PHY	TBA
235	ETH_1_LINK		Ethernet PHY	TBA
237	ETH_1_ACT		Ethernet PHY	TBA
239	ETH_1_MDI2_P		Ethernet PHY	TBA
241	ETH_1_MDI2_N		Ethernet PHY	TBA
243	GND		GND	
245	ETH_1_MDI3_N		Ethernet PHY	TBA
247	ETH_1_MDI3_P		Ethernet PHY	TBA
249	VCC_BACKUP		RTC battery	
251	VCC		VCC	

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
253	VCC		VCC	
255	VCC		VCC	
257	VCC		VCC	
259	VCC		VCC	

Module Bottom Side

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
2	ADC_1		ADC	TBA
4	ADC_2		ADC	TBA
6	ADC_3		ADC	TBA
8	ADC_4		ADC	TBA
10	GND		GND	
12	I2C_1_SDA	I2C1_SDA		
14	I2C_1_SCL	I2C1_SCL		
16	PWM_2	SPI0_CS1		
18	GND		GND	
20	CAN_1_TX	MCAN0_TX		
22	CAN_1_RX	MCAN0_RX		
24	CAN_2_TX	MCU_MCAN0_TX		CAN only accessible from M4 Core
26	CAN_2_RX	MCU_MCAN0_RX		CAN only accessible from M4 Core
28	GND		GND	
30	I2S_1_BCLK	MCASP0_ACLKX		
32	I2S_1_SYNC	MCASP0_AFSX		
34	I2S_1_D_OUT	MCASP0_AXR0		
36	I2S_1_D_IN	MCASP0_AXR1		
38	I2S_1_MCLK	GPMC0_WPn	24.576MHz Oscillator	
40	GND		GND	
42	I2S_2_BCLK	GPMC0_BE0n_CLE		
44	I2S_2_SYNC	GPMC0_WAIT0		
46	I2S_2_D_OUT	GPMC0_WEn		

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
48	I2S_2_D_IN	GPMC0_OEn_REn		
50	GND		GND	
52	QSPI_1_CLK	OSPI0_CLK		
54	QSPI_1_CS#	OSPI0_CSn0		
56	QSPI_1_IO0	OSPI0_D0		
58	QSPI_1_IO1	OSPI0_D1		
60	QSPI_1_IO2	OSPI0_D2		
62	QSPI_1_IO3	OSPI0_D3		
64	QSPI_1_CS2#	OSPI0_CSn1		
66	QSPI_1_DQS	SPI0_D0		
68	GND		GND	
70	SD_1_D2	MMC1_DAT2		
72	SD_1_D3	MMC1_DAT3		
74	SD_1_CMD	MMC1_CMD		
76	SD_1_PWR_EN	GPMC0_AD14		
78	SD_1_CLK	MMC1_CLK		
80	SD_1_D0	MMC1_DAT0		
82	SD_1_D1	MMC1_DAT1		
84	SD_1_CD#	MMC1_SDCD		
86	GND		GND	
88	MSP_1	OLDI0_CLK0N		
90	MSP_2	OLDI0_CLK0P		
92	MSP_3	WIFI_W_DISABLE		
94	MSP_4	OLDI0_A0N		
96	MSP_5	OLDI0_A0P		
98	GND		GND	
100	MSP_6	OLDI0_A1N		
102	MSP_7	OLDI0_A1P		
104	MSP_8	SOC_VPP		
106	MSP_9	OLDI0_A2N		
108	MSP_10	OLDI0_A2P		
110	GND		GND	
112	MSP_11	OLDI0_A3N		
114	MSP_12	OLDI0_A3P		

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
116	MSP_13	MCU_MCAN1_RX		CAN only accessible from M4 Core
118	MSP_14	OLDI0_CLK1N		
120	MSP_15	OLDI0_CLK1P		
122	GND		GND	
124	MSP_16	OLDI0_A4N		
126	MSP_17	OLDI0_A4P		
128	MSP_18	MCU_MCAN1_TX		CAN only accessible from M4 Core
130	MSP_19	OLDI0_A5N		
132	MSP_20	OLDI0_A5P		
134	GND		GND	
136	MSP_21	OLDI0_A6N		
138	MSP_22	OLDI0_A6P		
140	MSP_23	RTC_IRQ#		
142	MSP_24	OLDI0_A7N		
144	MSP_25	OLDI0_A7P		
146	GND		GND	
148	MSP_26		WiFi_TX_BCLK	TBA
150	MSP_27		WiFi_RX_DATA0	TBA
152	MSP_28		WiFi_TX_DATA0	TBA
154	MSP_29		WiFi_TX_SYNC	TBA
156	MSP_30	MMC2_CLK		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
158	GND		GND	
160	MSP_31	MMC2_CMD		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
162	MSP_32	MMC2_DAT0		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
164	MSP_33	MMC2_DAT1		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
166	MSP_34	MMC2_DAT2		SDIO assembly option modules w/o Wi-Fi, 1.8V only!

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
168	MSP_35	MMC2_DAT3		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
170	GND		GND	
172	MSP_36		WIFI_BT_WKUP_H	TBA
174	MSP_37		WIFI_WLAN_WKU	TBA
176	MSP_38		WIFI_BT_LED	TBA
178	MSP_39		WIFI_LTE_COEX_I	TBA
180	MSP_40		WIFI_LTE_COEX_C	TBA
182	GND		GND	
184	MSP_41	OSPI0_LBCLKO		UART assembly option modules w/o Wi-Fi
186	MSP_42	OSPI0_DQS		UART assembly option modules w/o Wi-Fi
188	MSP_43		WIFI_WLAN_LED	TBA
190	MSP_44	OSPI0_CSn3		UART assembly option modules w/o Wi-Fi
192	MSP_45	OSPI0_CSn2		UART assembly option modules w/o Wi-Fi
194	GND		GND	
196	SPI_1_CLK	OSPI0_D5		
198	SPI_1_MISO	OSPI0_D7		
200	SPI_1_MOSI	OSPI0_D6		
202	SPI_1_CS	OSPI0_D4		
204	GND		GND	
206	GPIO_1	MCU_SPI0_CS1		
208	GPIO_2	MCU_SPI0_CLK		
210	GPIO_3	MCU_SPI0_D0		
212	GPIO_4	MCU_SPI0_D1		
214	PWR_1V8_MOCI		1.8V	
216	GPIO_5_CSI	GPMC0_DIR		
218	GPIO_6_CSI	GPMC0_BE1n		
220	GPIO_7_CSI	GPMC0_CSn0		
222	GPIO_8_CSI	GPMC0_CSn1		
224	GND		GND	
226	PCIE_1_CLK_N	NC		

X1 Pin	Verdin Signal Name	SoC Ball Name	Non-SoC Ball Name	Note
228	PCIE_1_CLK_P	NC		
230	GND		GND	
232	PCIE_1_L0_RX_N	NC		
234	PCIE_1_L0_RX_P	NC		
236	GND		GND	
238	PCIE_1_L0_TX_N	NC		
240	PCIE_1_L0_TX_P	NC		
242	GND		GND	
244	PCIE_1_RESET#	MCU_SPI0_CS0		
246	CTRL_RECOVERY_MIC		Recovery Cirucuit	TBA
248	CTRL_PWR_BTN_MIC(		PMIC	TBA
250	CTRL_FORCE_OFF_MC		Circuit	TBA
252	CTRL_WAKE1_MICO#	GPMC0_ADVn_ALE		
254	CTRL_PWR_EN_MOCI		Circuit	TBA
256	CTRL_SLEEP_MOCI#	GPMC0_CLK		
258	CTRL_RESET_MOCI#		PMIC	TBA
260	CTRL_RESET_MICO#		PMIC	TBA

1.9 SoC Functions List

Below is a list of all the AM62 pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT5 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted.

ADC:	Analog to Digital Converter input
CAAM:	Cryptographic Acceleration and Assurance Module
CAN:	Controller Area Network
CCM:	Clock Control Module
CSI:	Camera Serial Interface
CSU:	Central Security Unit
EARC:	Enhanced Audio Return Channel (for HDMI)
ECC:	Error-Correcting Code
ECSPI:	Enhanced Configurable SPI
ENET:	Ethernet MAC interface
GPIO:	General-Purpose Input Output
GPC:	General Power Controller
GPT:	General Purpose Timer
HDMI:	High-Definition Multimedia Interface
I2C:	Inter-Integrated Circuit
ISP:	Image Signal Processor
JTAG:	Test Interface
LVDS:	FPD-Link/FlatLink Display interface
MIPI_CSI:	MIPI CSI Subsystem
MIPI_DSI:	MIPI DSI Subsystem
NAND:	Interface for NAND Flash
NPU:	Neural Processing Unit
PCIE:	PCI Express
PDM:	Pulse-Density Modulation Microphone Input
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
SAI:	Serial Interface for Audio (I2S and AC97)
SDMA:	Smart Direct Memory Access Controller
SNVS:	Secure Non-Volatile Storage
SPDIF:	Sony/Philips Digital Interface
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
VPU:	Video Processing Unit (acceleration for video encoding and decoding)

Function Short Forms

X1 Pin	SoC Ball Name	SoC Ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	TDI	A11	TDI									
3	TRSTn	B10	TRSTn									
5	TDO	D12	TDO									
9	TCK	A10	TCK									
12	I2C1_SDA	A17	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO	DDR0_IO_PLL_REFCLK_TEST0P	DDR0_IO_PLL_REFCLK_TEST1P	GPIO1_29	EHRPWM2_B	MMC2_SDWP
13	TMS	B11	TMS									
14	I2C1_SCL	B17	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI	DDR0_IO_PLL_TESTOUT0P	DDR0_IO_PLL_TESTOUT1P	GPIO1_28	EHRPWM2_A	MMC2_SDCD
15	SPI0_CS0	A13	SPI0_CS0		EHRPWM0_A				PR0_ECAP0_SYNC_IN	GPIO1_15		
16	SPI0_CS1	C13	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT				GPIO1_16		EHRPWM_TZn_IN5
17	MMC1_SDWP	C17	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				GPIO1_49		
19	SPI0_CLK	A14	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17		
20	MCAN0_TX	C15	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3
21	GPMC0_AD15	U24	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA19	GPIO0_30	UART2_RTSn	
22	MCAN0_RX	E15	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4
24	MCU_MCAN0_TX	D6	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13		
26	MCU_MCAN0_RX	B3	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14		
30	MCASP0_ACLKX	B20	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A	
32	MCASP0_AFSX	D20	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B	
34	MCASP0_AXR0	E18	MCASP0_AXR0	PR0_ECAP0_IN_APWM_OUT	AUDIO_EXT_REFCLK0			PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I	
36	MCASP0_AXR1	B18	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT			PR0_UART0_RXD	EHRPWM1_A	GPIO1_9	EQEP0_S	
42	GPMC0_BE0n_CLE	M24	GPMC0_BE0n_CLE		MCASP1_ACLKX		PR0_PRU0_GPO12	PR0_PRU0_GPI12	TRC_DATA10	GPIO0_35		
44	GPMC0_WAIT0	U23	GPMC0_WAIT0		MCASP1_AFSX		PR0_PRU0_GPO14	PR0_PRU0_GPI14	TRC_DATA12	GPIO0_37		
46	GPMC0_WEn	L25	GPMC0_WEn		MCASP1_AXR0		PR0_PRU0_GPO11	PR0_PRU0_GPI11	TRC_DATA9	GPIO0_34		
48	GPMC0_OEn_REn	L24	GPMC0_OEn_REn		MCASP1_AXR1		PR0_PRU0_GPO10	PR0_PRU0_GPI10	TRC_DATA8	GPIO0_33		
52	OSPI0_CLK	H24	OSPI0_CLK							GPIO0_0		
53	GPMC0_CSn3	K24	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5		TRC_DATA18	GPIO0_44	MCASP1_ACLKR	
54	OSPI0_CSn0	F23	OSPI0_CSn0							GPIO0_11		
55	GPMC0_CSn2	K22	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD	PR0_PRU0_GPO19	PR0_PRU0_GPI19	TRC_DATA17	GPIO0_43	MCASP1_AFSR	
56	OSPI0_D0	E25	OSPI0_D0							GPIO0_3		
57	MCU_I2C0_SDA	D10	MCU_I2C0_SDA							MCU_GPIO0_18		
58	OSPI0_D1	G24	OSPI0_D1							GPIO0_4		
59	MCU_I2C0_SCL	A8	MCU_I2C0_SCL							MCU_GPIO0_17		

X1 Pin	SoC Ball Name	SoC Ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
60	OSPI0_D2	F25	OSPI0_D2							GPIO0_5		
61	MCU_UART0_CTSn	A6	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7		
62	OSPI0_D3	F24	OSPI0_D3							GPIO0_6		
63	MCU_UART0_RTSn	B6	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8		
64	OSPI0_CSn1	G21	OSPI0_CSn1							GPIO0_12		
66	SPI0_D0	B13	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18		
70	MMC1_DAT2	C21	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43		
72	MMC1_DAT3	D22	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42		
74	MMC1_CMD	A21	MMC1_CMD		TIMER_IO5	UART3_TXD				GPIO1_47		
76	GPMC0_AD14	U25	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA20	GPIO0_29	UART2_CTSn	
78	MMC1_CLK	B22	MMC1_CLK		TIMER_IO4	UART3_RXD				GPIO1_46		
80	MMC1_DAT0	A22	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT			GPIO1_45		
82	MMC1_DAT1	B21	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT			GPIO1_44		
84	MMC1_SDCD	D17	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48		
88	OLDI0_CLK0N	AD4	OLDI0_CLK0N									
90	OLDI0_CLK0P	AE3	OLDI0_CLK0P									
91	WKUP_CLKOUT0	A12	WKUP_CLKOUT0							MCU_GPIO0_23		
93	UART0_RTSn	B15	UART0_RTSn	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1	PR0_ECAP0_IN_APWM_OUT	GPIO1_23	MCASP2_ACLKX	MMC2_SDWP
94	OLDI0_A0N	AA5	OLDI0_A0N									
95	UART0_CTSn	A15	UART0_CTSn	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0	PR0_ECAP0_SYNC_OUT	GPIO1_22	MCASP2_AFSX	MMC2_SDCD
96	OLDI0_A0P	Y6	OLDI0_A0P									
99	CSI0_RXP3	AC13	CSI0_RXP3									
100	OLDI0_A1N	AD3	OLDI0_A1N									
101	CSI0_RXN3	AB12	CSI0_RXN3									
102	OLDI0_A1P	AB4	OLDI0_A1P									
105	CSI0_RXP2	AE13	CSI0_RXP2									
106	OLDI0_A2N	Y8	OLDI0_A2N									
107	CSI0_RXN2	AD13	CSI0_RXN2									
108	OLDI0_A2P	AA8	OLDI0_A2P									
111	CSI0_RXCLKP	AE15	CSI0_RXCLKP									
112	OLDI0_A3N	AB6	OLDI0_A3N									
113	CSI0_RXCLKN	AD15	CSI0_RXCLKN									

X1 Pin	SoC Ball Name	SoC Ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
114	OLDI0_A3P	AA7	OLDI0_A3P									
116	MCU_MCAN1_RX	D4	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16		
117	CSI0_RXP1	AE14	CSI0_RXP1									
118	OLDI0_CLK1N	AE4	OLDI0_CLK1N									
119	CSI0_RXN1	AD14	CSI0_RXN1									
120	OLDI0_CLK1P	AD5	OLDI0_CLK1P									
123	CSI0_RXP0	AC15	CSI0_RXP0									
124	OLDI0_A4N	AC6	OLDI0_A4N									
125	CSI0_RXN0	AB14	CSI0_RXN0									
126	OLDI0_A4P	AC5	OLDI0_A4P									
128	MCU_MCAN1_TX	E5	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15		
129	MCASP0_AFSR	E19	MCASP0_AFSR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S	
130	OLDI0_A5N	AE5	OLDI0_A5N									
131	MCASP0_ACLKR	A20	MCASP0_ACLKR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I	
132	OLDI0_A5P	AD6	OLDI0_A5P									
133	MCASP0_AXR2	A19	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OUT29	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B	
135	MCASP0_AXR3	B19	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7	EQEP0_A	
136	OLDI0_A6N	AE6	OLDI0_A6N									
137	WKUP_UART0_RXD	B4	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9		
138	OLDI0_A6P	AD7	OLDI0_A6P									
139	WKUP_UART0_TXD	C5	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10		
141	WKUP_UART0_RTSn	A4	WKUP_UART0_RTSn	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12		
142	OLDI0_A7N	AD8	OLDI0_A7N									
143	WKUP_UART0_CTSn	C6	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11		
144	OLDI0_A7P	AE7	OLDI0_A7P									
147	UART0_RXD	D14	UART0_RXD	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20		
149	UART0_TXD	E14	UART0_TXD	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21		
151	MCU_UART0_RXD	B5	MCU_UART0_RXD							MCU_GPIO0_5		
153	MCU_UART0_TXD	A5	MCU_UART0_TXD							MCU_GPIO0_6		
155	USB0_DRVVBUS	C20	USB0_DRVVBUS							GPIO1_50		
156	MMC2_CLK	D25	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD				GPIO0_69		
157	MMC2_SDCD	A23	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				GPIO0_71		

X1 Pin	SoC Ball Name	SoC Ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
159	USB0_VBUS	AC11	USB0_VBUS									
160	MMC2_CMD	C24	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD				GPIO0_70		
161	SPI0_D1	B14	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					GPIO1_19		
162	MMC2_DAT0	B24	MMC2_DAT0	MCASP1_AXR0						GPIO0_68		
163	USB0_DM	AE11	USB0_DM									
164	MMC2_DAT1	C25	MMC2_DAT1	MCASP1_AXR1						GPIO0_67		
165	USB0_DP	AD11	USB0_DP									
166	MMC2_DAT2	E23	MMC2_DAT2	MCASP1_AXR2		UART5_TXD				GPIO0_66		
168	MMC2_DAT3	D24	MMC2_DAT3	MCASP1_AXR3		UART5_RXD				GPIO0_65		
181	USB1_DM	AD10	USB1_DM									
183	USB1_DP	AE9	USB1_DP									
184	OSPI0_LBCLKO	G25	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1		
185	USB1_DRVVBUS	F18	USB1_DRVVBUS							GPIO1_51		
186	OSPI0_DQS	J24	OSPI0_DQS					UART5_CTSn		GPIO0_2		
187	MMC2_SDWP	B23	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				GPIO0_72		
189	GPMC0_WAIT1	V25	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				GPIO0_38	EQEP2_I	
190	OSPI0_CSn3	E24	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14		
191	MDIO0_MDIO	AB22	MDIO0_MDIO							GPIO0_85		
192	OSPI0_CSn2	H21	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13		
193	MDIO0_MDC	AD24	MDIO0_MDC							GPIO0_86		
196	OSPI0_D5	J25	OSPI0_D5	SPI1_CLK	MCASP1_AXR0	UART6_TXD				GPIO0_8		
197	RGMII2_RXC	AD23	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1	PR0_PRU0_GPO1	PR0_PRU0_GPI1	PR0_ECAP0_SYNC_IN		GPIO1_2		
198	OSPI0_D7	J22	OSPI0_D7	SPI1_D1	MCASP1_AFSX	UART6_CTSn				GPIO0_10		
199	RGMII2_RX_CTL	AD22	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3	PR0_PRU0_GPO0	PR0_PRU0_GPI0			GPIO1_1		
200	OSPI0_D6	H25	OSPI0_D6	SPI1_D0	MCASP1_ACLKX	UART6_RTSn				GPIO0_9		
201	RGMII2_RD0	AE23	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2	PR0_PRU0_GPO2	PR0_PRU0_GPI2		PR0_UART0_RTSn	GPIO1_3		
202	OSPI0_D4	J23	OSPI0_D4	SPI1_CS0	MCASP1_AXR1	UART6_RXD				GPIO0_7		
203	RGMII2_RD1	AB20	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	MCASP2_AXR7		GPIO1_4		
205	RGMII2_RD2	AC21	RGMII2_RD2		MCASP2_AXR0	PR0_PRU0_GPO4	PR0_PRU0_GPI4	PR0_UART0_RXD		GPIO1_5	EQEP2_A	
206	MCU_SPI0_CS1	B8	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1		
207	RGMII2_RD3	AE22	RGMII2_RD3		AUDIO_EXT_REFCLK0	PR0_PRU0_GPO16	PR0_PRU0_GPI16	PR0_UART0_TXD		GPIO1_6	EQEP2_B	
208	MCU_SPI0_CLK	A7	MCU_SPI0_CLK							MCU_GPIO0_2		

X1 Pin	SoC Ball Name	SoC Ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
210	MCU_SPI0_D0	D9	MCU_SPI0_D0							MCU_GPIO0_3		
211	RGMII2_TX_CTL	AA19	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4	PR0_PRU1_GPO0	PR0_PRU1_GPI0			GPIO0_87		
212	MCU_SPI0_D1	C9	MCU_SPI0_D1							MCU_GPIO0_4		
213	RGMII2_TXC	AE21	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5	PR0_PRU1_GPO1	PR0_PRU1_GPI1			GPIO0_88		
215	RGMII2_TD3	AC20	RGMII2_TD3		MCASP2_ACLKX	PR0_PRU1_GPO16	PR0_PRU1_GPI16	PR0_ECAP0_SYNC_OUT	PR0_UART0_CTSn	GPIO1_0	EQEP2_S	
216	GPMC0_DIR	M22	GPMC0_DIR	PR0_ECAP0_IN_APWM_OUT		MCASP2_AXR13	PR0_PRU0_GPO16	PR0_PRU0_GPI16	TRC_DATA14	GPIO0_40	EQEP2_S	
217	RGMII2_TD2	AD21	RGMII2_TD2		MCASP2_AFSX	PR0_PRU1_GPO4	PR0_PRU1_GPI4	PR0_ECAP0_IN_APWM_OUT		GPIO0_91	EQEP2_I	
218	GPMC0_BE1n	N20	GPMC0_BE1n			MCASP2_AXR12	PR0_PRU0_GPO13	PR0_PRU0_GPI13	TRC_DATA11	GPIO0_36		
219	RGMII2_TD1	AA18	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLKR	PR0_PRU1_GPO3	PR0_PRU1_GPI3	MCASP2_AXR8		GPIO0_90		
220	GPMC0_CSn0	M21	GPMC0_CSn0			MCASP2_AXR14	PR0_PRU0_GPO17	PR0_PRU0_GPI17	TRC_DATA15	GPIO0_41		
221	RGMII2_TD0	Y18	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6	PR0_PRU1_GPO2	PR0_PRU1_GPI2			GPIO0_89		
222	GPMC0_CSn1	L21	GPMC0_CSn1	PR0_PRU1_GPO16	PR0_PRU1_GPI16	MCASP2_AXR15	PR0_PRU0_GPO18	PR0_PRU0_GPI18	TRC_DATA16	GPIO0_42		
244	MCU_SPI0_CS0	E8	MCU_SPI0_CS0				WKUP_TIMER_IO1			MCU_GPIO0_0		
252	GPMC0_ADVn_ALE	L23	GPMC0_ADVn_ALE		MCASP1_AXR2		PR0_PRU0_GPO9	PR0_PRU0_GPI9	TRC_DATA7	GPIO0_32		
256	GPMC0_CLK	P25	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX	PR0_PRU0_GPO8	PR0_PRU0_GPI8	TRC_DATA6	GPIO0_31		

1.10 Additional Resources

1.10.1 Verdin Carrier Board Design Guide

A custom carrier board should follow the Verdin Carrier Board Design Guide to make the board compatible with the Verdin module family. Please study this document in detail before starting your carrier board design.

`https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf`

1.10.2 Verdin Family Specification

This document outlines the specification which defines the Verdin Computer-on-Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and possible thermal solutions.

`https://docs.toradex.com/109262-verdin-family-specification.pdf`

1.10.3 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.

`http://docs.toradex.com/102492-layout-design-guide.pdf`

1.10.4 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there.

Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Verdin AM62.

`http://www.developer.toradex.com`

1.10.5 Verdin Carrier Board Schematics

We provide complete schematics plus an Altium project file which includes library symbols and IPC-7351 compliant footprints for the Verdin Software Development Board, as well as other carrier boards, free of charge. This resource is of great help when designing your own carrier board.

`http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design`

1.10.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, and Colibri Modules. The tool allows comparing the interfaces across

different modules.

`http://developer.toradex.com/knowledge-base/pinout-designer`

Product Compliance Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: `http://www.toradex.com/support/product-compliance`

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