XC6601 Series

ETR03035-008a

Low Voltage Input LDO Voltage Regulator with Soft-Start Function

■GENERAL DESCRIPTION

The XC6601 series is a low voltage input CMOS LDO regulator which provides highly accurate (±20mV) outputs and can supply current efficiently due to its ultra low on-resistance even at low output voltages. The series is ideally suited to the applications which require very low dropout voltage operation and consists of a voltage reference, an error amplifier, a driver transistor, a current limiter, a fold back circuit, a thermal shutdown (TSD) circuit, an under voltage lock out (UVLO) circuit, soft-start circuit and a phase compensation circuit.

Output voltage is selectable in 0.05V increments within a range of 0.7V to 1.8V using laser trimming technology and ceramic capacitors can be used for the output stabilization capacitor (C_L).

The over current protection circuit (the current limiter and the fold back circuit) as well as the thermal shutdown circuit (the TSD circuit) are built-in. These two protection circuits will operate when either the output current reaches the current limit level or the junction temperature reaches the temperature limit level.

With the built-in UVLO function, the regulator output is forced OFF when the voltage level at the V_{BIAS} pin or the V_{IN} pin falls below the UVLO voltage level. With the soft-start function, the inrush current from V_{IN} to V_{OUT} for charging C_L at start-up can be reduced and makes the V_{IN} stable.

The CE function enables the output to be turned off and the series to be put in stand-by mode resulting in greatly reduced power consumption. At the time of entering the stand-by mode, the series enables the electric charge at the output capacitor (C_L) to be discharged via the internal auto-discharge switch which is located between the V_{OUT} pin and the V_{SS} pin. As a result the V_{OUT} pin quickly returns to the V_{SS} level.

■APPLICATIONS

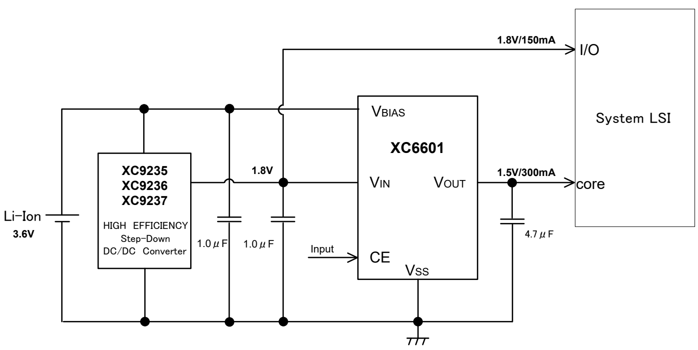
- ●Smart phones / Mobile phones
- ●Portable game consoles
- ●Digital still cameras / Camcorders
- ●Digital audio equipment
- ●Mobile devices / terminals

■FEATURES

Maximum Output Current	: 400mA (Limit:550mA TYP.)
Dropout Voltage	: 38mV@I_{OUT}=100mA (TYP.) (at V_{BIAS} - V_{OUT}=2.4V)
Bias Voltage Range	: 2.5V ~ 6.0V (V_{BIAS} - V_{OUT}≧1.2V)
Input Voltage Range	: 1.0V ~ 3.0V(V_{IN}≦V_{BIAS})
Output Voltage Range	: 0.7V ~ 1.8V (0.05V increments)
Output Voltage Accuracy	:±20mV
Power Consumption	: I_{BIAS}=25μA , I_{IN}=1.0μA (TYP.) I_{BIAS}=0.01μA , I_{IN}=0.01μA (TYP.)
UVLO	: V_{BIAS}=2.0V, V_{IN}=0.4V (TYP.)
TSD (Detect/Release)	: 150℃/125℃ (TYP.)
Soft-Start Time	: 240μs @ V_{OUT}=1.2V (TYP.)
Operating Temperature Range	: -40℃ ~ 85℃
Function	: C_L High Speed Auto-Discharge
Low ESR Capacitor	: Ceramic Capacitor Compatible
Packages	: USP-6C, SOT-25, SOT-89-5
Environmentally Friendly	: EU RoHS Compliant, Pb Free

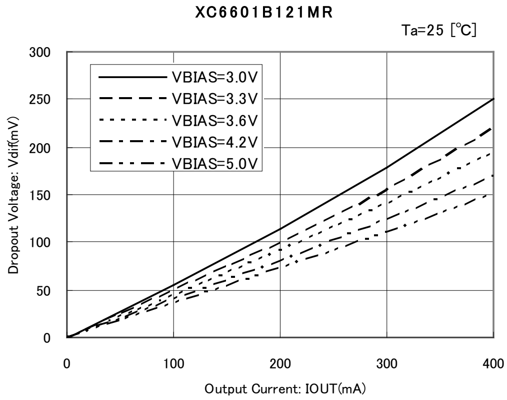
■ TYPICAL APPLICATION CIRCUIT

●V_{BIAS} =3.6V , V_{IN} =1.8V , V_{OUT} =1.5V



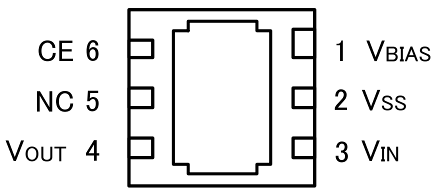
■ TYPICAL PEFORMANCE CHARACTERISTICS

●Dropout Voltage vs. Output Current



■PIN CONFIGURATION

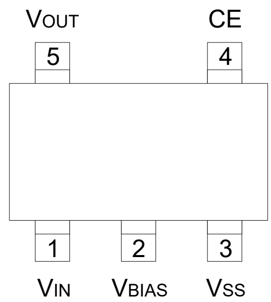
●USP-6C



USP-6C
(BOTTOM VIEW)

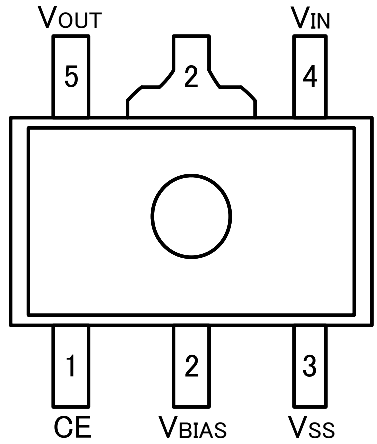
*The heat dissipation pad of the USP-6C package is recommended to solder as the recommended mount pattern and metal mask pattern for mounting strength. This pad should be electrically opened or connected to the V_{BIAS} (No.1) pin.

●SOT-25



SOT-25
(TOP VIEW)

●SOT-89-5



SOT-89-5
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTION
USP-6C	SOT-25	SOT-89-5		
1	2	2	V_{BIAS}	Power Supply Input
3	1	4	V_{IN}	Driver Transistor Input
4	5	5	V_{OUT}	Output
2	3	3	V_{SS}	Ground
6	4	1	CE	ON/OFF Control

■PRODUCT CLASSIFICATION

●Ordering Information

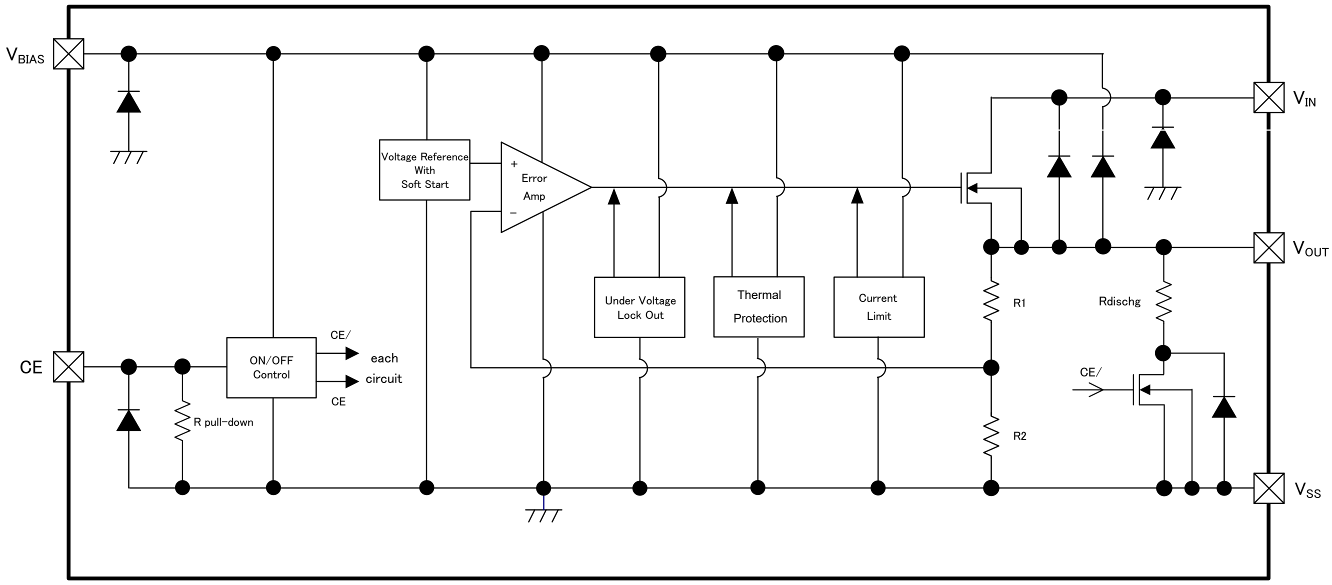
XC6601①②③④⑤⑥-⑦ (*1) : CE High Active, Soft-Start Function Built-in, CL Auto Discharge Function

MARK	DESCRIPTION	SYMBOL	DESCRIPTION
①	Type of Regulators	A	Pull-Down Resistor Built-in
		B	No Pull-Down Resistor Built-in
②③	Output Voltage	07 ~ 18	e.g.) $V_{OUT(T)}$=1.2V⇒②=1,③=2
④	Output Voltage Type	1	0.1V increments e.g.) 1.2V⇒②=1,③=2,④=1
		B	0.05V increments e.g.) 1.25V⇒②=1,③=2,④=B
⑤⑥-⑦	Packages Taping Type (*2)	MR-G	SOT-25 (3,000pcs/Reel)
		ER-G	USP-6C (3,000pcs/Reel)
		PR-G	SOT-89-5 (1,000pcs/Reel)

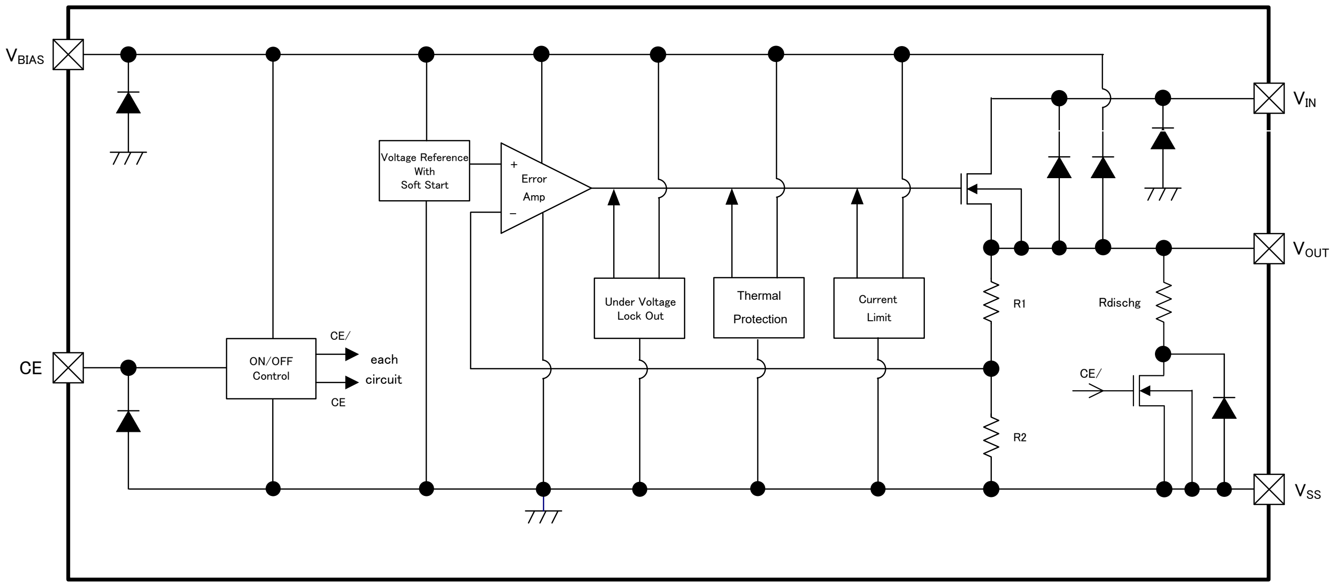
(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.
(*2) The device orientation is fixed in its embossed tape pocket.
For reverse orientation, please contact your local Torex sales office or representative.
(Standard orientation: ⑤R-⑦, Reverse orientation: ⑤L-⑦)

■BLOCK DIAGRAMS

(1) XC6601A Series



(2) XC6601B Series



*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■MAXIMUM ABSOLUTE RATINGS

Ta=25 ℃

PARAMETER		SYMBOL	RATINGS	UNITS
Bias Voltage		V_{BIAS}	V_{SS} - 0.3 ~ 7.0	V
Input Voltage		V_{IN}	V_{SS} - 0.3 ~ 7.0	V
Output Current		I_{OUT}	700 (*1)	mA
Output Voltage		V_{OUT}	V_{SS} - 0.3 ~ V_{BIAS} + 0.3	V
			V_{SS} - 0.3 ~ V_{IN} + 0.3	
CE Input Voltage		V_{CE}	V_{SS} - 0.3 ~ 7.0	V
Power Dissipation	USP-6C	Pd	100	mW
			1000 (40mm x 40mm Standard board) (*2)	
			1250 (JESD51-7 Board) (*2)	
	SOT-25		250	
			600 (40mm x 40mm Standard board) (*2)	
			760 (JESD51-7 Board) (*2)	
	SOT-89-5		500	
			1300 (40mm x 40mm Standard board) (*2)	
			1750 (JESD51-7 Board) (*2)	
Operating Temperature Range		Topr	-40 ~ 85	℃
Storage Temperature Range		Tstg	-55 ~ 125	℃

(*1) I_{OUT}=Less than Pd / (V_{IN}-V_{OUT})

(*2) Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

Ta=25 ℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Bias Voltage (*1)	V_{BIAS}	$V_{CE}=V_{BIAS}$, $V_{IN}=V_{OUT(T)}+0.3V$	2.5	-	6.0	V	①
Input Voltage (*2)	V_{IN}	$V_{BIAS}=V_{CE}=3.6V$	1.0	-	3.0	V	①
Output Voltage	$V_{OUT(E)}$ (*3)	$V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=100mA$	-0.02 E-0 (*5)	$V_{OUT(T)}$ (*4)	+0.02	V	①
Maximum Output Current 1	$I_{OUTMAX\ 1}$	$V_{CE}=V_{BIAS}$, $V_{BIAS}-V_{OUT(T)}\geqq1.2V$ $V_{IN}=V_{OUT(T)}+0.5V$	200	-	-	mA	①
Maximum Output Current 2	$I_{OUTMAX\ 2}$	$V_{CE}=V_{BIAS}$, $V_{BIAS}-V_{OUT(T)}\geqq1.3V$ $V_{IN}=V_{OUT(T)}+0.5V$	300	-	-	mA	①
Maximum Output Current 3	$I_{OUTMAX\ 3}$	$V_{CE}=V_{BIAS}$, $V_{BIAS}-V_{OUT(T)}\geqq1.5V$ $V_{IN}=V_{OUT(T)}+0.5V$	400	-	-	mA	①
Load Regulation	$\triangle V_{OUT}$	$V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $1mA\leqq I_{OUT}\leqq300mA$	-	8	17	mV	①
Dropout Voltage 1	Vdif1 (*7)	$V_{BIAS}=V_{CE}$, $I_{OUT}=100mA$		E-1 (*6)		mV	①
Dropout Voltage 2	Vdif2 (*7)	$V_{CE}=V_{BIAS}$, $I_{OUT}=200mA$		E-2 (*6)		mV	①
Dropout Voltage 3	Vdif3 (*7)	$V_{CE}=V_{BIAS}$, $I_{OUT}=300mA$		E-3 (*6)		mV	①
Dropout Voltage 4	Vdif4 (*7)	$V_{CE}=V_{BIAS}$, $I_{OUT}=400mA$		E-4 (*6)		mV	①
Supply Current 1	I_{BIAS}	$V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$ V_{OUT}=OPEN	8	25	45	μA	①
Supply Current 2	I_{IN}	$V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$ V_{OUT}=OPEN	0.1	1.0	3.0	μA	①
Bias Current (*10)	$I_{BIASMAX}$	$V_{OUT(T)}\geqq1.0V$ $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}$ $V_{OUT}=V_{OUT(T)}-0.05V$ $V_{OUT(T)}<1.0V$ $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=1.0V$ $V_{OUT}=V_{OUT(T)}-0.05V$	-	1.0	2.5	mA	①
Stand-by Current 1	I_{BIAS_STB}	$V_{BIAS}=6.0V$, $V_{IN}=3.0V$, $V_{CE}=V_{SS}$	-	0.01	0.10	μA	①
Stand-by Current 2	I_{IN_STB}	$V_{BIAS}=6.0V$, $V_{IN}=3.0V$, $V_{CE}=V_{SS}$	-	0.01	0.35	μA	①
Bias Regulation	$\triangle V_{OUT}/$ $(\triangle V_{BIAS}\cdot V_{OUT})$	$V_{OUT(T)}\geqq1.3V$ $V_{OUT(T)}+1.2V\leqq V_{BIAS}\leqq6.0V$, $V_{IN}=V_{OUT(T)}+0.3V$, $V_{CE}=V_{BIAS}$, $I_{OUT}=1mA$ $V_{OUT(T)}<1.3V$ $2.5V\leqq V_{BIAS}\leqq6.0V$, $V_{IN}=V_{OUT(T)}+0.3V$, $V_{CE}=V_{BIAS}$, $I_{OUT}=1mA$	-	0.01	0.3	%/V	①
Input Regulation	$\triangle V_{OUT}/$ $(\triangle V_{IN}\cdot V_{OUT})$	$V_{OUT(T)}\geqq0.90V$, $V_{OUT(T)}+0.1V\leqq V_{IN}\leqq3.0V$, $V_{BIAS}=V_{CE}=3.6V$, $I_{OUT}=1mA$ $V_{OUT(T)}<0.90V$, $1.0V\leqq V_{IN}\leqq3.0V$ $V_{BIAS}=V_{CE}=3.6V$, $I_{OUT}=1mA$	-	0.01	0.1	%/V	①
Bias Voltage UVLO	V_{BIAS_UVLO}	$V_{CE}=V_{BIAS}$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$	1.37	2.0	2.5	V	①
Input Voltage UVLO	V_{IN_UVLO}	$V_{BIAS}=V_{CE}=3.6V$, $I_{OUT}=1mA$	0.07	0.4	0.6	V	①
V_{BIAS} Ripple Rejection	V_{BIAS_PSRR}	$V_{BIAS}=V_{CE}=3.6V_{DC}+0.2V_{p-pAC}$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=30mA$, f=1kHz	-	40	-	dB	②
V_{IN} Ripple Rejection	V_{IN_PSRR}	$V_{IN}=V_{OUT(T)}+0.3V_{DC}+0.2V_{p-pAC}$, $V_{BIAS}=3.6V$, $I_{OUT}=30mA$, f=1kHz	-	60	-	dB	②

■ELECTRICAL CHARACTERISTICS (Continued)

Ta=25 ℃

PARAMETER	SYNBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage Temperature Characteristics	△VOUT/ △Topr・VOUT	VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V , IOUT=30mA, - 40℃≦ Topr ≦85℃	-	±100	-	ppm/℃	①
Limit Current	ILIM	VOUT=VOUT(E)×0.95, VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V	400	550	-	mA	①
Short Current	ISHORT	VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V, VOUT=0V	-	80	-	mA	①
Thermal Shutdown Detect Temperature	TTSD	Junction Temperature	-	150	-	℃	①
Thermal Shutdown Release Temperature	TTSR	Junction Temperature	-	125	-	℃	①
Hysteresis Width	TTSD−TTSR		-	25	-	℃	①
CL Auto-Discharge Resistance	Rdischg	VBIAS=3.6V, VIN= VOUT(T)+0.3V, VCE= VSS, VOUT=VOUT(T)	290	430	610	Ω	①
CE "H" Level Voltage	VCEH	VBIAS=3.6V, VIN= VOUT(T)+0.3V	0.75	-	6.0	V	①
CE "L" Level Voltage	VCEL	VBIAS=3.6V, VIN= VOUT(T)+0.3V	-	-	0.16	V	①
CE "H" Level Current (A Series)	ICEH	VBIAS=VCE=6.0V, VIN=VOUT(T)+0.3V	2.4	-	8.0	μA	①
CE "H" Level Current (B Series)			-0.1	-	0.1		
CE "L" Level Current	ICEL	VBIAS=6.0V, VCE=VSS VIN=VOUT(T)+0.3V	-0.1	-	0.1	μA	①
Soft-Start Time (*11)	tSS	VBIAS=3.6V, VIN=VOUT(T)+0.3V, IOUT=1mA VCE=0V→3.6V	100	-	410	μs	③

NOTE:
* 1: Please use Bias voltage V_{BIAS} within the range $V_{BIAS}-V_{OUT(E)}$ (*3)≧1.2V
* 2: Please use Input voltage V_{IN} within the range $V_{IN}≦V_{BIAS}$
* 3: VOUT(E) = Effective output voltage (Refer to the voltage chart E-0 and E-1)
* 4: VOUT (T) = Specified output voltage
* 5: E-0 = Please refer to the table named OUTPUT VOLTAGE CHART
* 6: E-1 = Please refer to the table named DROPOUT VOLTAGE CHART
* 7: Vdif = {VIN1(*8)-VOUT1(*9)}.
* 8: VIN1 = The input voltage when VOUT1 appears as input voltage is gradually decreased.
* 9: VOUT1 = A voltage equal to 98% of the output voltage while maintaining an amply stabilized output voltage when V_{IN}=VBIAS at V_{BIAS}<3.0V, and V_{IN}=3.0V at V_{BIAS}≧3.0V is input to the V_{IN} pin.
* 10: IBIASMAX = A supply current at the V_{BIAS} pin providing for the output current (I_{OUT}).
* 11: t_{SS} is defined as a time V_{OUT} reaches $V_{OUT(E)}$x0.9V from the time when CE H threshold 0.75V is input to the CE pin.

■OUTPUT VOLTAGE CHART

NOMINAL OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) VOUT	
VOUT(T)	MIN.	MAX.
0.70	0.680	0.720
0.75	0.730	0.770
0.80	0.780	0.820
0.85	0.830	0.870
0.90	0.880	0.920
0.95	0.930	0.970
1.00	0.980	1.020
1.05	1.030	1.070
1.10	1.080	1.120
1.15	1.130	1.170
1.20	1.180	1.220
1.25	1.230	1.270

NOMINAL OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) VOUT	
VOUT(T)	MIN.	MAX.
1.30	1.280	1.320
1.35	1.330	1.370
1.40	1.380	1.420
1.45	1.430	1.470
1.50	1.480	1.520
1.55	1.530	1.570
1.60	1.580	1.620
1.65	1.630	1.670
1.70	1.680	1.720
1.75	1.730	1.770
1.80	1.780	1.820

■DROPOUT VOLTAGE CHART

NOMINAL OUTPUT VOLTAGE (V)	E-1														
	DROPOUT VOLTAGE 1 (mV)														
	Vdif 1														
	V_{BIAS}=3.0 (V)			V_{BIAS}=3.3 (V)			V_{BIAS}=3.6 (V)			V_{BIAS}=4.2 (V)			V_{BIAS}=5.0 (V)		
	Vgs[*1]	Vdif(mV)		Vgs	Vdif(mV)		Vgs	Vdif(mV)		Vgs	Vdif(mV)		Vgs	Vdif(mV)	
$V_{OUT(T)}$	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.
0.70	2.30	40	300	2.60	35	300	2.90	33	300	3.50	30	300	4.30	27	300
0.75	2.25	41	250	2.55	36	250	2.85	34	250	3.45	31	250	4.25	28	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	42	150	2.45	38	150	2.75	34	150	3.35	31	150	4.15	28	150
0.90	2.10		100	2.40		100	2.70		100	3.30		100	4.10		100
0.95	2.05	43	68	2.35	40	61	2.65	35	56	3.25	32	50	4.05	28	50
1.00	2.00			2.30			2.60			3.20		49	4.00		44
1.05	1.95	46	72	2.25	41	63	2.55	36	58	3.15	32	50	3.95	29	45
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	48	75	2.15	42	65	2.45	38	59	3.05	32	51	3.85	29	46
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	51	81	2.05	43	68	2.35	40	61	2.95	33	52	3.75	29	47
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	54	87	1.95	46	72	2.25	41	63	2.85	34	53	3.65	30	47
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	57	92	1.85	48	75	2.15	42	65	2.75	34	54	3.55	30	48
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	61	94	1.75	51	81	2.05	43	68	2.65	35	56	3.45	31	48
1.60	1.40	63	97	1.70			2.00			2.60			3.40		
1.65	1.35	67	104	1.65	54	87	1.95	46	72	2.55	36	58	3.35	31	49
1.70	1.30	70	113	1.60			1.90			2.50			3.30		
1.75	1.25	74	131	1.55	57	92	1.85	48	75	2.45	38	59	3.25	32	49
1.80	1.20	79	154	1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} – $V_{OUT(T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-2														
	DROPOUT VOLTAGE 2 (mV)														
	Vdif 2														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs(*1) (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)	
$V_{OUT (T)}$		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.
0.70	2.30	81	300	2.60	74	300	2.90	68	300	3.50	62	300	4.30	57	300
0.75	2.25	85	250	2.55	76	250	2.85	70	250	3.45	63	250	4.25	58	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	88	150	2.45	78	150	2.75	72	150	3.35	63	150	4.15	58	150
0.90	2.10		131	2.40		117	2.70		110	3.30		100	4.10		100
0.95	2.05	90	139	2.35	81	123	2.65	74	111	3.25	64	98	4.05	58	88
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	96	146	2.25	85	127	2.55	76	114	3.15	65	101	3.95	59	90
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	101	154	2.15	88	131	2.45	78	117	3.05	67	103	3.85	59	91
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	108	170	2.05	90	139	2.35	81	123	2.95	68	106	3.75	60	92
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	115	179	1.95	96	146	2.25	85	127	2.85	70	108	3.65	61	93
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	122	192	1.85	101	154	2.15	88	131	2.75	72	110	3.55	62	94
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	129	197	1.75	108	170	2.05	90	139	2.65	74	111	3.45	63	95
1.60	1.40	135	206	1.70			2.00			2.60			3.40		
1.65	1.35	145	223	1.65	115	179	1.95	96	146	2.55	76	114	3.35	63	97
1.70	1.30	154	248	1.60			1.90			2.50			3.30		
1.75	1.25	165	293	1.55	122	192	1.85	101	154	2.45	78	117	3.25	64	98
1.80	1.20	175	353	1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} – $V_{OUT(T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-3														
	DROPOUT VOLTAGE 3 (mV)														
	Vdif 3														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs(*1) (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)	
$V_{OUT(T)}$		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.
0.70	2.30	130	300	2.60	115	300	2.90	107	300	3.50	95	300	4.30	89	300
0.75	2.25	134	250	2.55	117	250	2.85	109	250	3.45	96	250	4.25	90	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	138	204	2.45	119	181	2.75	111	167	3.35	97	150	4.15	90	150
0.90	2.10			2.40			2.70			3.30		148	4.10		132
0.95	2.05	145	216	2.35	130	190	2.65	115	170	3.25	98	151	4.05	91	134
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	153	227	2.25	134	197	2.55	117	176	3.15	101	153	3.95	92	137
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	161	239	2.15	138	204	2.45	119	181	3.05	105	155	3.85	93	139
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	173	264	2.05	145	216	2.35	130	190	2.95	107	159	3.75	93	140
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	184	289	1.95	153	227	2.25	134	197	2.85	109	163	3.65	94	141
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	196	313	1.85	161	239	2.15	138	204	2.75	111	167	3.55	95	142
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	209	323	1.75	173	264	2.05	145	216	2.65	115	170	3.45	96	145
1.60	1.40	222	344	1.70			2.00			2.60			3.40		
1.65	1.35	239	388	1.65	184	289	1.95	153	227	2.55	117	176	3.35	97	148
1.70	1.30	256	442	1.60			1.90			2.50			3.30		
1.75	1.25	-	-	1.55	196	313	1.85	161	239	2.45	119	181	3.25	98	151
1.80	1.20			1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of $V_{BIAS} – V_{OUT(T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-4														
	DROPOUT VOLTAGE 4 (mV)														
	Vdif 4														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs(*1) (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)	
$V_{OUT\ (T)}$		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.
0.70	2.30	189	300	2.60	157	300	2.90	146	300	3.50	129	300	4.30	116	300
0.75	2.25	195	277	2.55	164	272	2.85	150	250	3.45	131	250	4.25	118	250
0.80	2.20			2.50			2.80			3.40		246	4.20		231
0.85	2.15	201	277	2.45	170	272	2.75	153	250	3.35	134	246	4.15	119	231
0.90	2.10			2.40			2.70			3.30			4.10		
0.95	2.05	206	277	2.35	189	272	2.65	157	250	3.25	136	246	4.05	121	231
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	218	277	2.25	195	272	2.55	164	250	3.15	139	246	3.95	125	231
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	231	227	2.15	201	272	2.45	170	250	3.05	142	246	3.85	128	231
1.20	1.80		334	2.10		277	2.40		248	3.00		215	3.80		189
1.25	1.75	248	376	2.05	206	296	2.35	189	255	2.95	146	219	3.75	128	191
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	264	418	1.95	218	315	2.25	195	266	2.85	150	224	3.65	129	193
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	281	460	1.85	231	334	2.15	201	277	2.75	153	228	3.55	129	195
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	-	-	1.75	248	376	2.05	206	296	2.65	157	234	3.45	131	198
1.60	1.40			1.70			2.00			2.60			3.40		
1.65	1.35	-	-	1.65	264	418	1.95	218	315	2.55	164	241	3.35	134	202
1.70	1.30			1.60			1.90			2.50			3.30		
1.75	1.25	-	-	1.55	281	460	1.85	231	334	2.45	170	248	3.25	136	205
1.80	1.20			1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of VBIAS – VOUT(T).

■OPERATIONAL EXPLANATION

<Voltage Regulator>

The voltage divided by resistors R1 & R2 is compared with the internal reference voltage by the error amplifier. The N-channel MOSFET which is connected to the V_{OUT} pin is then driven by the subsequent output signal. The output voltage at the V_{OUT} pin is controlled & stabilized by a system of negative feedback.

V_{BIAS} pin is power supply pin for output voltage control circuit, protection circuit and CE circuit. When output current increase, the V_{BIAS} pin supplies output current also. V_{IN} pin is connected to a driver transistor and provides output current.

In order to obtain highly efficient output current through low on-resistance, please take enough Vgs (=V_{BIAS} – $V_{OUT(T)}$) of the driver transistor. Output current triggers operation of constant current limiter and fold-back circuit, heat generation triggers operation of thermal shutdown circuit, the driver transistor circuit is forced OFF when V_{BIAS} or V_{IN} voltage goes lower than UVLO voltage. Further, the IC's internal circuitry can be shutdown via the CE pin's signal.

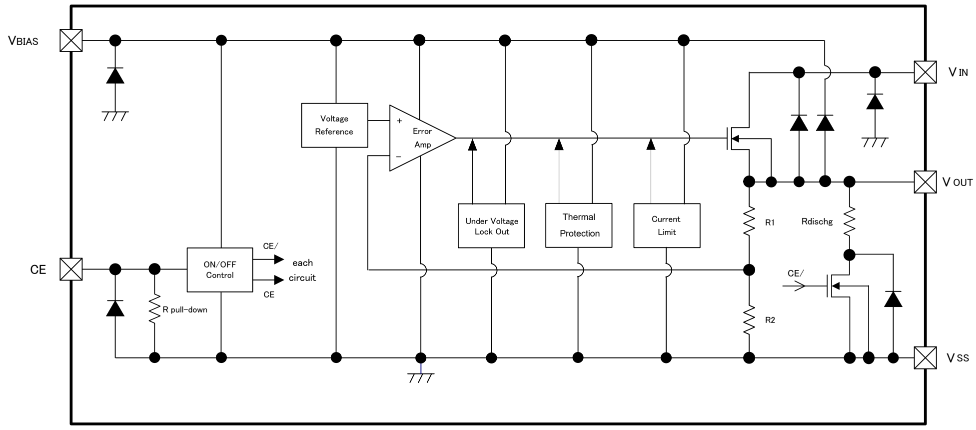


Figure1: XC6601A series

<Low ESR Capacitor>

With the XC6601 series, a stable output voltage is achievable even if used with low ESR capacitors, as a phase compensation circuit is built-in. The output capacitor (C_L) should be connected as close to V_{OUT} pin and V_{SS} pin to obtain stable phase compensation. Values required for the phase compensation are as the table below.

For a stable power input, please connect an bias capacitor (C_{BIAS}) of 1.0μF between the V_{BIAS} pin and the V_{SS} pin. Also, please connect an input capacitor (C_{IN}) of 1.0μF between the V_{IN} pin and the V_{SS} pin. In order to ensure the stable phase compensation while avoiding run-out of values, please use the capacitor (C_{BIAS}, C_{IN}, C_L) which does not depend on bias or temperature too much. The table below shows recommended values of C_{BIAS}, C_{IN}, C_L.

SETTING VOLTAGE	BIAS CAPACITOR	INPUT CAPACITOR	OUTPUT CAPACITOR
	C_{BIAS}	C_{IN}	C_L
0.7V ~ 1.8V	C_{BIAS}=1.0μF	C_{IN}=1.0μF	C_L=4.7μF

Recommended Values of C_{BIAS}, C_{IN}, C_L

■OPERATIONAL EXPLANATION (Continued)

<Soft-Start Function>

With the XC6601, the inrush current from V_{IN} to V_{OUT} for charging C_L at start-up can be reduced and makes the V_{IN} stable. The soft-start time is optimized to 240 μs (TYP.) at V_{OUT}=1.2V internally. Soft-start time is defined as the V_{OUT} reaches 90% of $V_{OUT(E)}$ from the time when CE H threshold 0.75V is input to the CE pin.

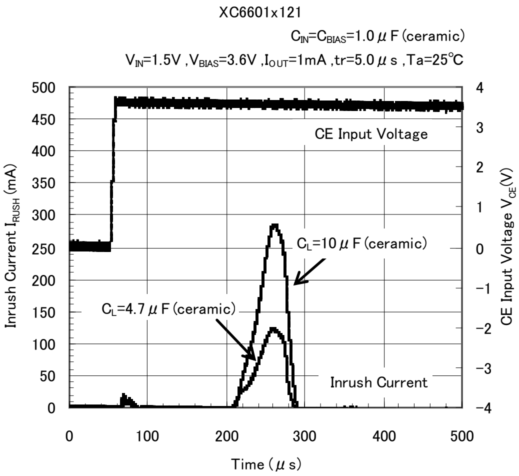


Figure2: Example of the inrush current wave form at IC start-up.

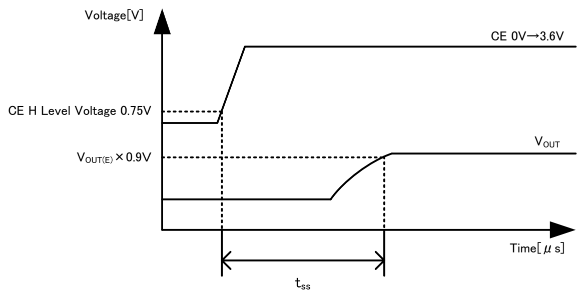


Figure3: Timing chart at IC start-up

<C_L High Speed Auto-Discharge>

XC6601 series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the EN pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the V_{OUT} pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it could avoids malfunction. At that time, CL discharge resistance is depended on a bias voltage. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R] and an output capacitor value (C_L) as τ (τ =C x R), the output voltage after discharge via the N channel transistor is calculated by the following formulas.

$V = V_{OUT} \times e^{-t/\tau}$, or $t = \tau \ln(V_{OUT(E)} / V)$

V : Output voltage after discharge, $V_{OUT(E)}$: Output voltage, t: Discharge time,

τ : C_L auto-discharge resistance R × Output capacitor (C_L) value C

<Current Limit, Short-Circuit Protection>

The XC6601 series' fold-back circuit operates as an output current limiter and a short protection of the output pin. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. When the output pin is shorted to the V_{SS} level, current flows about 80mA.

<Thermal Shutdown Circuit (TSD) >

When the junction temperature of the built-in driver transistor reaches the temperature limit level (150℃ TYP.), the thermal shutdown circuit operates and the driver transistor will be set to OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature (125℃ TYP.).

■OPERATIONAL EXPLANATION (Continued)

<Under Voltage Lock Out (UVLO) >

When the V_{BIAS} pin voltage drops below 2.0V (TYP.) or V_{IN} pin voltage drops below 0.4V (TYP.), the output driver transistor is forced OFF by UVLO function to prevent false output caused by unstable operation of the internal circuitry. When the V_{BIAS} pin voltage rise at 2.2V (TYP.) or the V_{IN} pin voltage rises at 0.4V (TYP.), the UVLO function is released. The driver transistor is turned in the ON state and start to operate voltage regulation.

<CE Pin>

The IC internal circuitry can be shutdown via the signal from the CE pin with the XC6601 series. In shutdown mode, output at the V_{OUT} pin will be pulled down to the V_{SS} level via R1 & R2. However, as for the XC6601 series, the CL auto-discharge resistor is connected in parallel to R1 and R2 while the power supply is applied to the V_{IN} pin. Therefore, time until the V_{OUT} pin reaches the V_{SS} level becomes short.

The CE pin of XC6601A has pull-down circuitry so that CE input current increase during IC operation. The CE pin of XC6601B does not have pull-down circuitry so that logic is not fixed when the CE pin is open. If the CE pin voltage is taken from V_{BIAS} pin or V_{SS} pin then logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry when medium voltage is input.

■NOTE ON USE

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.

2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{BIAS} and V_{SS} wiring or V_{IN} and V_{SS} wiring in particular.

3. Please wire the bias capacitor (C_{BIAS}), input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

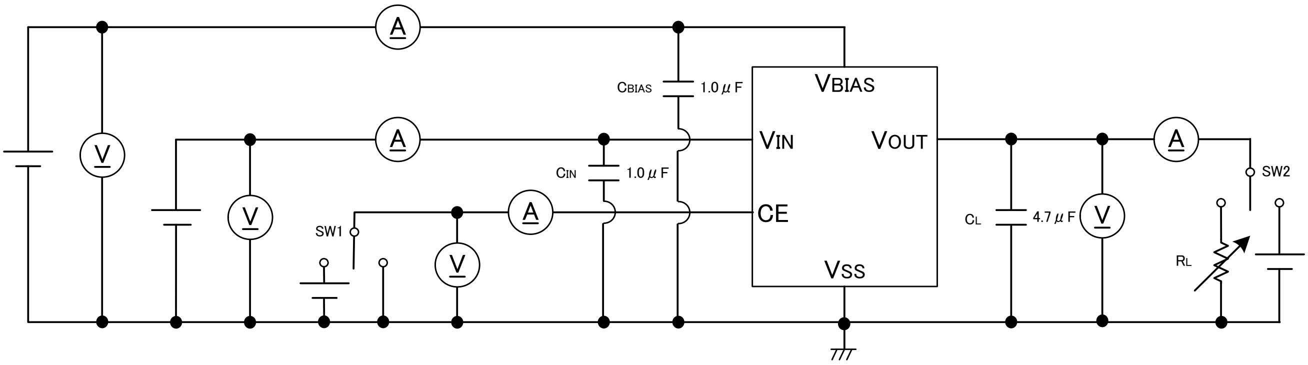
4. Capacitance values of these capacitors ($C_{BIAS,}$ $C_{IN,}$ C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.

5. In case of the output capacitor more than C_L=22μF is used, ringing of input current occurs when rising time.

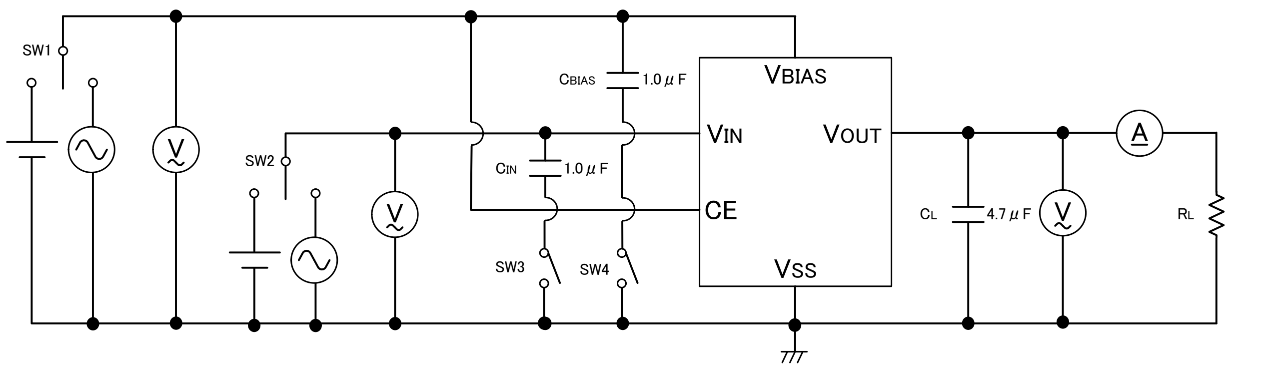
6. V_{IN} and CE should be applied at least 10μs after the bias voltage V_{BIAS} reaches the requested voltage.
   If V_{IN} and CE are applied within 10μs, inrush current like 1A may occurs.

■TEST CIRCUITS

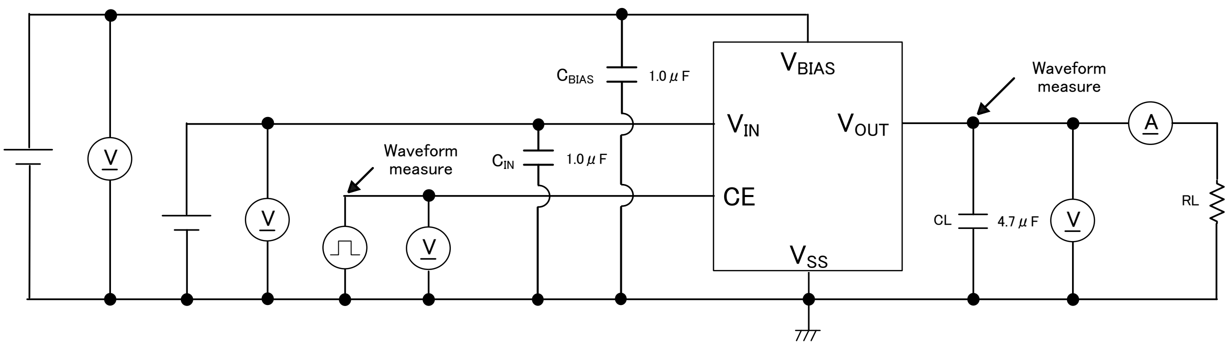
Circuit ①



Circuit ②



Circuit ③



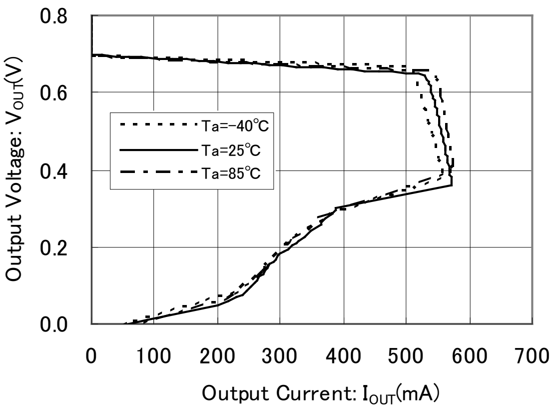
* For the timing chart, please refer to page 12 <Soft-Start Function>.

■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs. Output Current

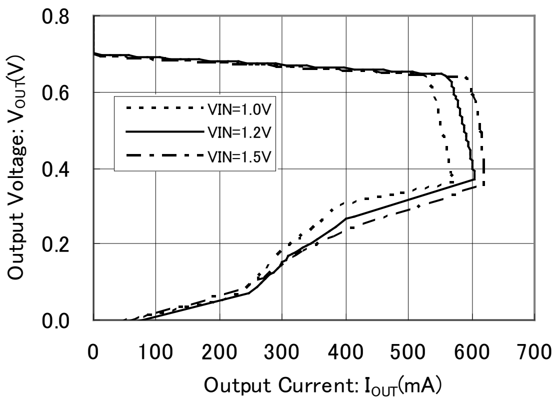
XC6601B071MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.0V



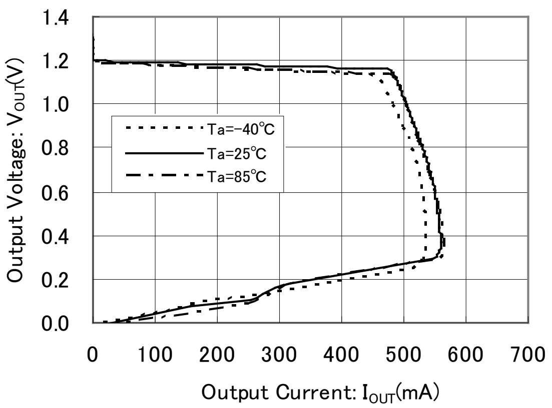
XC6601B071MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, Ta=25℃



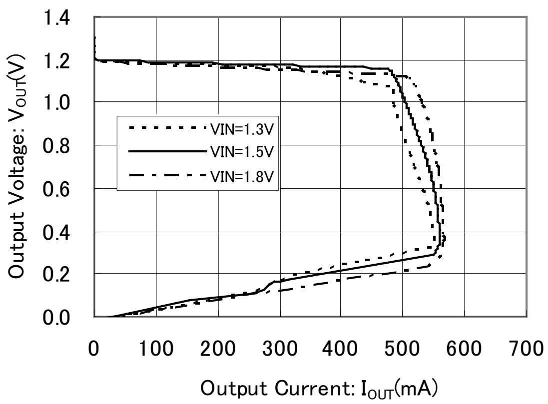
XC6601B121MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.5V



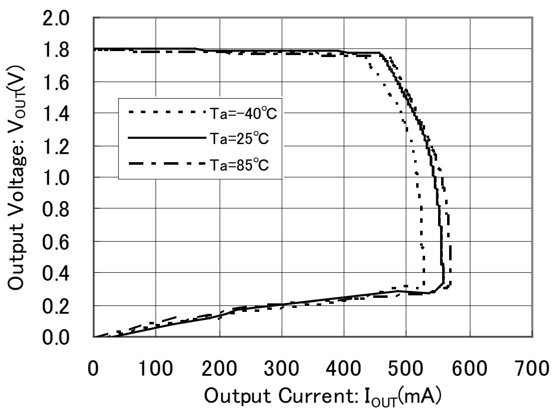
XC6601B121MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, Ta=25℃



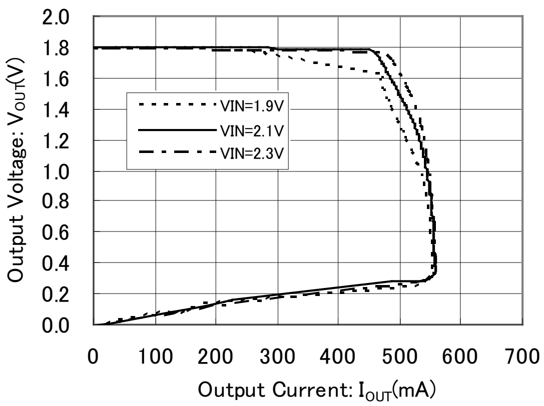
XC6601B181MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, V_{IN}=2.1V



XC6601B181MR

C_{IN}=C_{BIAS}=1.0 μ F(ceramic), C_L=4.7 μ F(ceramic)
V_{BIAS}=3.6V, Ta=25℃

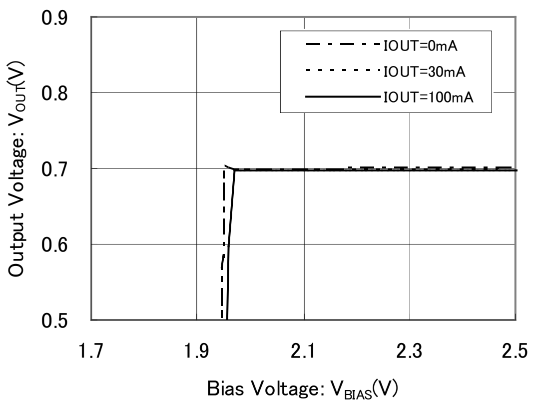


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Bias Voltage

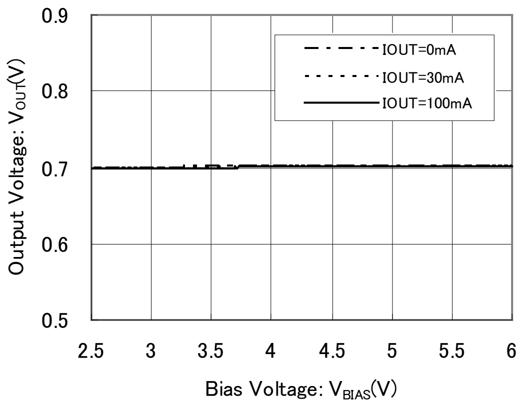
XC6601x071

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=1.0V$, Ta=25℃



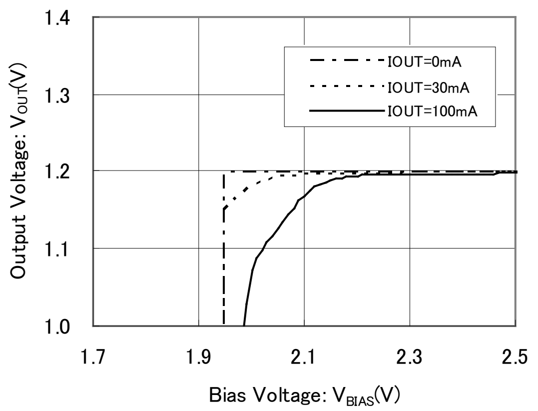
XC6601x071

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=1.0V$, Ta=25℃



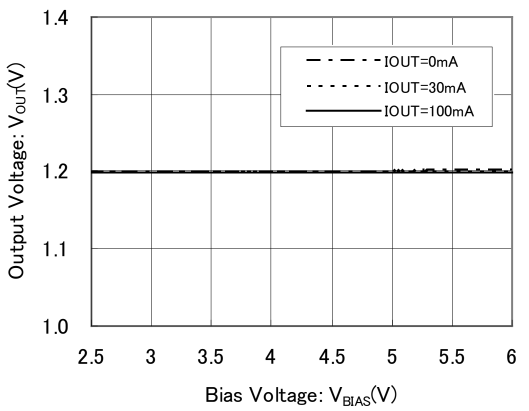
XC6601x121

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=1.5V$, Ta=25℃



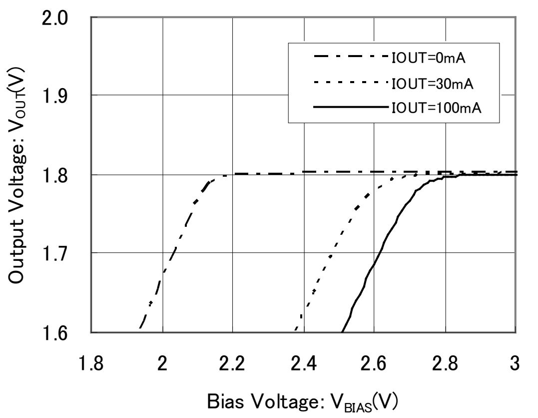
XC6601x121

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=1.5V$, Ta=25℃



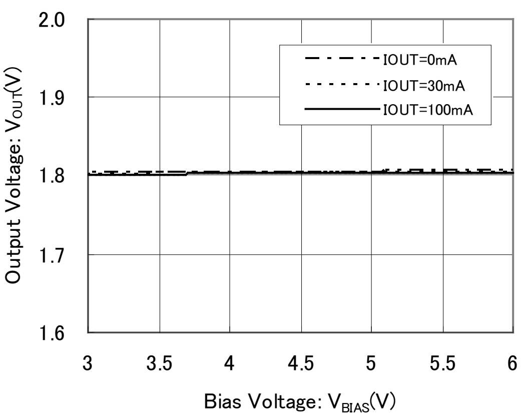
XC6601x181

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=2.1V$, Ta=25℃



XC6601x181

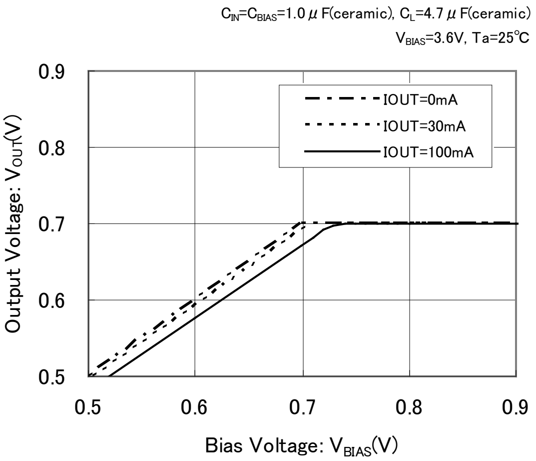
$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
$V_{IN}=2.1V$, Ta=25℃



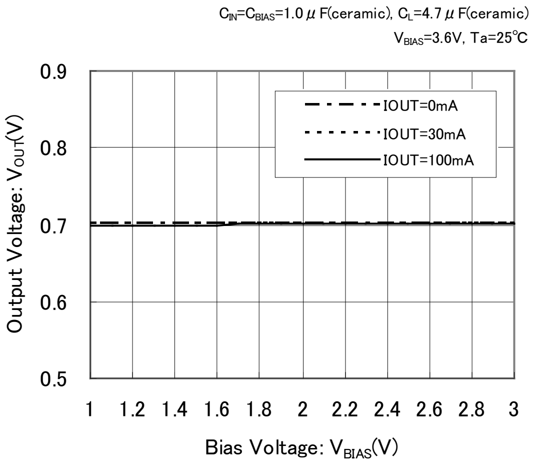
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Output Voltage vs. Input Voltage

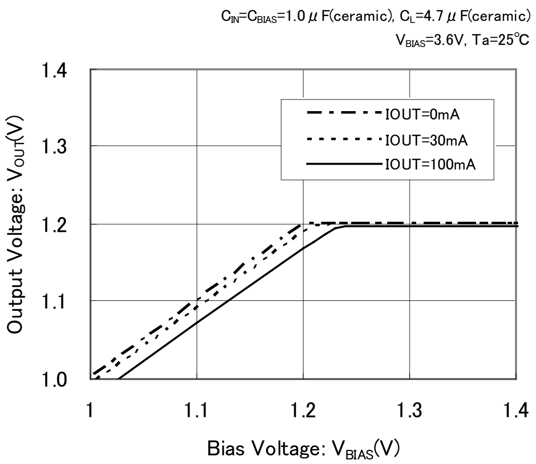
XC6601x071



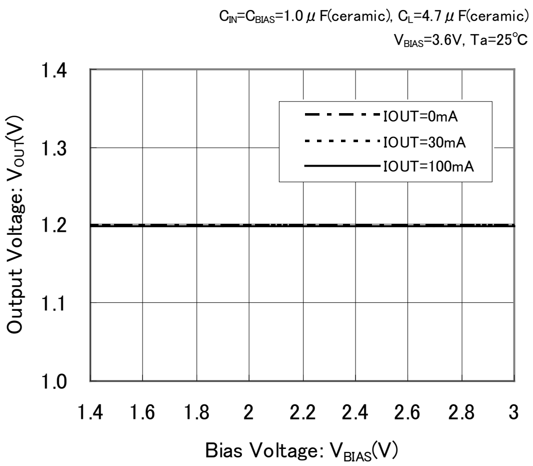
XC6601x071



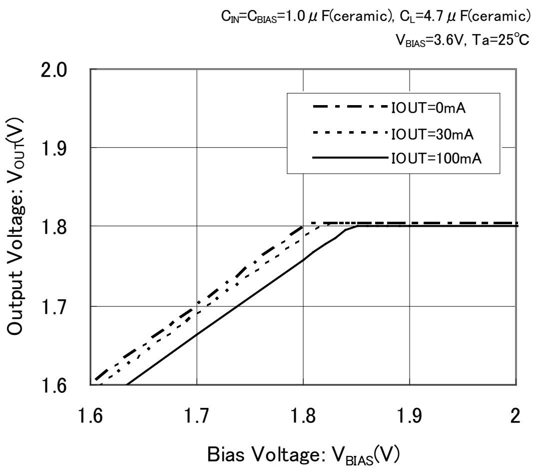
XC6601x121



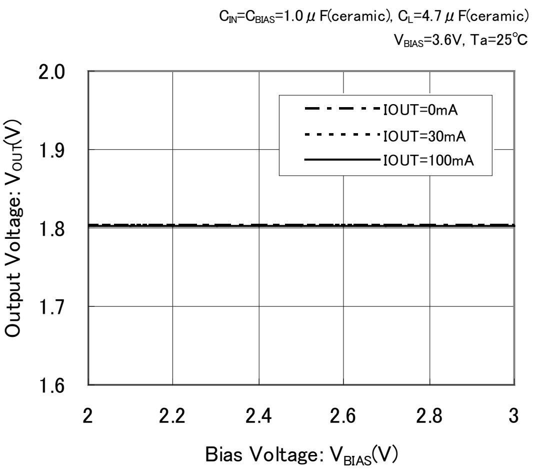
XC6601x121



XC6601x181



XC6601x181

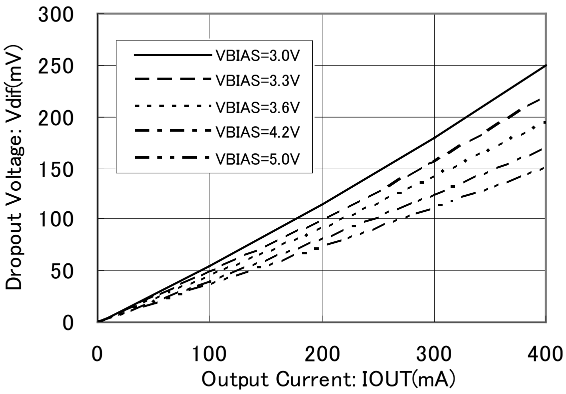


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4)Dropout Voltage vs. Output Current

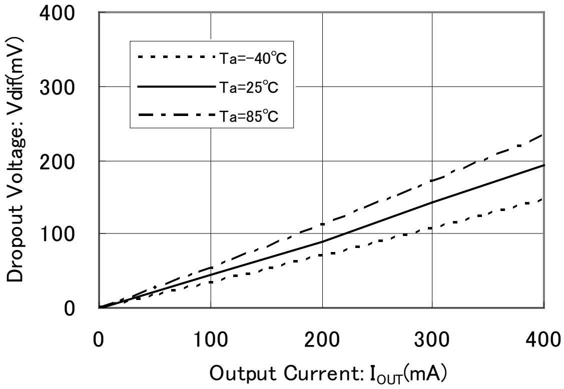
XC6601B121MR

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
Ta=25℃



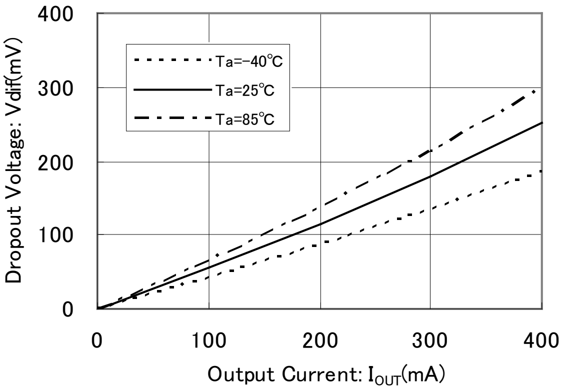
XC6601B121MR (Vgs(*1)=2.4V)

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
V_{BIAS}=3.6V



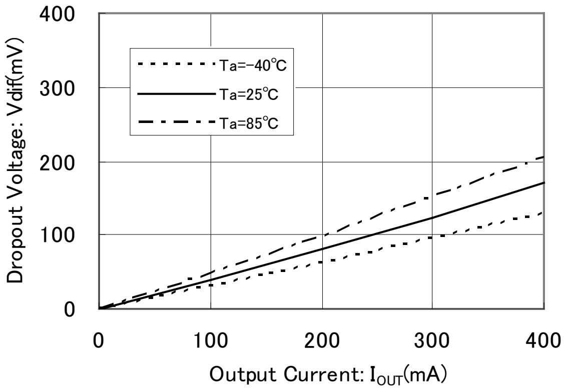
XC6601B121MR (Vgs(*1)=1.8V)

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
V_{BIAS}=3.0V



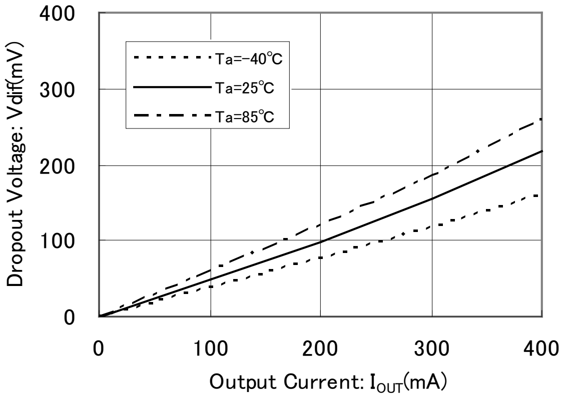
XC6601B121MR (Vgs(*1)=3.0V)

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
V_{BIAS}=4.2V



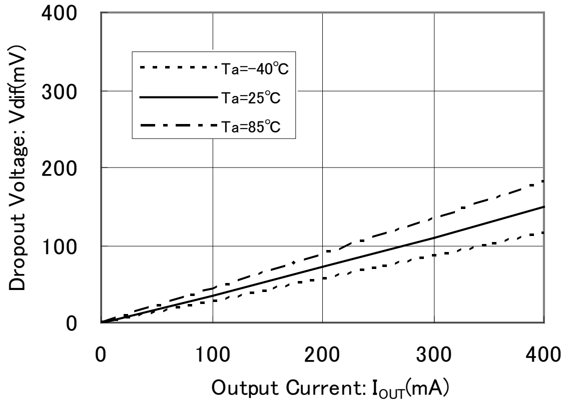
XC6601B121MR (Vgs(*1)=2.1V)

$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
V_{BIAS}=3.3V



XC6601B121MR (Vgs(*1)=3.8V)

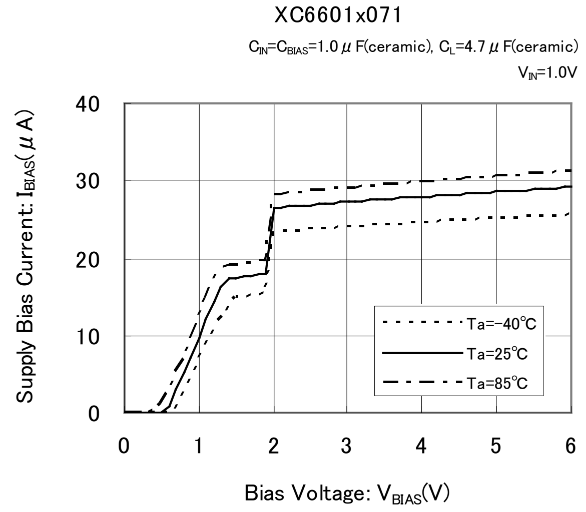
$C_{IN}=C_{BIAS}=1.0\mu F$(ceramic), $C_L=4.7\mu F$(ceramic)
V_{BIAS}=5.0V

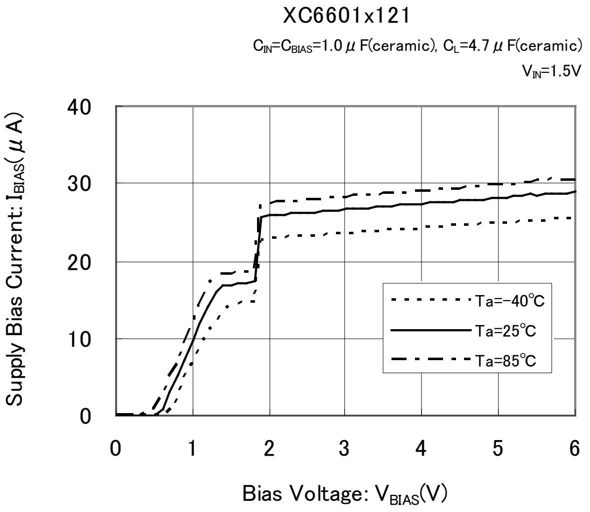


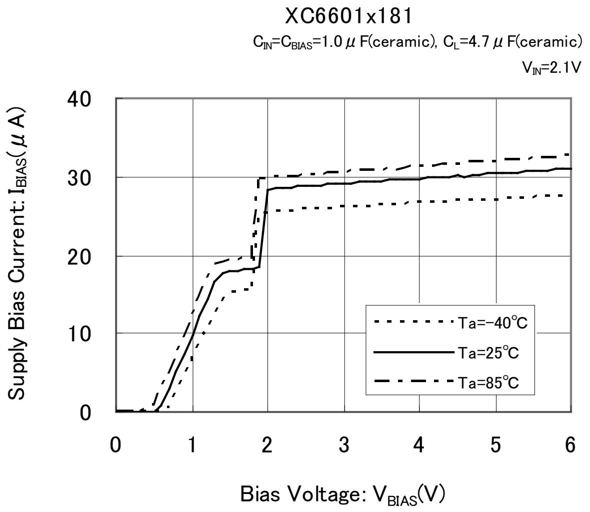
*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - V_{OUT} (T).
A value of the dropout voltage is determined by the value of the Vgs.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

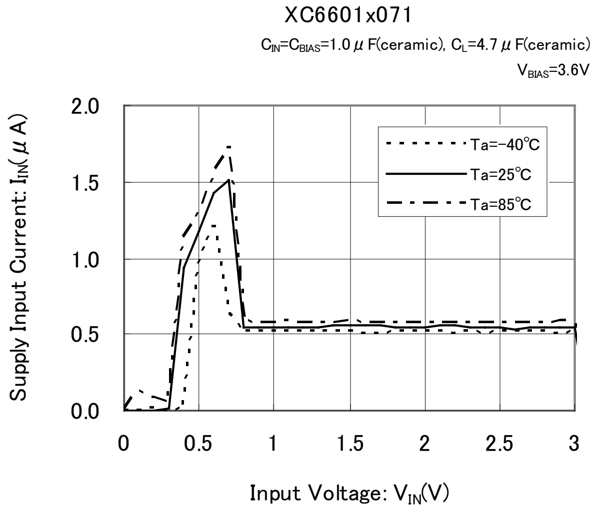
(5) Supply Bias Current vs. Bias Voltage

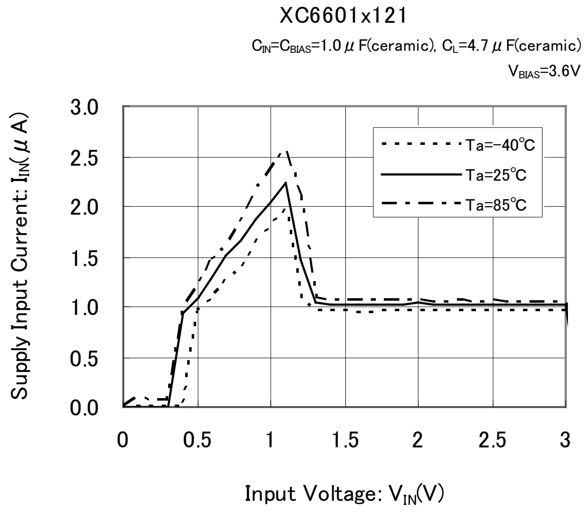


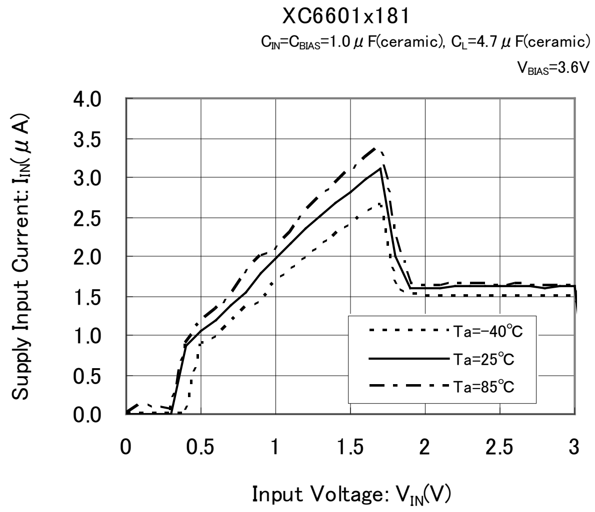




(6) Supply Input Current vs. Input Voltage



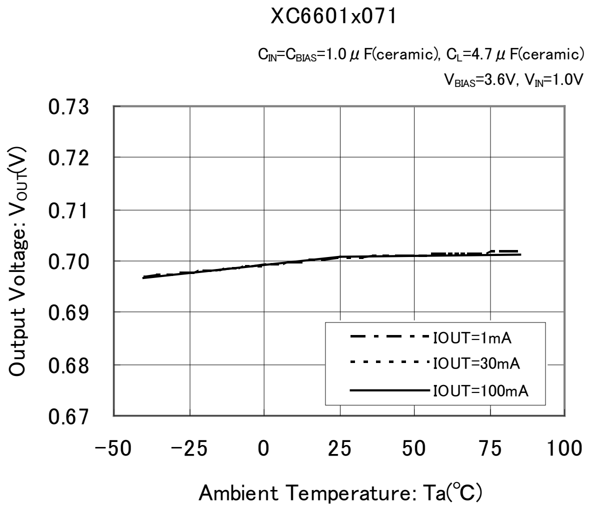


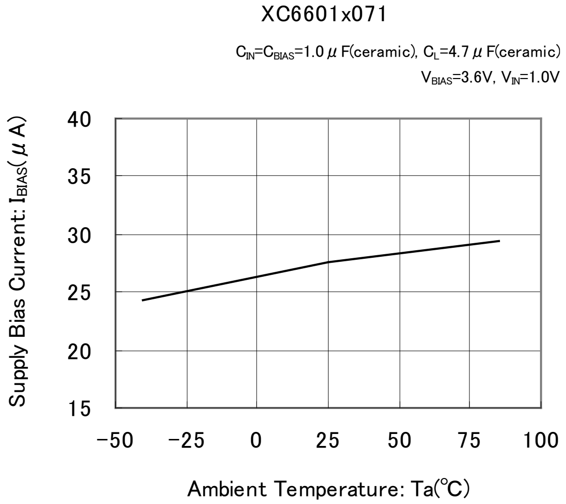


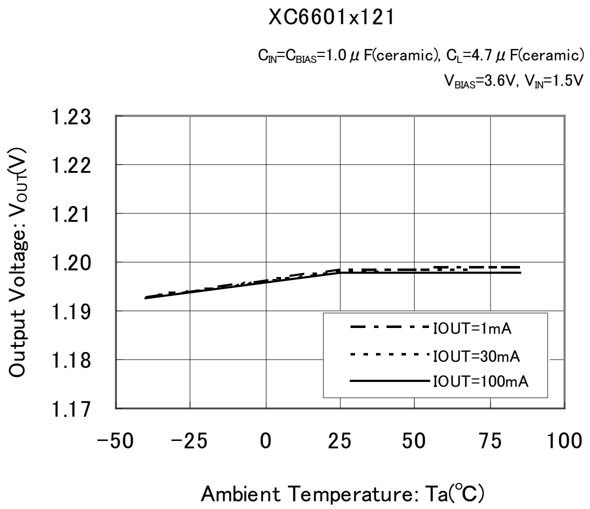
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

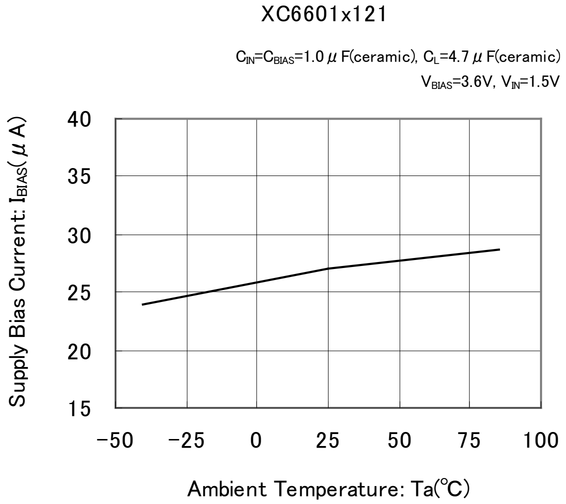
(7) Output Voltage vs. Ambient Temperature

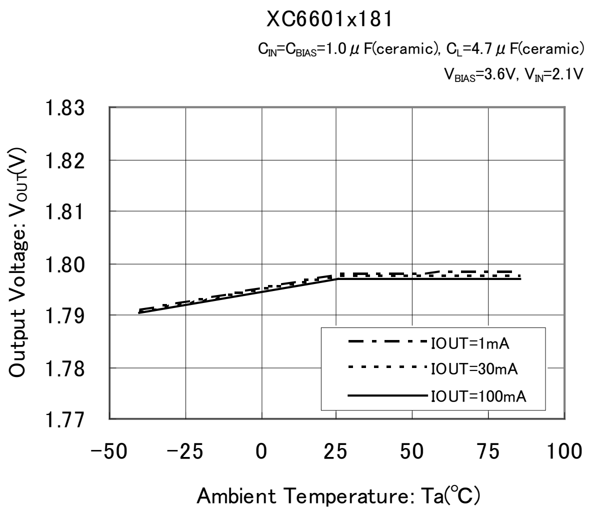
(8) Supply Bias Current vs. Ambient Temperature

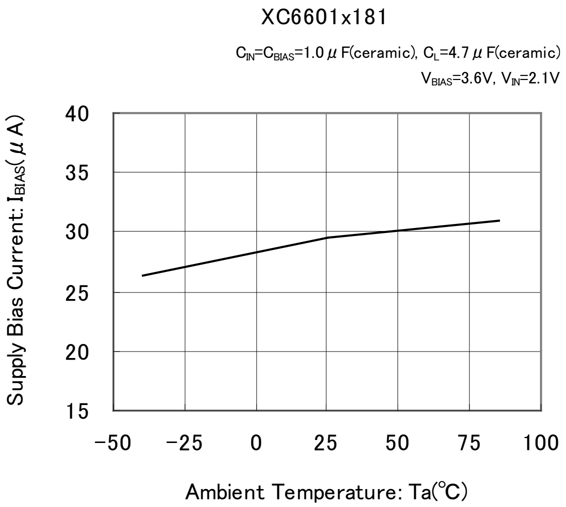






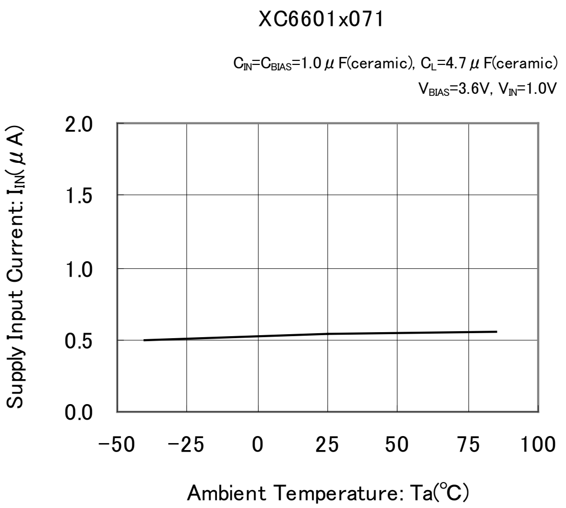


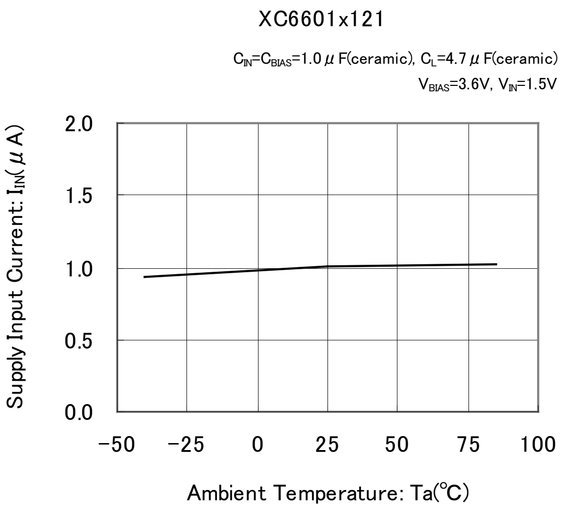


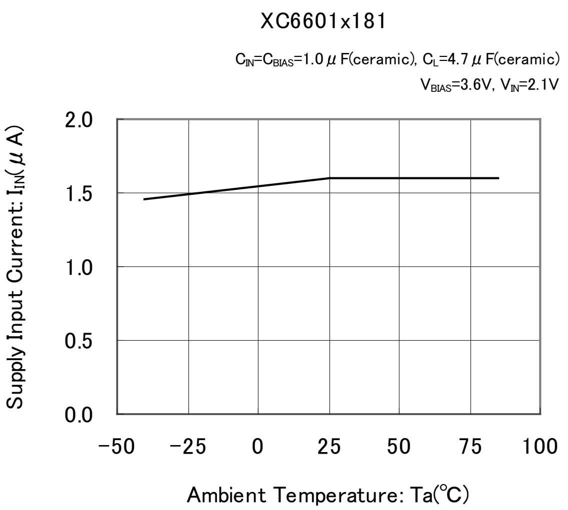


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(9) Supply Input Current vs. Ambient Temperature

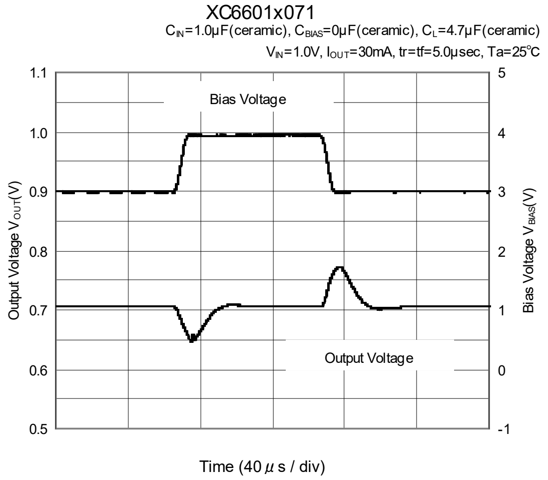


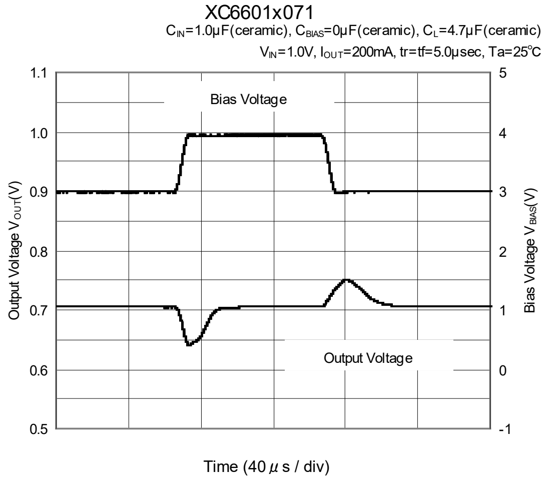


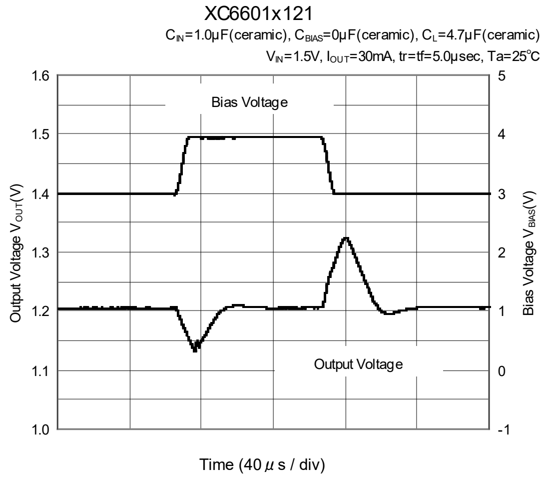


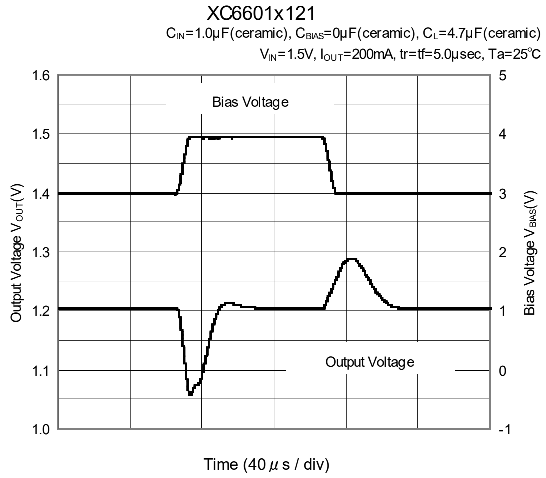
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

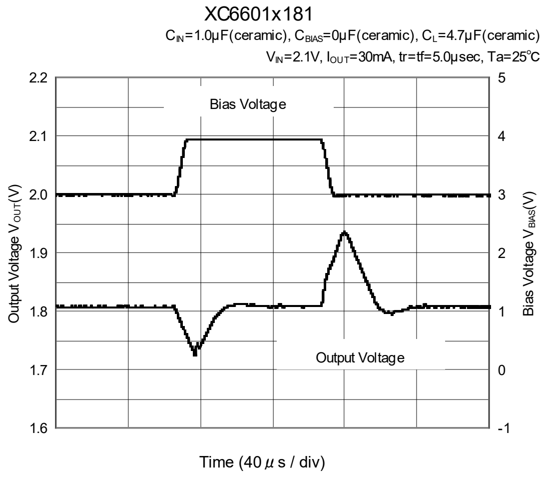
(10) Bias Transient Response

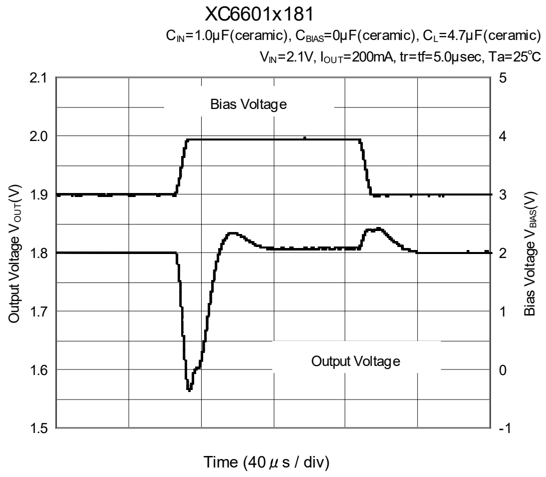






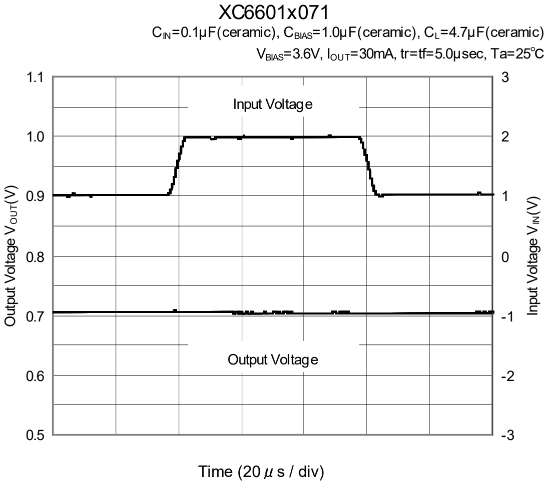


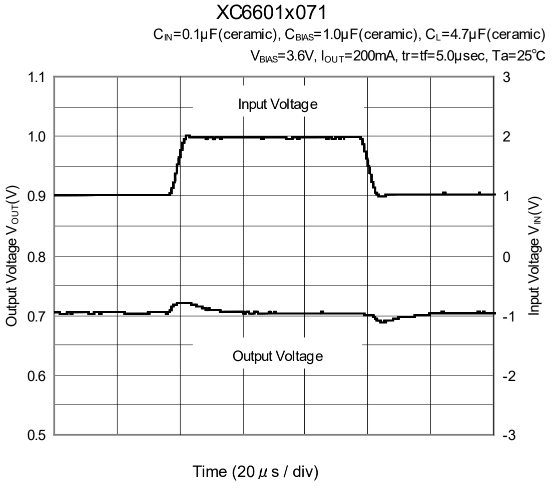


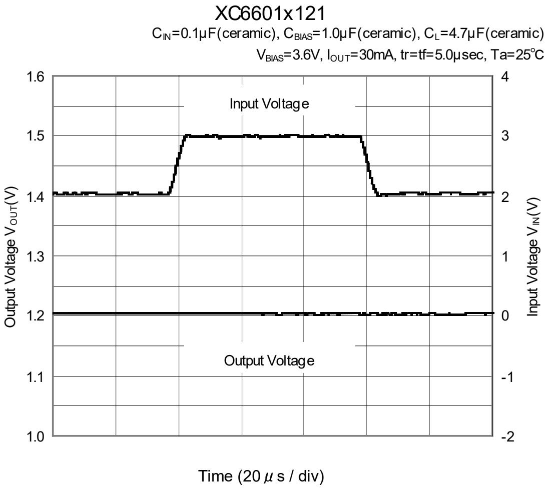


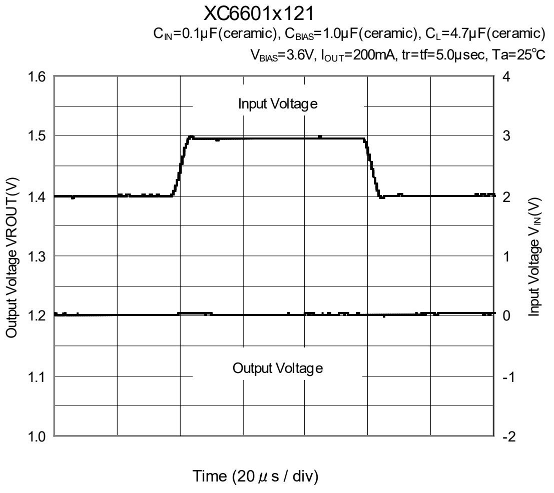
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

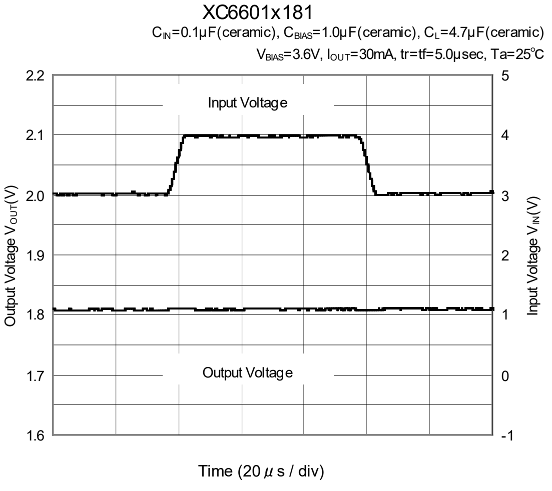
(11) Input Transient Response

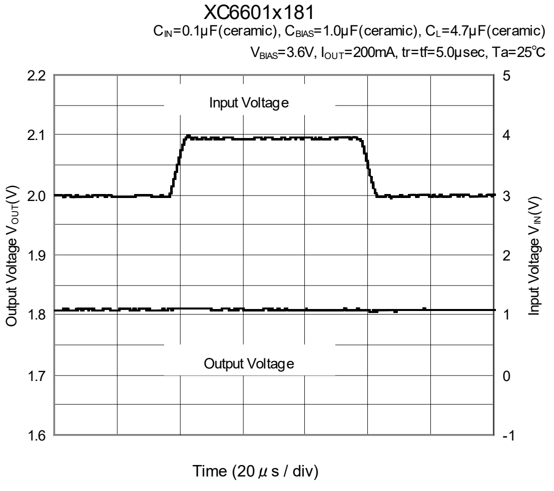










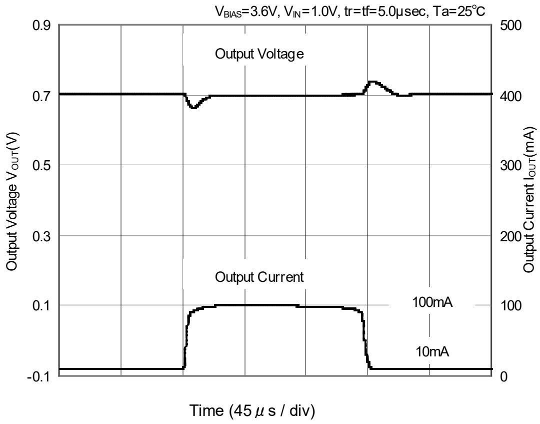


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(12) Load Transient Response

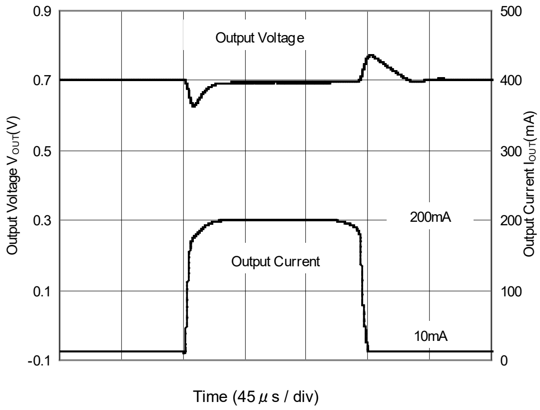
XC6601B071MR

$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.0V, tr=tf=5.0μsec, Ta=25℃



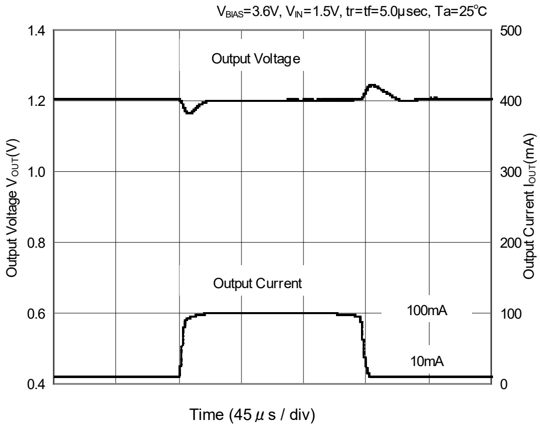
XC6601B071MR

$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.0V, tr=tf=5.0μsec, Ta=25℃



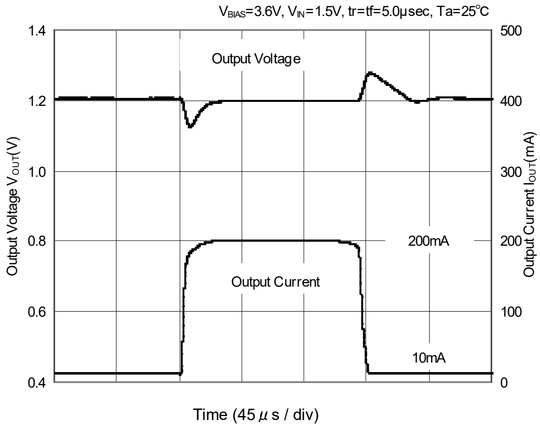
XC6601B121MR

$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.5V, tr=tf=5.0μsec, Ta=25℃



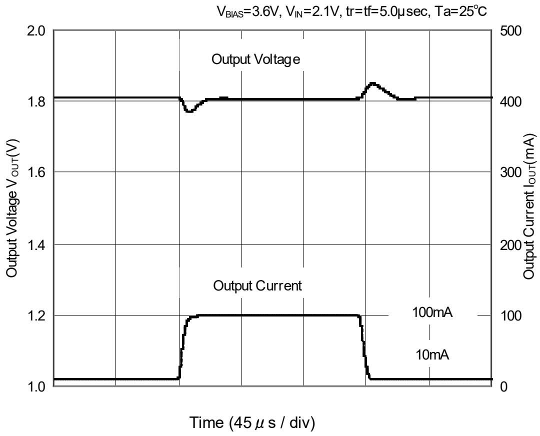
XC6601B121MR

$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.5V, tr=tf=5.0μsec, Ta=25℃



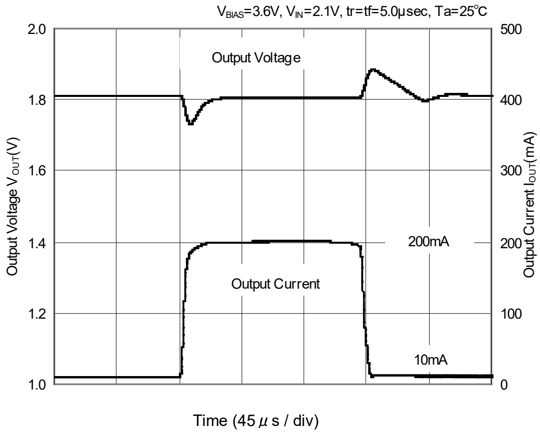
XC6601B181MR

$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=2.1V, tr=tf=5.0μsec, Ta=25℃



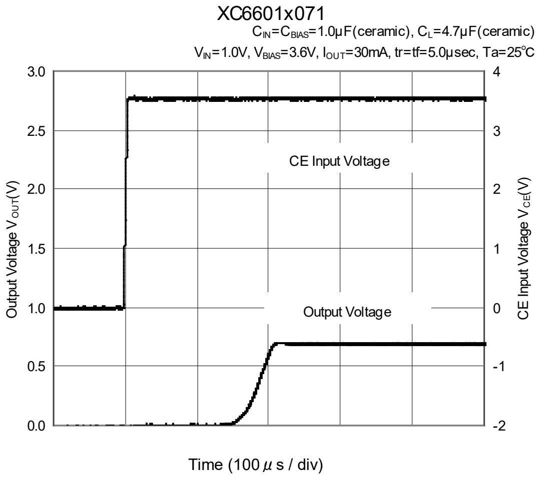
XC6601B181MR

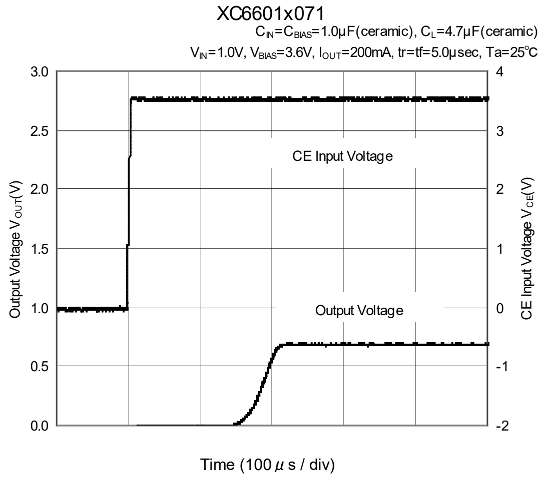
$C_{IN}=C_{BIAS}$=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=2.1V, tr=tf=5.0μsec, Ta=25℃

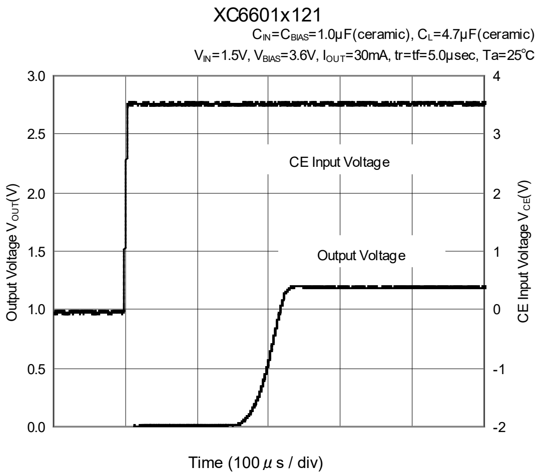


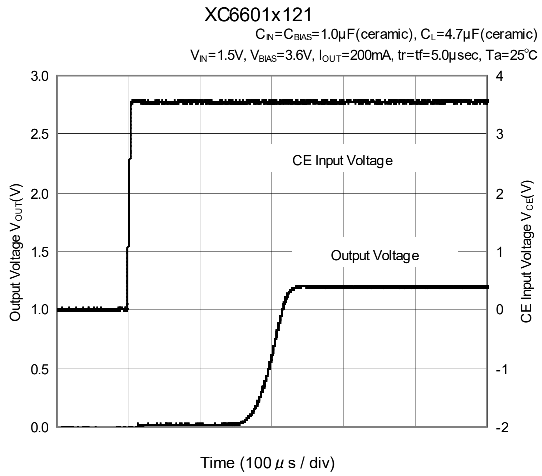
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

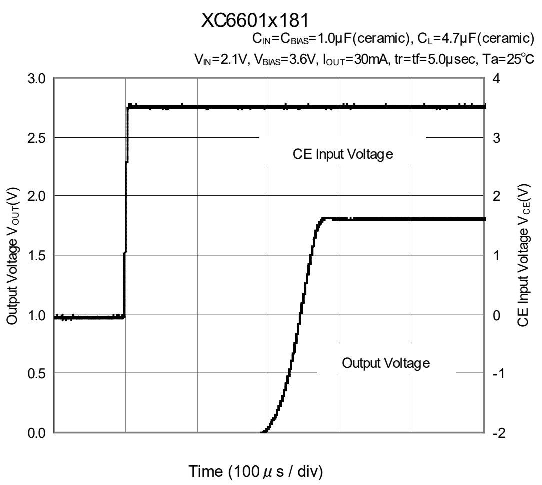
(13) CE Rising Response Time

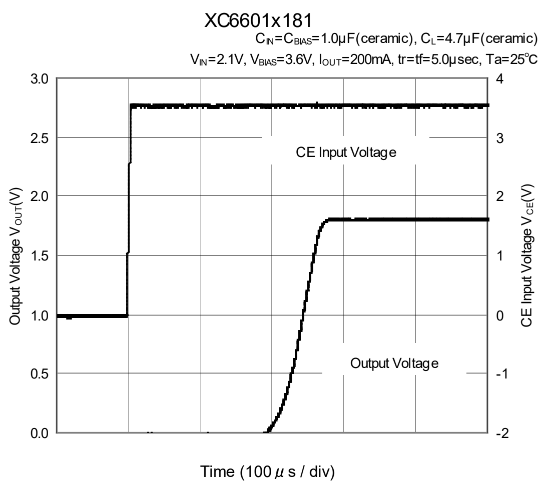






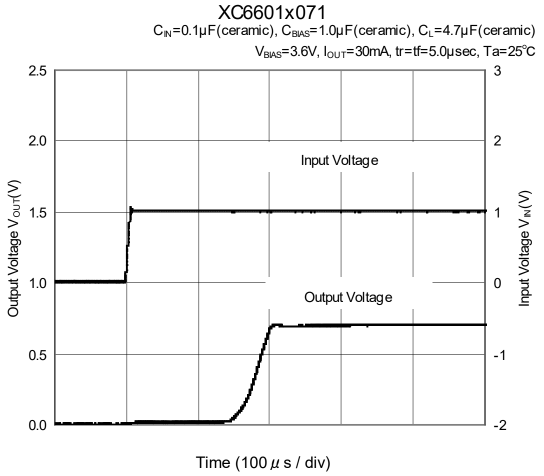


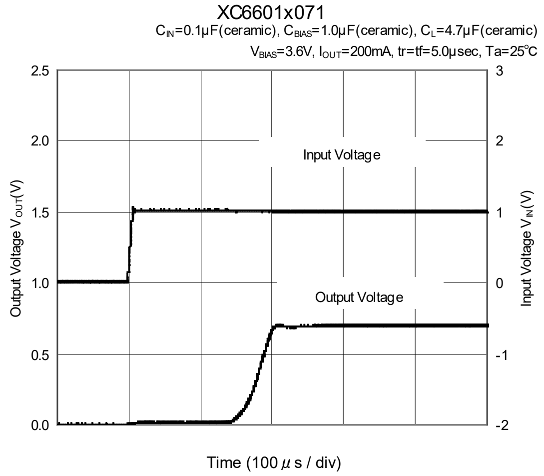


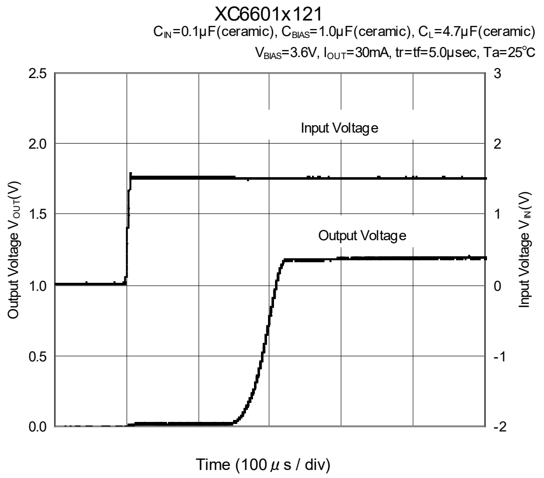


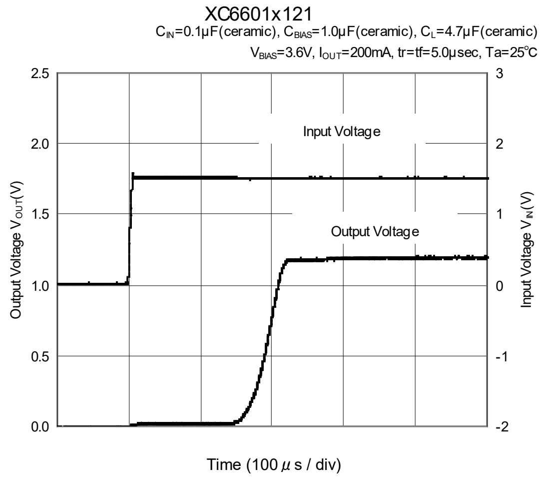
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

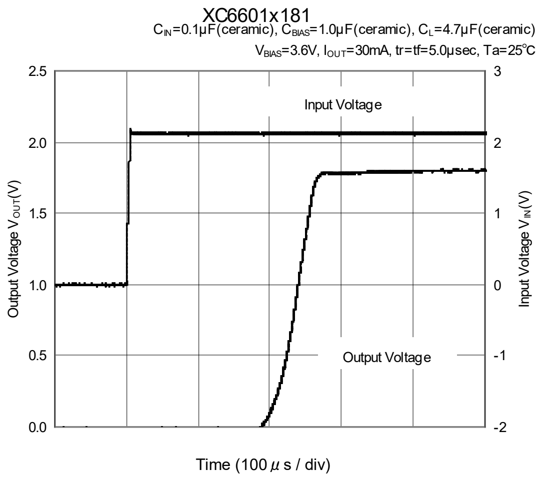
(14) V_{IN} Rising Response Time

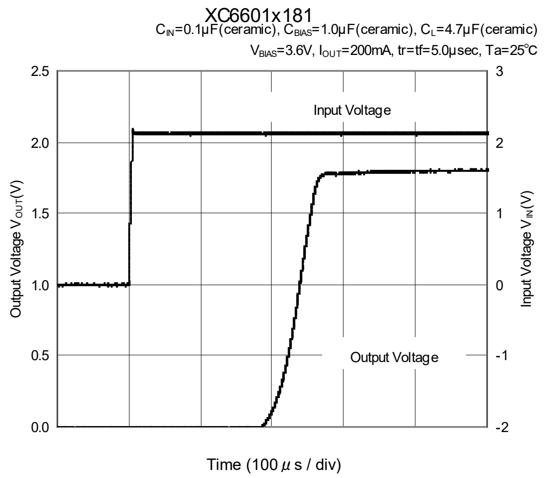










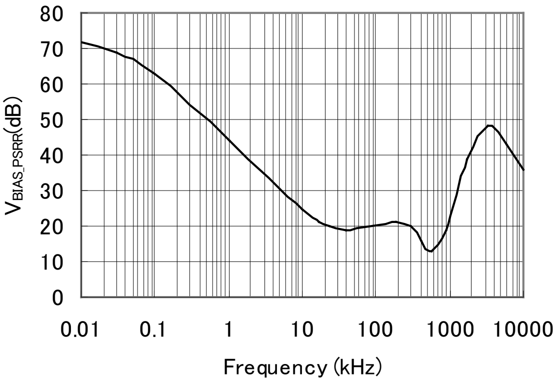


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Bias Voltage Ripple Rejection Rate

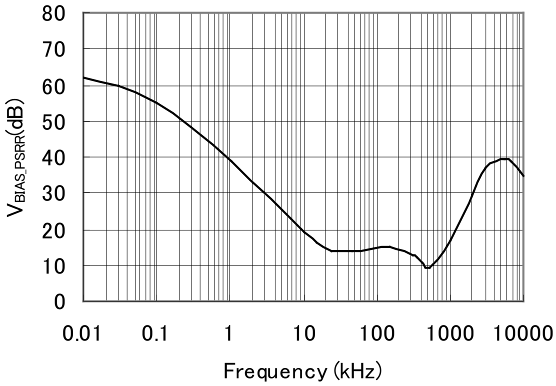
XC6601x071

C_{BIAS}=0μF, C_{IN}=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V_{DC}+0.2Vp-p_{AC}, V_{IN}=1.0V, I_{OUT}=30mA, Ta=25℃



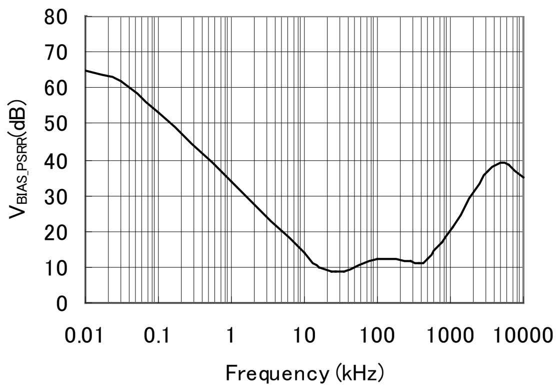
XC6601x121

C_{BIAS}=0μF, C_{IN}=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V_{DC}+0.2Vp-p_{AC}, V_{IN}=1.5V, I_{OUT}=30mA, Ta=25℃



XC6601x181

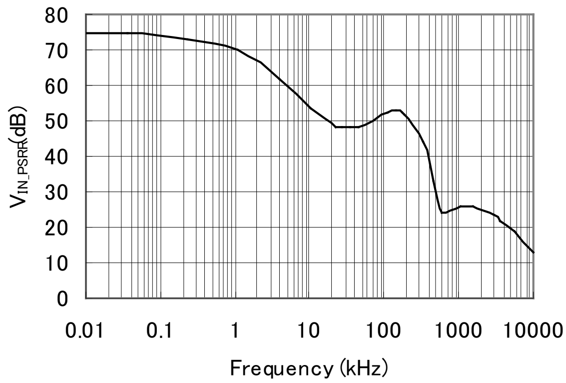
C_{BIAS}=0μF, C_{IN}=1.0μF(ceramic), C_L=4.7μF(ceramic)
V_{BIAS}=3.6V_{DC}+0.2Vp-p_{AC}, V_{IN}=2.1V, I_{OUT}=30mA, Ta=25℃



(16) Input Voltage Ripple Rejection Rate

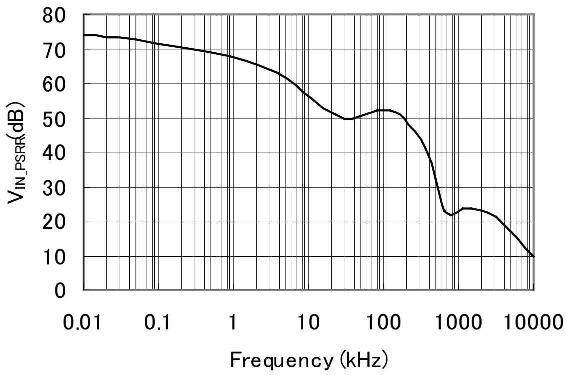
XC6601x071

C_{BIAS}=1.0μF(ceramic), C_{IN}=0μF, C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.0V_{DC}+0.2Vp-p_{AC}, IOUT=30mA, Ta=25℃



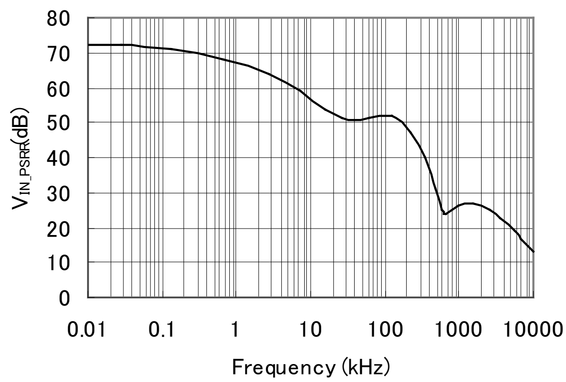
XC6601x121

C_{BIAS}=1.0μF(ceramic), C_{IN}=0μF, C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=1.5V_{DC}+0.2Vp-p_{AC}, IOUT=30mA, Ta=25℃



XC6601x181

C_{BIAS}=1.0μF(ceramic), C_{IN}=0μF, C_L=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN}=2.1V_{DC}+0.2Vp-p_{AC}, IOUT=30mA, Ta=25℃



■PACKAGING INFORMATION

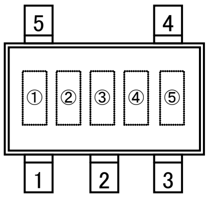
For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-25	SOT-25 PKG	SOT-25 Power Dissipation
SOT-89-5	SOT-89-5 PKG	SOT-89-5 Power Dissipation
USP-6C	USP-6C PKG	USP-6C Power Dissipation

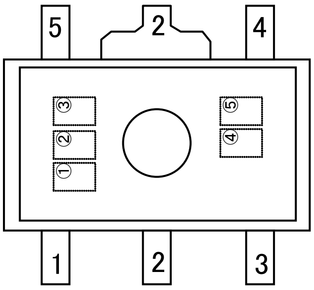
■MARKING RULE

●SOT25, 89-5, USP6C

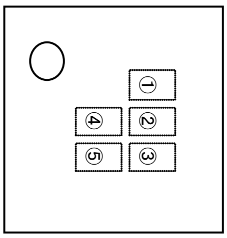
SOT25



SOT89-5



USP6C



① represents product series

MARK	PRODUCT SERIES
9	XC6601******

② represents type of regulators

MARK	OUTPUT VOLTAGE RANGE
A	XC6601A*****
B	XC6601B*****

③ represents output voltage

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
0	0.7	F	1.45
1	0.75	H	1.5
2	0.8	K	1.55
3	0.85	L	1.6
4	0.9	M	1.65
5	0.95	N	1.7
6	1.0	P	1.75
7	1.05	R	1.8
8	1.1	S	-
9	1.15	T	-
A	1.2	U	-
B	1.25	V	-
C	1.3	X	-
D	1.35	Y	-
E	1.4	Z	-

④,⑤ represents production lot number
01～09、0A～0Z、11･･･9Z、A1～A9、
AA･･･Z9、ZA～ZZ repeated
(G, I, J, O, Q, W excluded)
*No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

TOREX SEMICONDUCTOR LTD.