

## Ultra-Low Quiescent Current Voltage Regulator (with Stand-by Function)

### ■ GENERAL DESCRIPTION

The XD6506 series are positive voltage LDO regulators manufactured using CMOS processes. The series achieves Ultra low supply current,  $0.8 \mu\text{A}$  (TYP.) and consists of a reference voltage source, an error amplifier, a current fold-back circuit, and a phase compensation circuit plus a driver transistor.

The series is also compatible with low ESR ceramic capacitors, which give added output stability.

The current limiter's fold-back circuit also operates as a short protect for the output current limiter and the output pin.

Furthermore, the CE function allows the output of the regulator to be turned off, resulting in greatly reduced power consumption.

### ■ APPLICATIONS

- Car navigation systems
- Car audios
- Automotive ECU
- Other automotive equipment

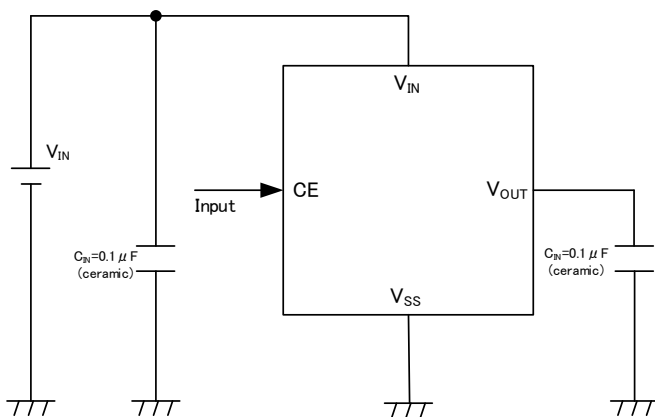
### ■ FEATURES

Maximum Output Current	:	150mA
Low Power Consumption	:	$0.8 \mu\text{A}$
Stand-by Current	:	Less than $0.1 \mu\text{A}$
Dropout Voltage	:	$360\text{mV}@I_{\text{OUT}}=100\text{mA}$ ( $V_{\text{OUT}}=3.3\text{V}$ )
Operating Input Voltage	:	$1.5\text{V} \sim 6.0\text{V}$
Output Voltage Range	:	$1.2\text{V}, 1.5\text{V}, 1.8\text{V}, 2.5\text{V},$ $2.8\text{V}, 3.0\text{V}, 3.3\text{V}, 5.0\text{V}^{(*)}$
Output Accuracy	:	$\pm 2.0\%$ ( $1.5\text{V} < V_{\text{OUT}} \leq 5.0\text{V}$ ) $\pm 30\text{mV}$ ( $1.2 \leq V_{\text{OUT}} \leq 1.5\text{V}$ )
Protection function	:	Current limit
Low ESR Capacitor Compatible	:	Ceramic Capacitor Compatible
Operating Temperature Range	:	$-40^\circ\text{C} \sim +105^\circ\text{C}$
Packages	:	SOT-25
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

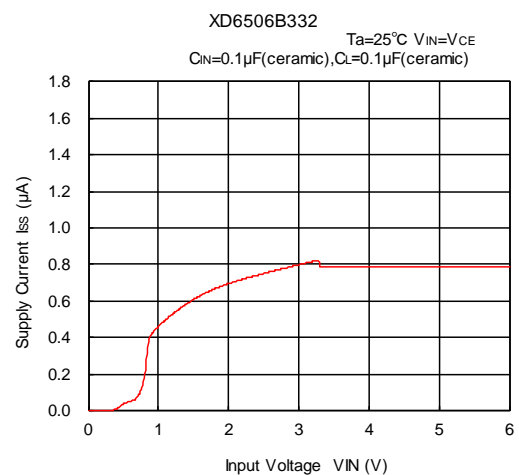
(\*) Output voltages can be set internally from 1.2V to 5.0V (Step 0.1V).

For other voltages, please contact your local Torex sales office or distribution.

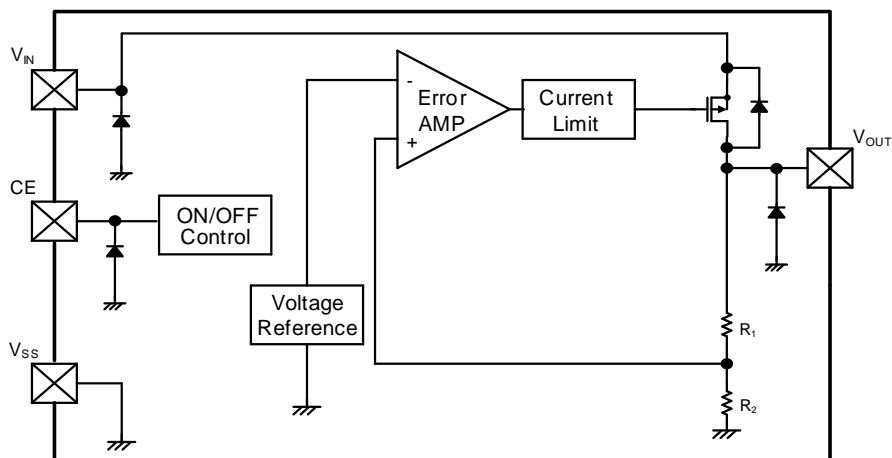
### ■ TYPICAL APPLICATION CIRCUIT



### ■ TYPICAL PERFORMANCE CHARACTERISTICS



## ■ BLOCK DIAGRAMS



\* Diodes shown in the above circuit are ESD protection diodes and parasitic diodes

## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

XD6506 ①②③④⑤⑥-⑦<sup>(\*)</sup>

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	TYPE	B	Refer to Selection Guide
②③	Output Voltage	12, 15, 18, 25, 28, 30, 33, 50 <sup>(*)2</sup>	e.g. 3.3V ⇒ 33, 5.0V ⇒ 50
④	Output Voltage Accuracy	2	±2% ( $V_{OUT} \geq 1.5V$ ) ±30mV ( $V_{OUT} < 1.5V$ )
⑤⑥-⑦ <sup>(*)1</sup>	Packages (Order Unit)	MR-Q	SOT-25 (3,000pcs/Reel)

<sup>(\*)1</sup> The "-Q" suffix denotes "AEC-Q100" and "Halogen and Antimony free" as well as being fully EU RoHS compliant.

<sup>(\*)2</sup> Output voltages can be set internally from 1.2V to 5.0V (Step 0.1V). For other voltages, please contact your local Torex sales office or distribution.

### ● Selection Guide

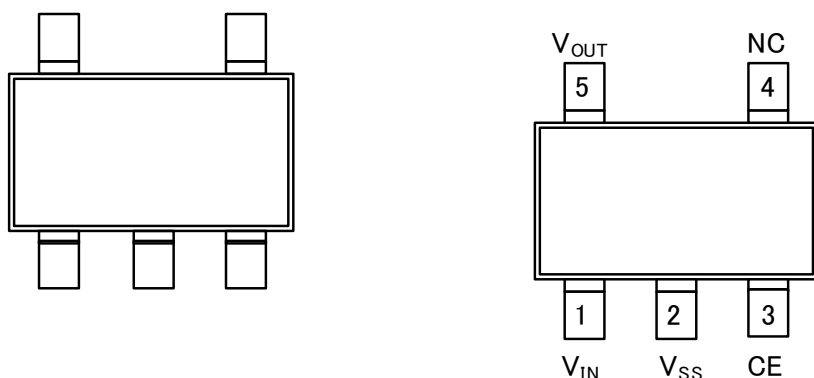
TYPE	CE function
B	Yes

## ■ STANDARD VOLTAGE

### ● Examples for standard voltage

V <sub>OUT</sub> (V)	PACKAGES
	SOT-25
1.2	XD6506B122MR-Q
1.5	XD6506B152MR-Q
1.8	XD6506B182MR-Q
2.5	XD6506B252MR-Q
2.8	XD6506B282MR-Q
3.0	XD6506B302MR-Q
3.3	XD6506B332MR-Q
5.0	XD6506B502MR-Q

## ■ PIN CONFIGURATION



SOT-25  
(TOP VIEW)

## ■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
SOT-25		
1	V <sub>IN</sub>	Power Supply Input
2	V <sub>SS</sub>	Ground
3	CE	ON/OFF Control
4	NC	No Connection
5	V <sub>OUT</sub>	Output

## ■ FUNCTION

PIN NAME	DESIGNATOR	IC OPERATION
CE	L	Stand-by
	H	Active
	OPEN	Undefined state *

\* Please do not leave the CE pin open.

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS	
V <sub>IN</sub> Pin Voltage	V <sub>IN</sub>	-0.3 ~ +7.0	V	
Output Voltage	V <sub>OUT</sub>	-0.3 ~ V <sub>IN</sub> + 0.3 or +7.0 <sup>(*)</sup>	V	
CE Input Voltage	V <sub>CE</sub>	-0.3 ~ +7.0	V	
Power Dissipation (T <sub>a</sub> =25°C)	SOT-25	P <sub>d</sub>	250	mW
			600 (40mm x 40mm Standard board) <sup>(*)</sup>	
			760 (JESD51-7 board) <sup>(*)</sup>	
Operating Ambient Temperature	T <sub>opr</sub>	-40 ~ +105	°C	
Storage Temperature	T <sub>stg</sub>	-55 ~ +125	°C	

All voltages are described based on the V<sub>SS</sub>.

<sup>(\*)</sup> The maximum rating corresponds to the lowest value between V<sub>IN</sub>+0.3V or +7.0V.

<sup>(\*)</sup> The power dissipation figure shown is PCB mounted and is for reference only.

The mounting condition is please refer to PACKAGING INFORMATION.

## ELECTRICAL CHARACTERISTICS

Ta=25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	$V_{OUT(E)}^{(*)2}$	$I_{OUT}=1mA$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	E-0			V	①
Maximum Output Current	$I_{OUTMAX}$	$V_{OUT(T)}=1.2V \sim 2.4V$ $V_{IN}=V_{CE}=V_{OUT(T)}+2.0V$ $V_{OUT(T)} \geq 2.5V$ $V_{IN}=V_{CE}=V_{OUT(T)}+1.0V$	150	-	-	mA	①
Load Regulation	$\Delta V_{OUT}$	$V_{OUT(T)}=1.2V \sim 1.3V$ $1mA \leq I_{OUT} \leq 80mA$ $V_{OUT(T)} \geq 1.4V$ $1mA \leq I_{OUT} \leq 100mA$	-	15	70	mV	①
Dropout Voltage	$V_{dif}^{(*)3}$	$V_{OUT(T)}=1.2V \sim 1.3V$ $V_{CE}=V_{IN}, I_{OUT}=80mA$ $V_{OUT(T)} \geq 1.4V$ $V_{CE}=V_{IN}, I_{OUT}=100mA$	E-1			mV	①
Supply Current	$I_{SS}$	$V_{OUT(T)} \leq 3.9V$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$ $V_{OUT(T)} \geq 4.0V$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	-	0.8	1.5	μA	②
			-	-	1.8		
			-	1	2.1		
Stand-by Current	$I_{STB}$	$V_{IN}=6.0V, V_{CE}=V_{SS}$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	-	0.01	0.1	μA	②
			-	-	0.6		
Line Regulation	$\frac{\Delta V_{OUT}}{(\Delta V_{IN} \cdot V_{OUT})}$	$V_{OUT(T)}=1.2V, V_{CE}=V_{IN}$ $V_{OUT(T)}+0.5V \leq V_{IN} \leq 6.0V$ $I_{OUT}=1mA$ $V_{OUT(T)} \geq 1.3V, V_{CE}=V_{IN}$ $V_{OUT(T)}+0.5V \leq V_{IN} \leq 6.0V$ $I_{OUT}=30mA$	-	0.05	0.15	%/V	①
			-	0.05	0.15	%/V	①
Input Voltage	$V_{IN}$	$-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	1.5	-	6.0	V	-
Current Limit	$I_{LIM}$	$V_{OUT(T)}=1.2V \sim 2.4V$ $V_{OUT}=V_{OUT(E)} \times 0.95$ $V_{IN}=V_{CE}=V_{OUT(T)}+2.0V$ $V_{OUT(T)} \geq 2.5V$ $V_{OUT}=V_{OUT(E)} \times 0.95$ $V_{IN}=V_{CE}=V_{OUT(T)}+1.0V$	150	260	-	mA	①
			150	260	-		
Short Current	$I_{SHORT}$	$V_{OUT}=V_{SS}$	-	30	-	mA	①
CE "H" Level Voltage	$V_{CEH}$	$V_{IN}=V_{OUT(T)}+1.0V$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	1.0	-	6.0	V	③
CE "L" Level Voltage	$V_{CEL}$	$V_{IN}=V_{OUT(T)}+1.0V$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	-	-	0.3	V	③
CE "H" Level Current	$I_{CEH}$	$V_{IN}=V_{CE}=6.0V$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	-0.1	-	0.1	μA	②
CE "L" Level Current	$I_{CEL}$	$V_{IN}=6.0V$ $V_{CE}=V_{SS}$ $-40^{\circ}C \leq Ta \leq 105^{\circ}C^{(*)4}$	-0.1	-	0.1	μA	②

Unless otherwise stated,  $V_{IN}=V_{CE}=V_{OUT}+1.0V$ ,

NOTE:

(\*)1  $V_{OUT(T)}$ : Fixed output voltage

(\*)2  $V_{OUT(E)}$  = Effective output voltage

(i.e. the output voltage when " $V_{OUT(T)} + 1.0V$ " is provided at the  $V_{IN}$  pin while maintaining a certain  $I_{OUT}$  value).

(\*)3  $V_{dif} = \{V_{IN1} - V_{OUT1}\}$

$V_{OUT1}$  is the voltage equal to 98% output voltage when an amply stabilized  $V_{OUT(T)} + 1.0V$  are supplied to the  $V_{IN}$  pin.

$V_{IN1}$  is the input voltage when  $V_{OUT1}$  appears at the  $V_{OUT}$  pin while input voltage is gradually decreased.

(\*)4 The ambient temperature range ( $-40^{\circ}C \leq Ta \leq 105^{\circ}C$ ) is a design Value.

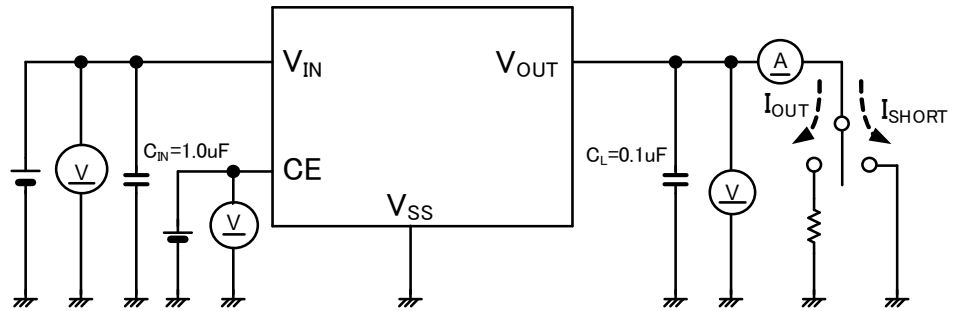
## ■ VOLTAGE CHART

● Voltage Chart 1

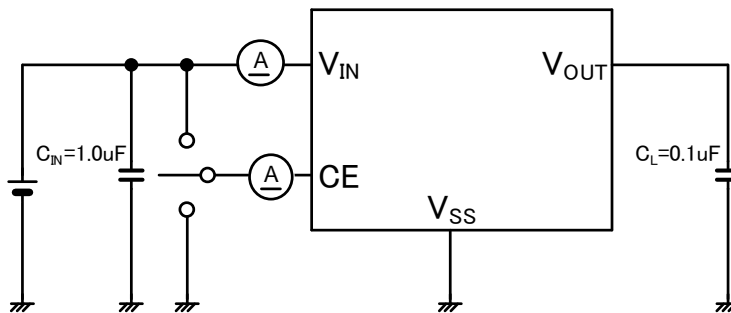
NOMINAL OUTPUT VOLTAGE(V)	E-0				E-1	
	Output Voltage				Dropout Voltage	
	Ta=25°C		-40°C ≤ Ta ≤ 105°C		Ta=25°C	
	V <sub>OUT(E)</sub> (V)		V <sub>OUT(E)</sub> (V)		V <sub>dif</sub> (mV)	
V <sub>OUT(T)</sub>	MIN.	MAX.	MIN.	MAX.	TYP.	MAX.
1.2	1.170	1.230	1.125	1.275	910	1130
1.3	1.270	1.330	1.225	1.375		
1.4	1.370	1.430	1.325	1.475		
1.5	1.470	1.530	1.425	1.575	800	1010
1.6	1.568	1.632	1.520	1.680		
1.7	1.666	1.734	1.615	1.785		
1.8	1.764	1.836	1.710	1.890	710	910
1.9	1.862	1.938	1.805	1.995		
2.0	1.960	2.040	1.900	2.100		
2.1	2.058	2.142	1.995	2.205		
2.2	2.156	2.244	2.090	2.310		
2.3	2.254	2.346	2.185	2.415		
2.4	2.352	2.448	2.280	2.520		
2.5	2.450	2.550	2.375	2.625	510	660
2.6	2.548	2.652	2.470	2.730		
2.7	2.646	2.754	2.565	2.835		
2.8	2.744	2.856	2.660	2.940		
2.9	2.842	2.958	2.755	3.045		
3.0	2.940	3.060	2.850	3.150	360	480
3.1	3.038	3.162	2.945	3.255		
3.2	3.136	3.264	3.040	3.360		
3.3	3.234	3.366	3.135	3.465		
3.4	3.332	3.468	3.230	3.570		
3.5	3.430	3.570	3.325	3.675		
3.6	3.528	3.672	3.420	3.780		
3.7	3.626	3.774	3.515	3.885		
3.8	3.724	3.876	3.610	3.990		
3.9	3.822	3.978	3.705	4.095		
4.0	3.920	4.080	3.800	4.200		
4.1	4.018	4.182	3.895	4.305		
4.2	4.116	4.284	3.990	4.410		
4.3	4.214	4.386	4.085	4.515		
4.4	4.312	4.488	4.180	4.620		
4.5	4.410	4.590	4.275	4.725		
4.6	4.508	4.692	4.370	4.830		
4.7	4.606	4.794	4.465	4.935		
4.8	4.704	4.896	4.560	5.040		
4.9	4.802	4.998	4.655	5.145		
5.0	4.900	5.100	4.750	5.250	260	350

## TEST CIRCUITS

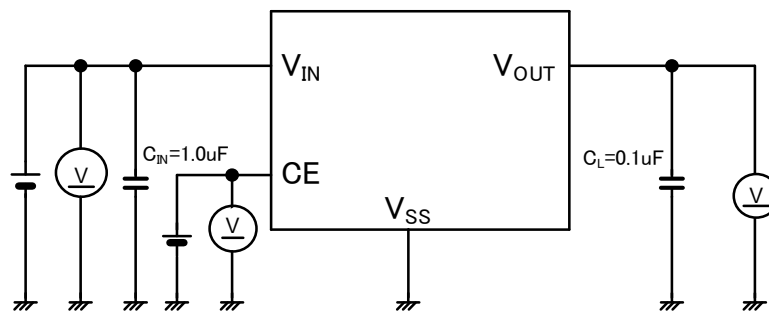
●CIRCUIT①



●CIRCUIT②

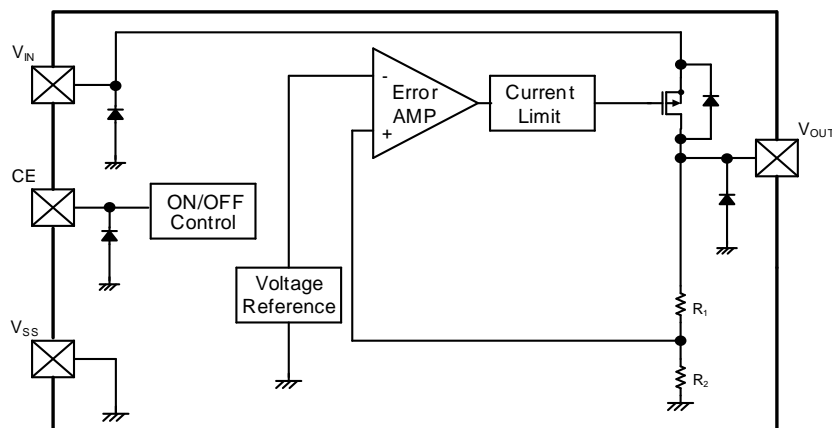


●CIRCUIT③



## ■ OPERATIONAL EXPLANATION

The voltage divided by resistors  $R_1$  &  $R_2$  is compared with the internal voltage reference by the error amplifier. The P-channel MOSFET, which is connected to the  $V_{OUT}$  pin, is then driven by the subsequent output signal. The output voltage at the  $V_{OUT}$  pin is controlled and stabilized by a system of negative feedback. The current limit operates in relation to the level of output current. Further, the IC's internal circuitry can be operated or shutdown via the CE pin's signal.



\* Diodes shown in the above circuit are ESD protection diodes and parasitic diodes

### <Low ESR Capacitors>

The XD6506 series needs an output capacitor ( $C_L$ ) for phase compensation. In order to ensure the stable phase compensation, please place an output capacitor ( $C_L$ ) of  $0.1\mu\text{F}$  or bigger at the  $V_{OUT}$  pin and  $V_{SS}$  pin as close as possible. For a stable power input, please connect an input capacitor ( $C_{IN}$ ) of  $0.1\mu\text{F}$  between the input pin ( $V_{IN}$ ) and the ground pin ( $V_{SS}$ ). Since Input capacitor ( $C_{IN}$ ), the output capacitor ( $C_L$ ) are bias dependence of the capacitor the influence of the missing capacity due to temperature characteristics, also there is a risk that cannot be stable phase compensation. Please pay attention to the selection of the capacitor to be used.

### <Current Limit>

The XD6506 series includes a current fold-back circuit as a current limit protection. When the load current reaches the current limit level, the current fold-back circuit operates and output voltage drops. The output voltage drops further and output current decreases. When the output pin is shorted, a current of about 30mA flows.

### <CE Pin>

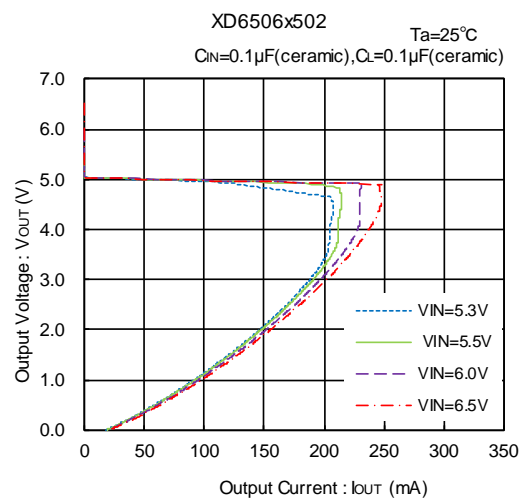
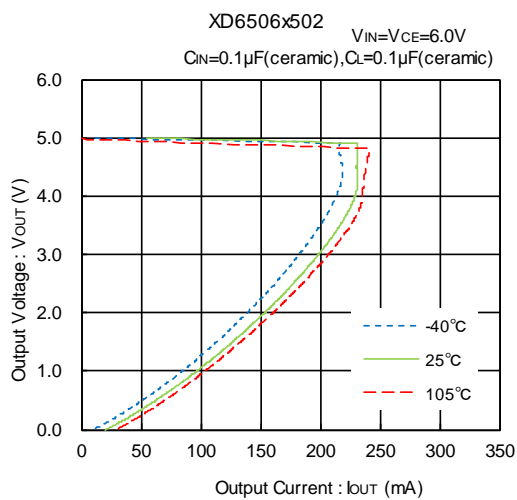
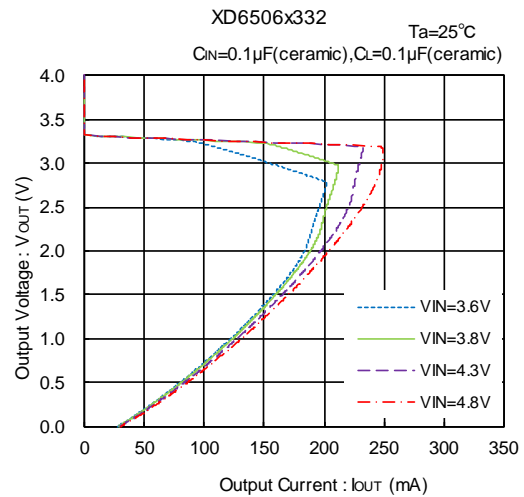
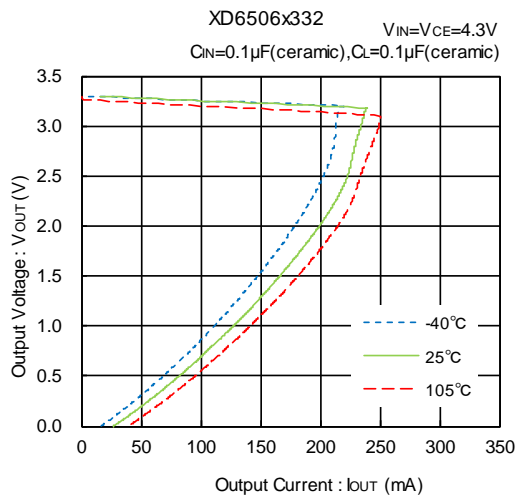
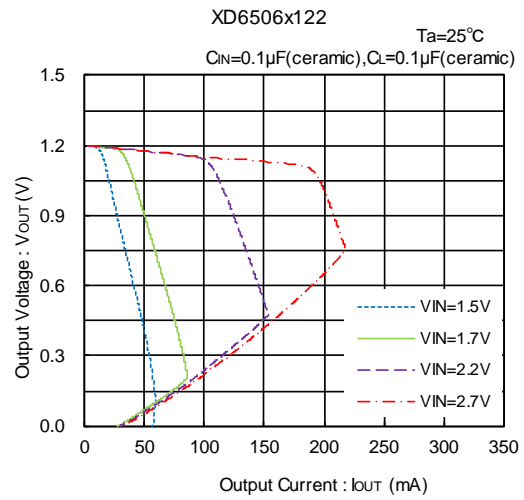
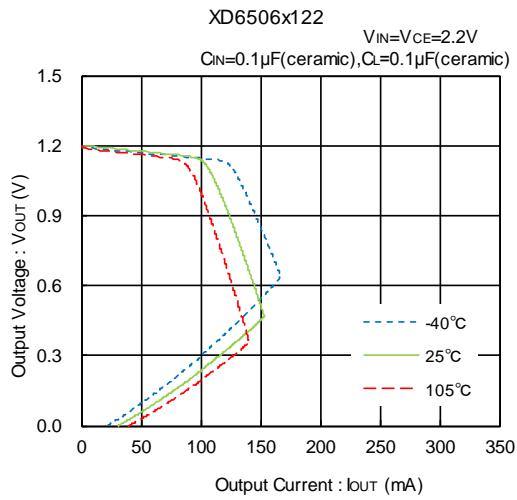
The IC's internal circuitry can be active or stand-by via the signal from the CE pin. In stand-by mode, output at the  $V_{OUT}$  pin will be pulled down to the  $V_{SS}$  level via  $R_1$  &  $R_2$ . We suggest that you use this IC with either a  $V_{IN}$  voltage or a  $V_{SS}$  voltage input at the CE pin. If this IC is used with the correct specifications for the CE pin, the operational logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

## ■ NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please strengthen  $V_{IN}$  and  $V_{SS}$  wiring in particular. The input capacitor ( $C_{IN}$ ) and the output capacitor ( $C_L$ ) should be placed to the IC as close as possible with a shorter wiring.
3. In order to stabilize the  $V_{IN}$ 's voltage level, we recommend that an input capacitor ( $C_{IN}$ ) of about  $0.1$  to  $1.0\mu\text{F}$  be connected between the  $V_{IN}$  pin and the  $V_{SS}$  pin. Moreover, during transient response, so as to prevent an undershoot or overshoot, we recommend that the output capacitor ( $C_L$ ) of about  $0.1$  to  $1.0\mu\text{F}$  be connected between the  $V_{OUT}$  pin and the  $V_{SS}$  pin.
4. Torex places an importance on improving our products and its reliability. However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

## TYPICAL PERFORMANCE CHARACTERISTICS

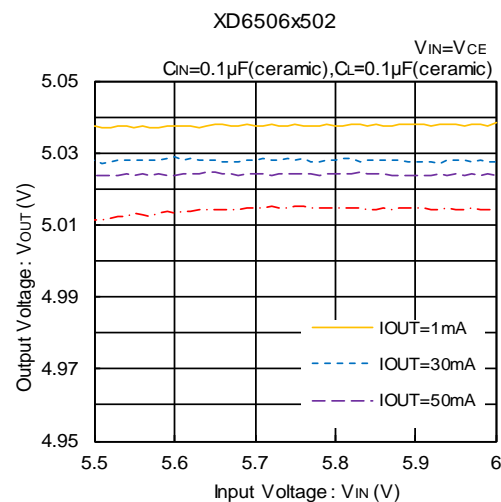
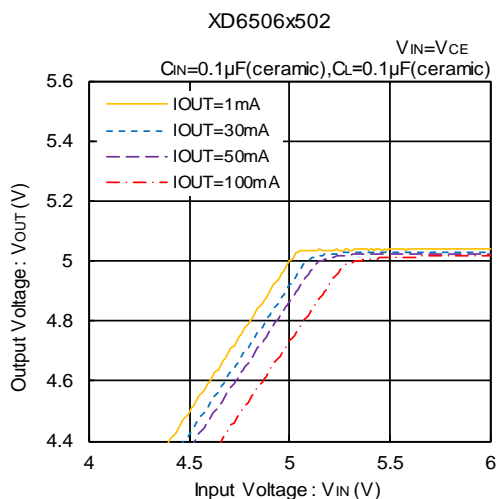
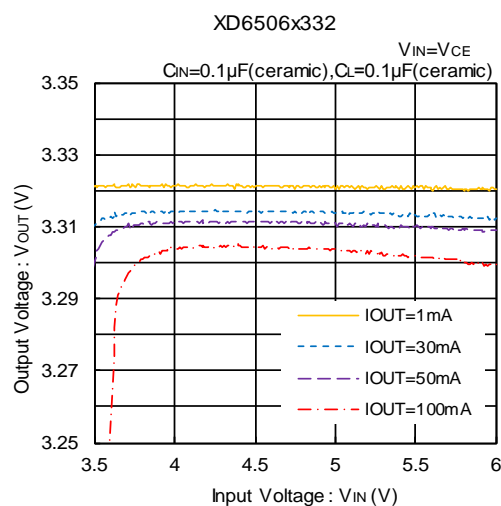
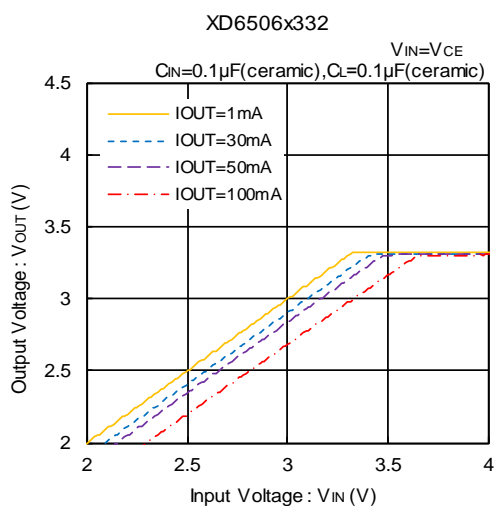
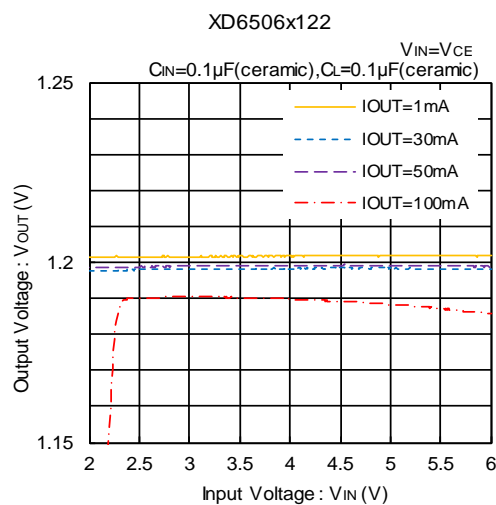
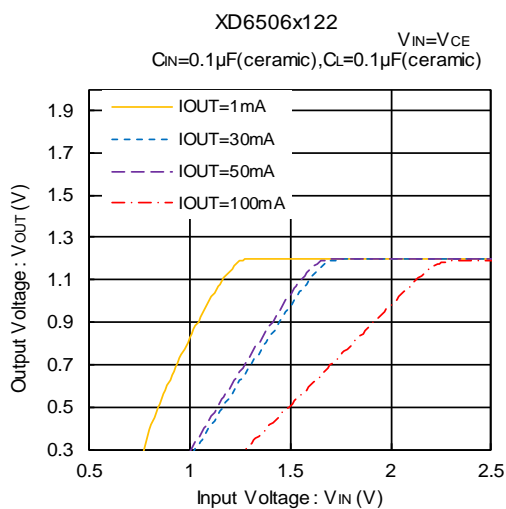
(1) Output Voltage vs. Output Current





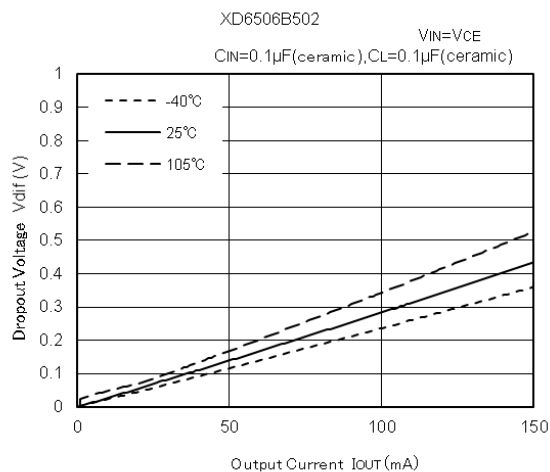
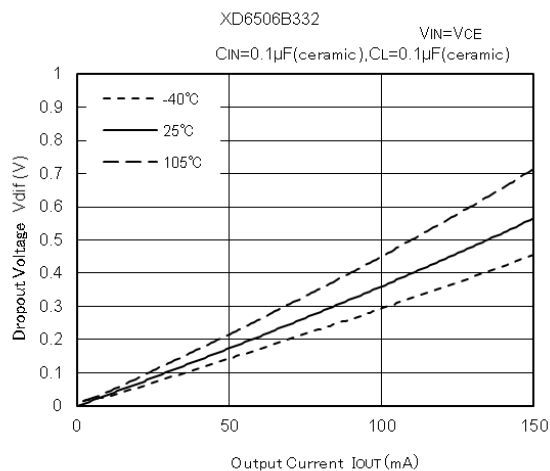
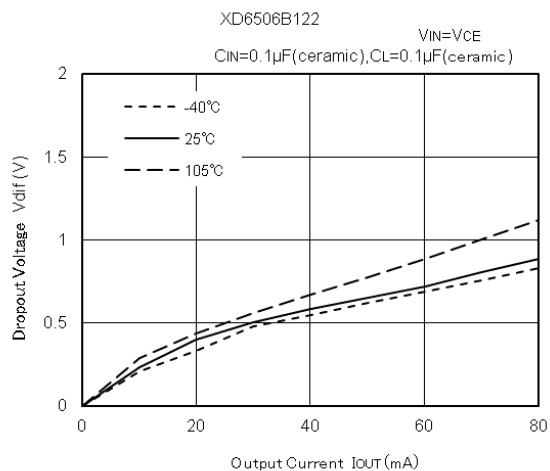
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Input Voltage

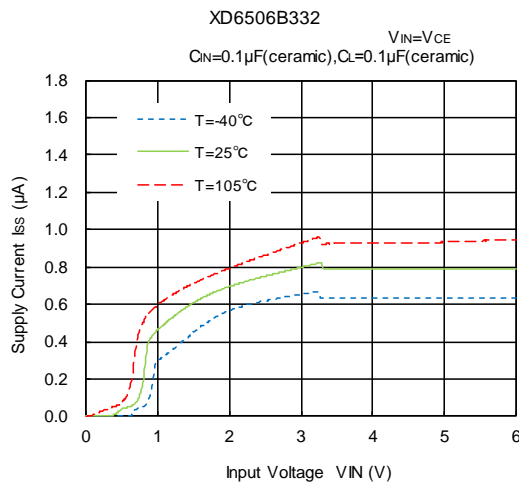
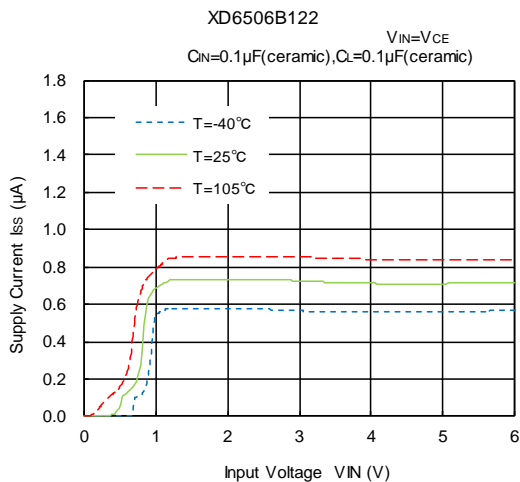


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (3) Dropout Voltage vs. Output Current

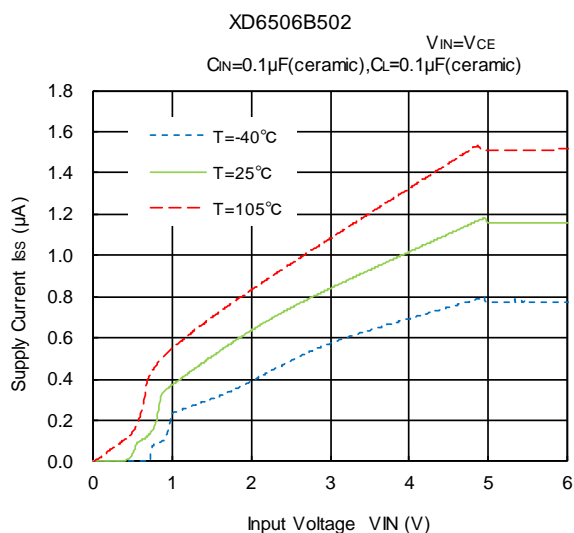


### (4) Supply Current vs. Input Voltage

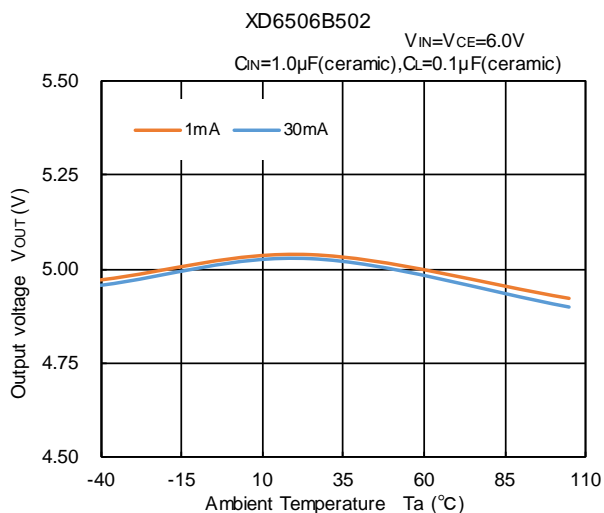
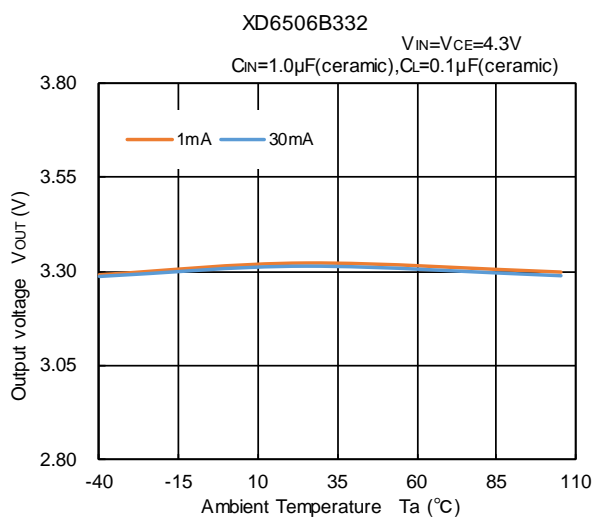
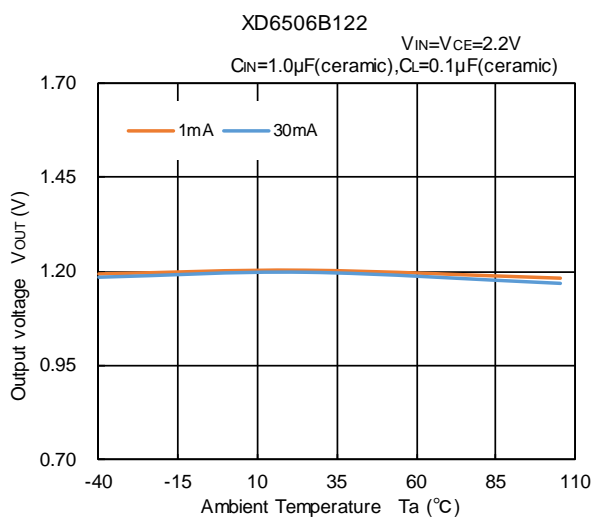


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Supply Current vs. Input Voltage (Continued)

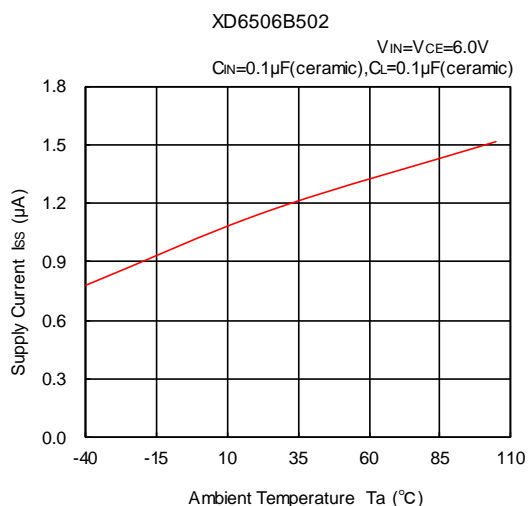
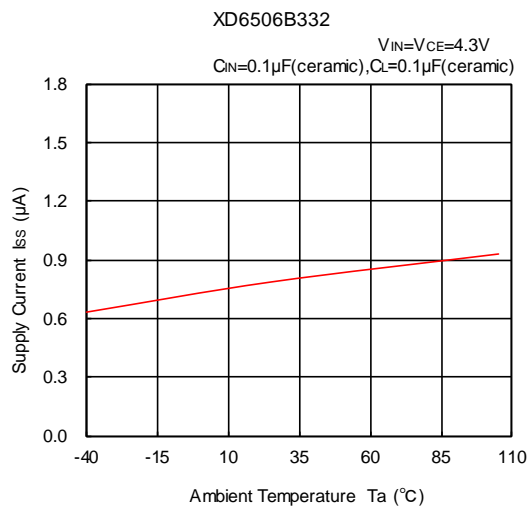
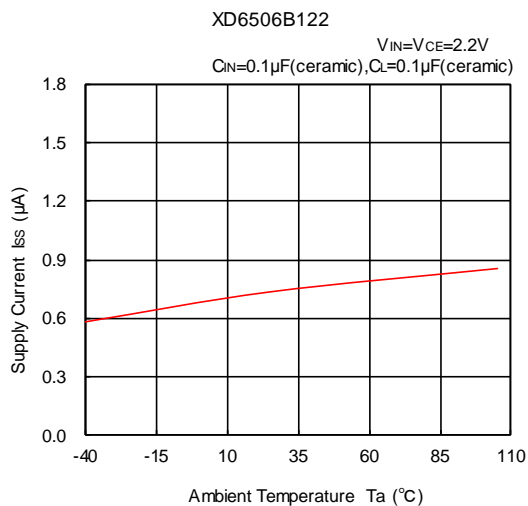


(5) Output Voltage vs. Ambient Temperature

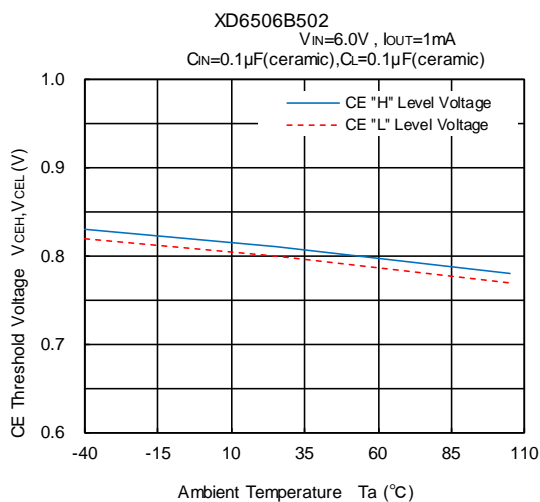
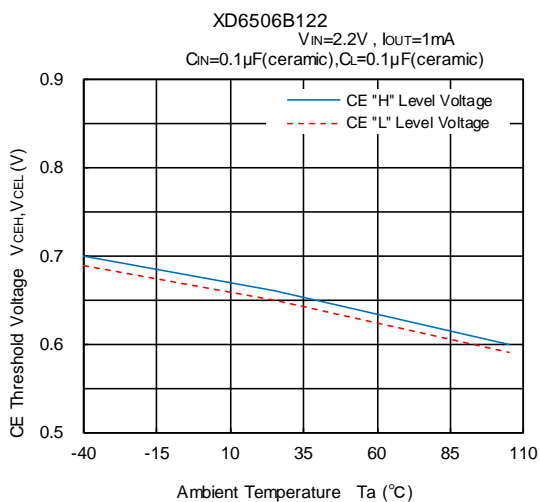


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (6) Supply Current vs. Ambient Temperature

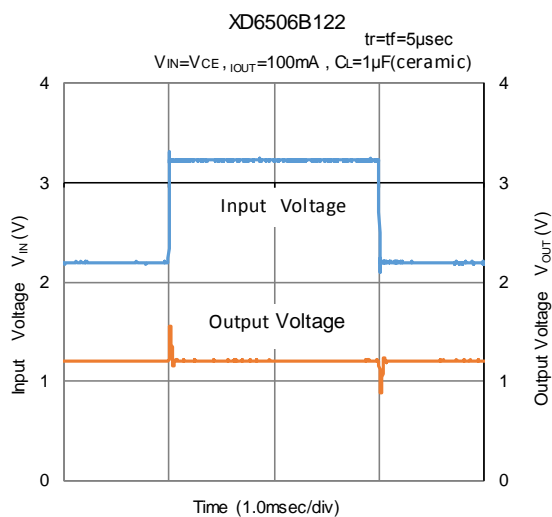
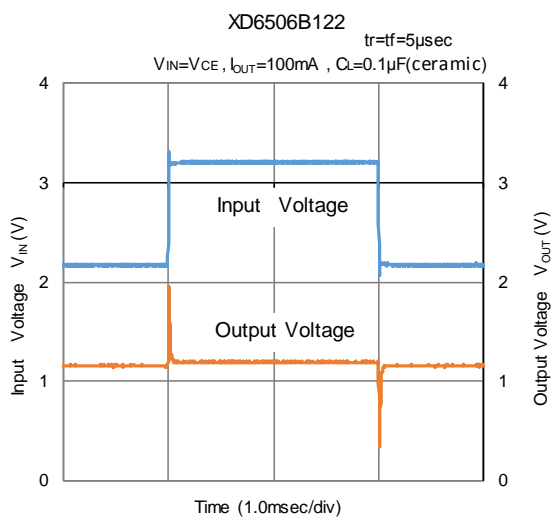
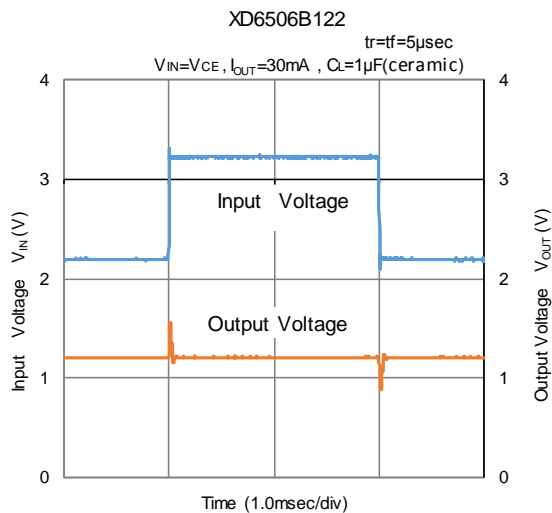
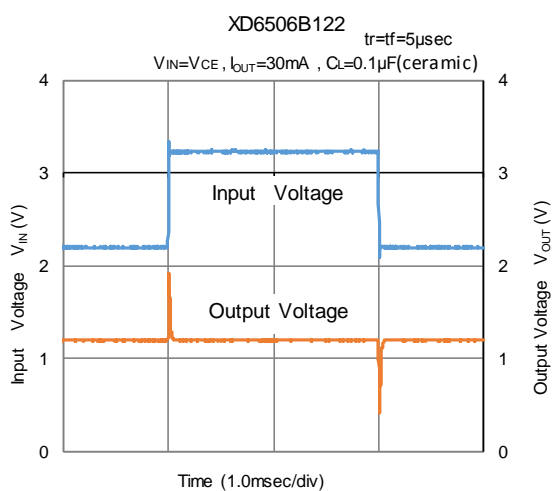
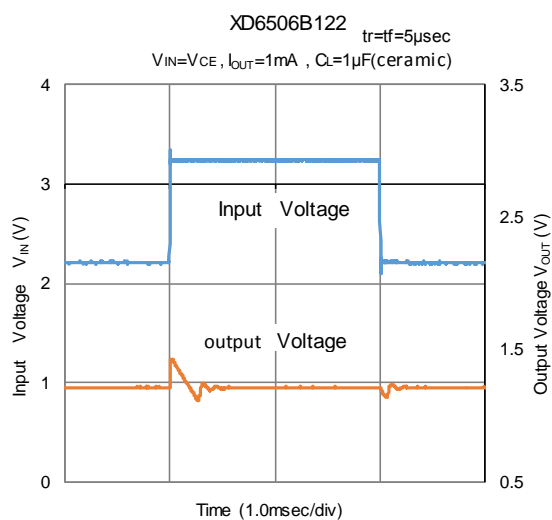
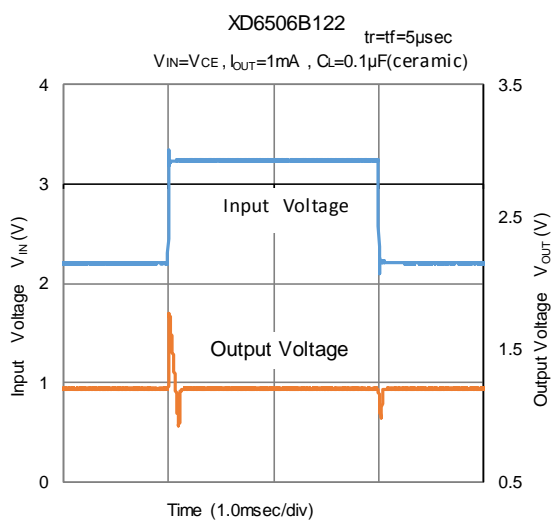


### (7) CE Threshold Voltage vs. Ambient Temperature



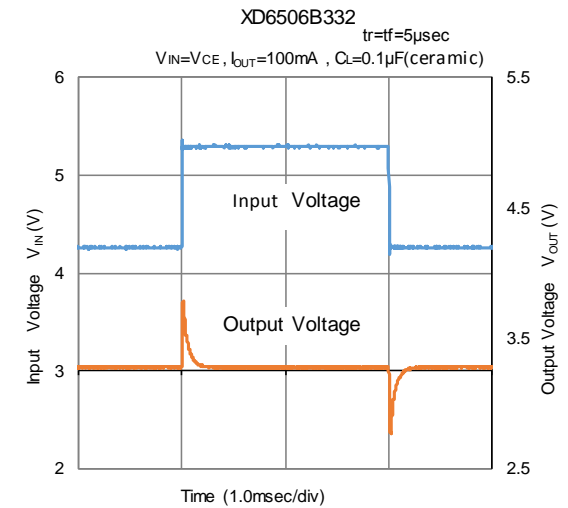
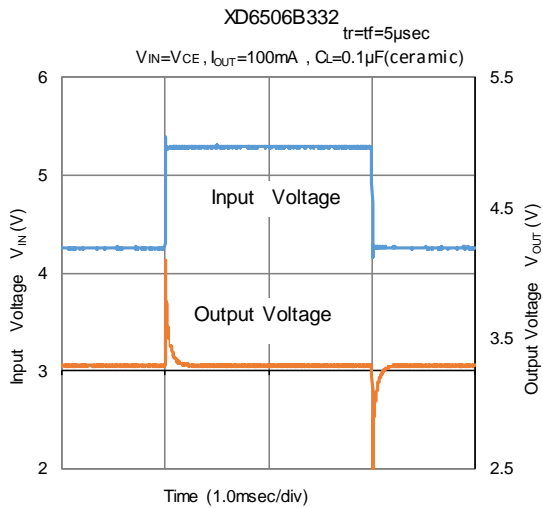
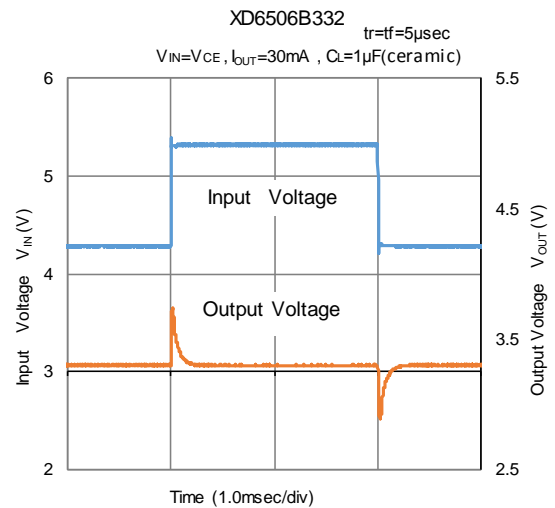
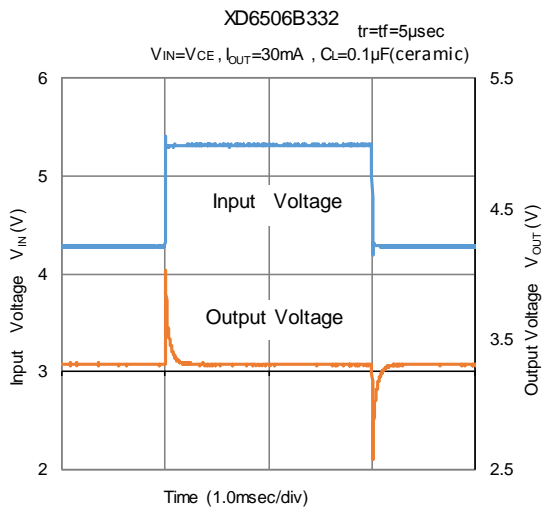
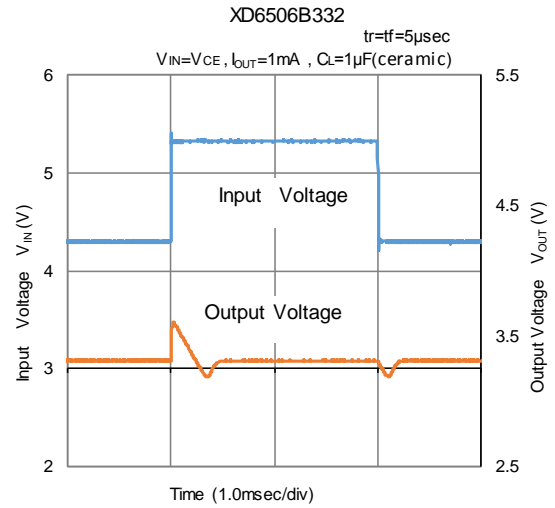
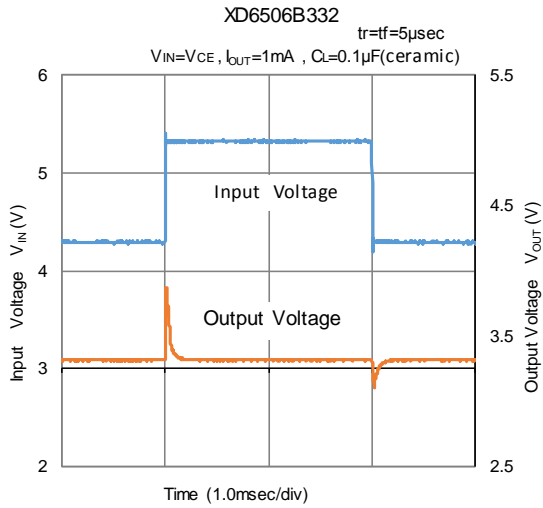
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (8) Input Transient Response



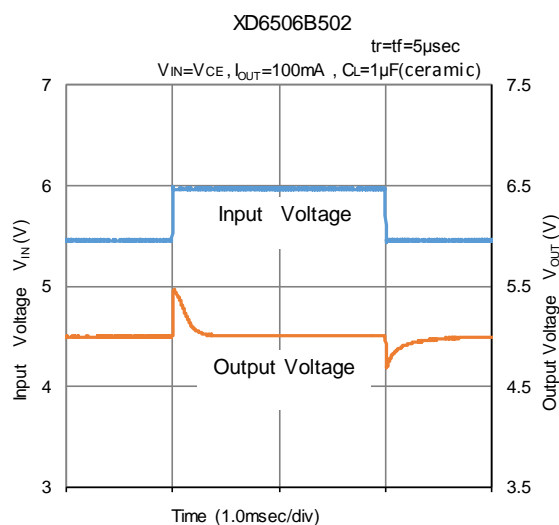
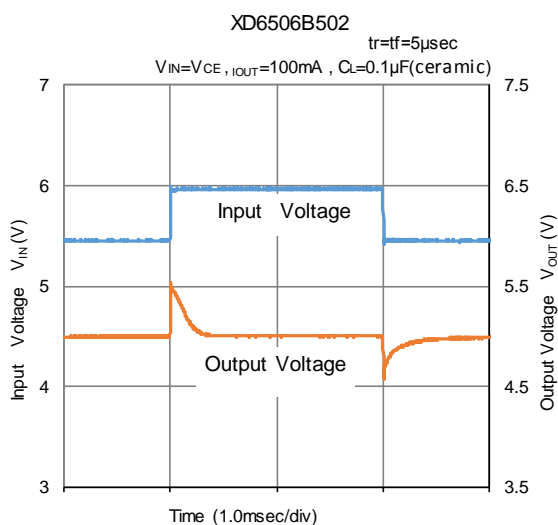
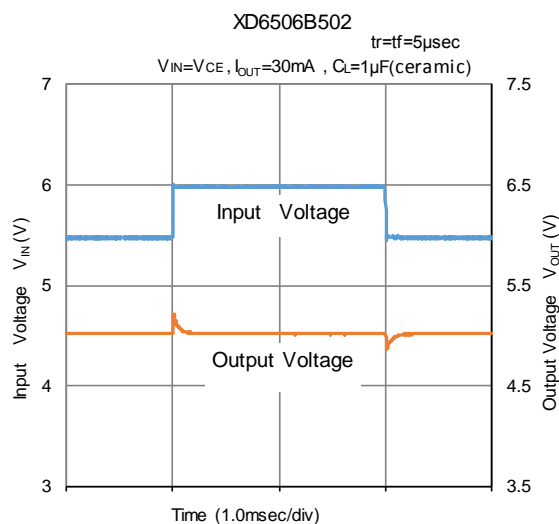
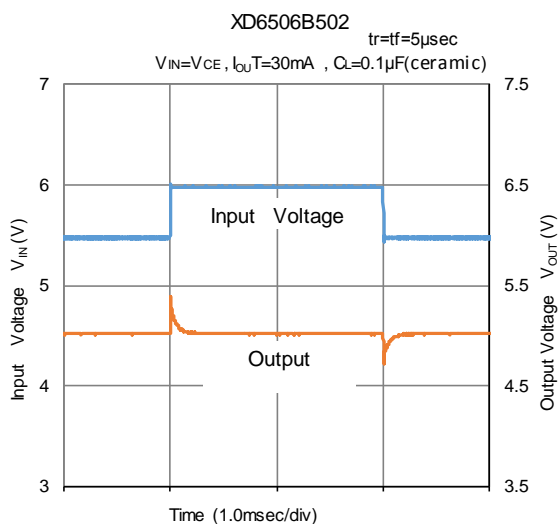
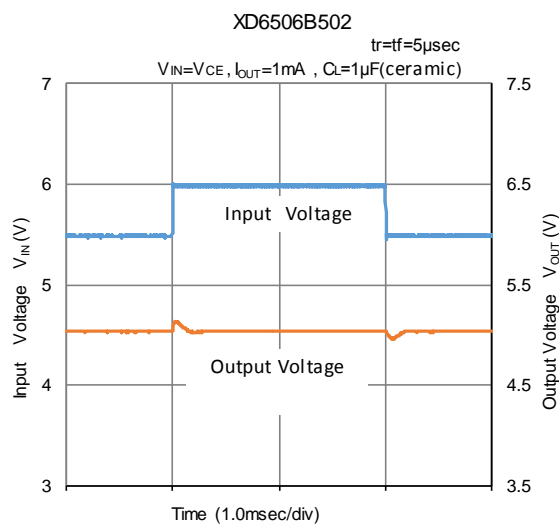
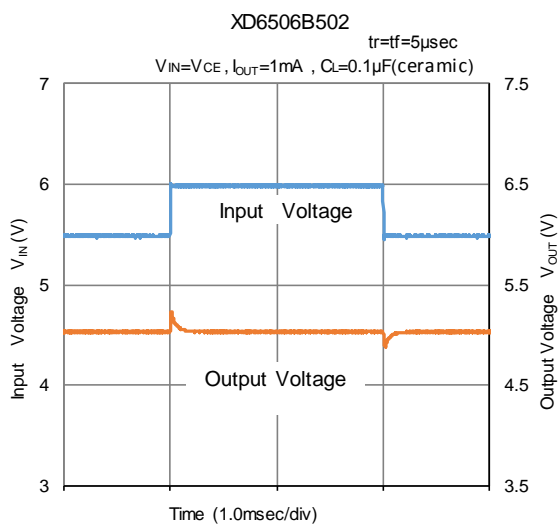
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (8) Input Transient Response (Continued)



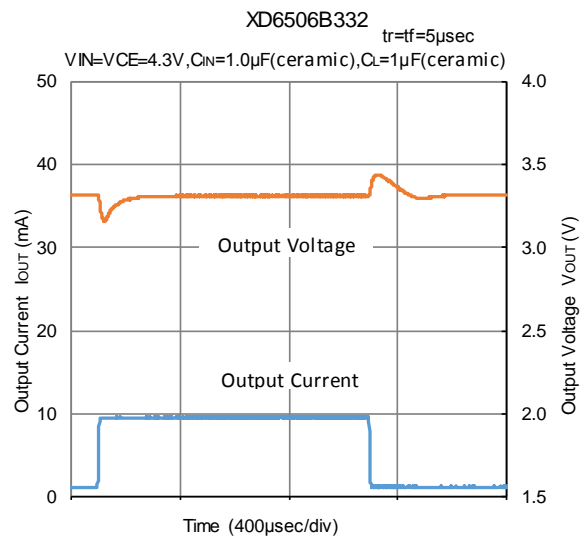
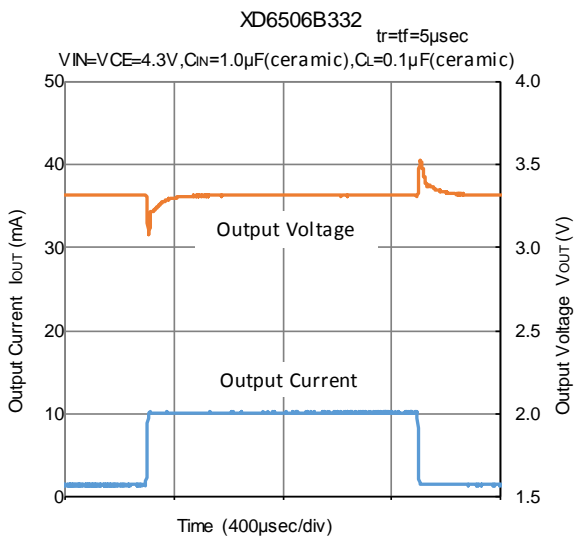
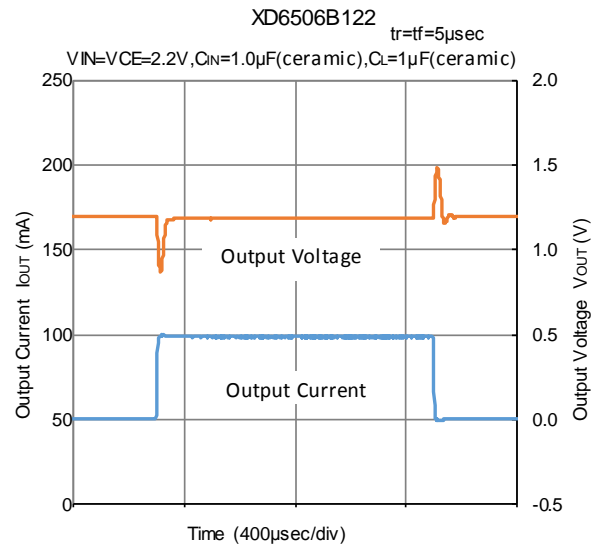
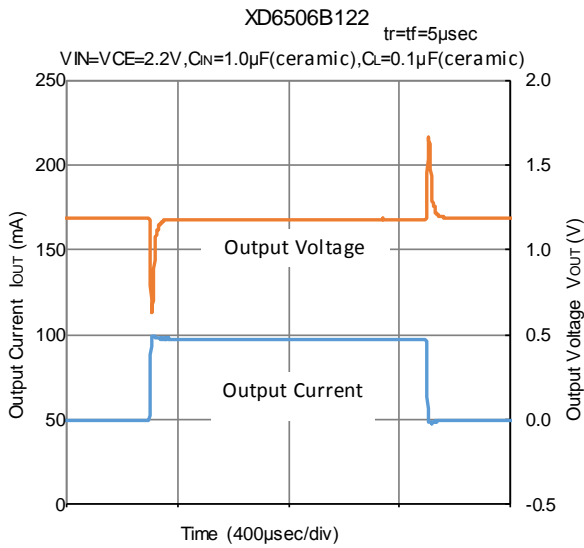
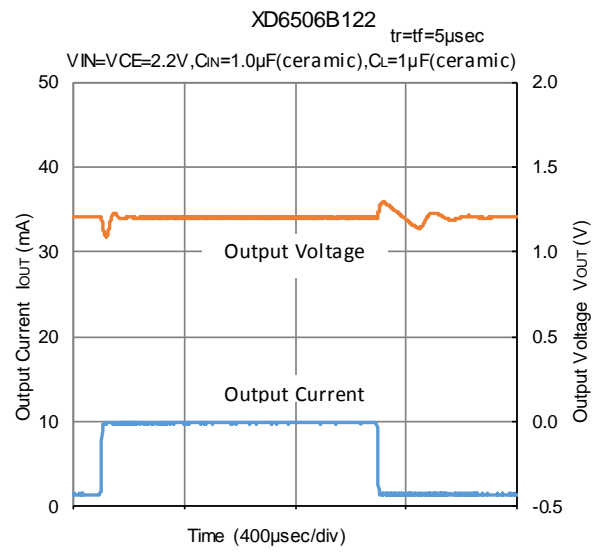
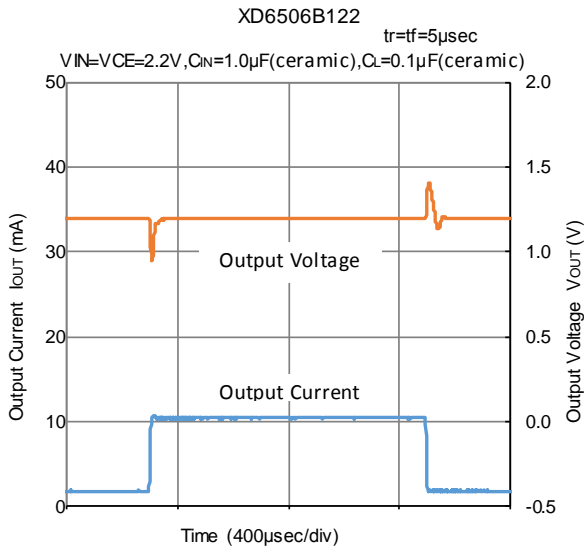
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (8) Input Transient Response (Continued)



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

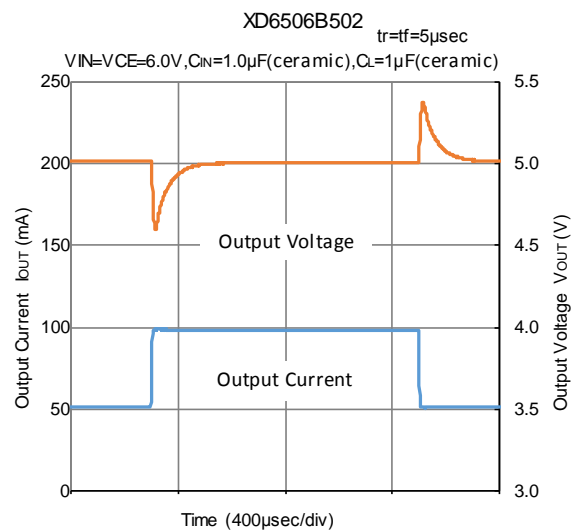
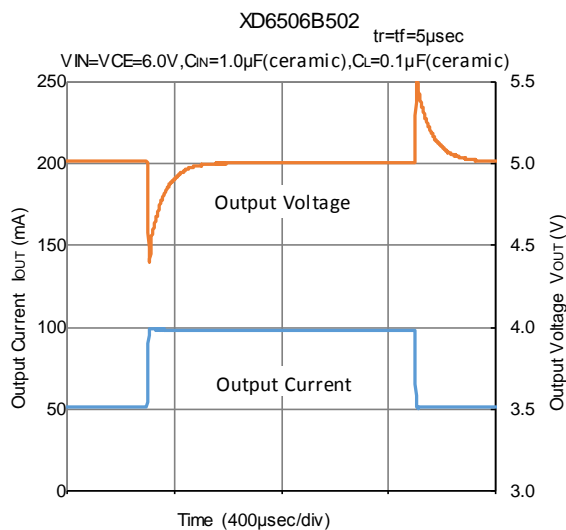
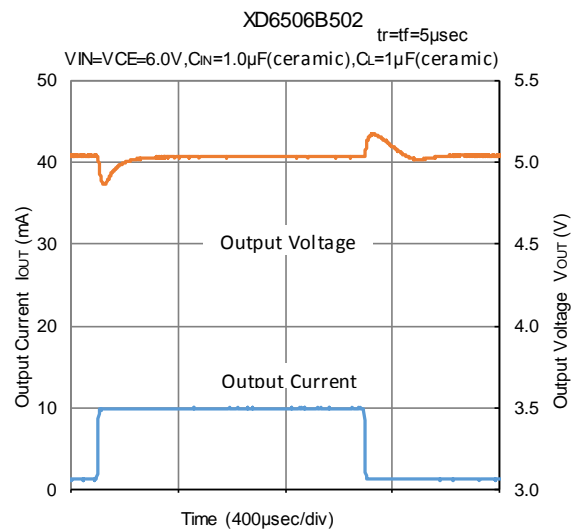
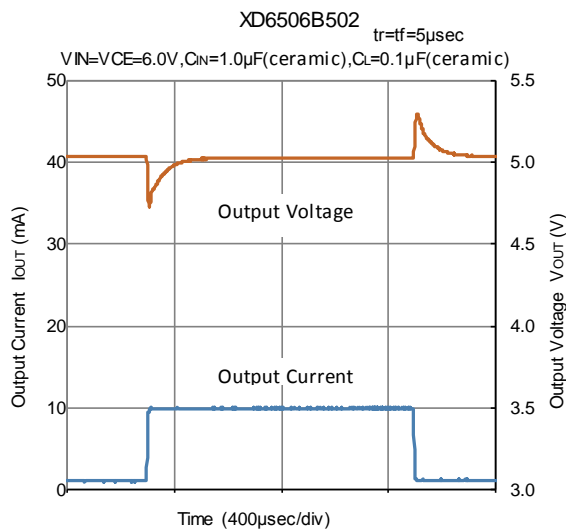
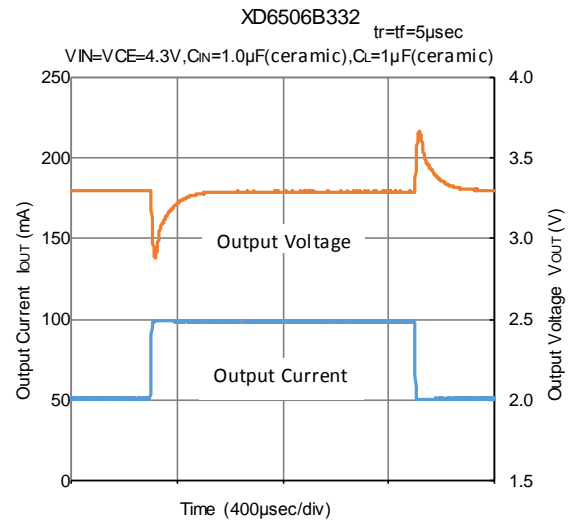
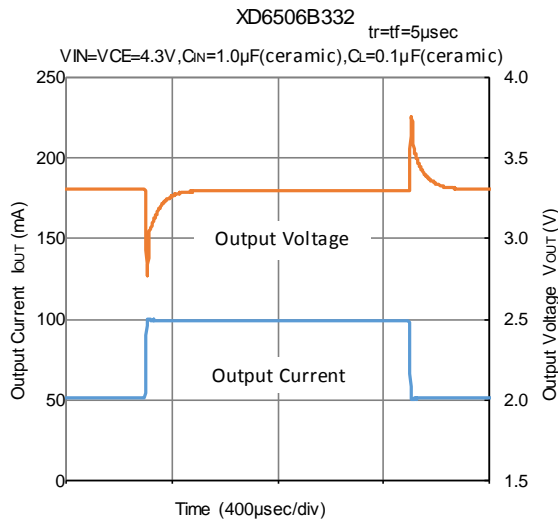
### (9) Load Transient Response





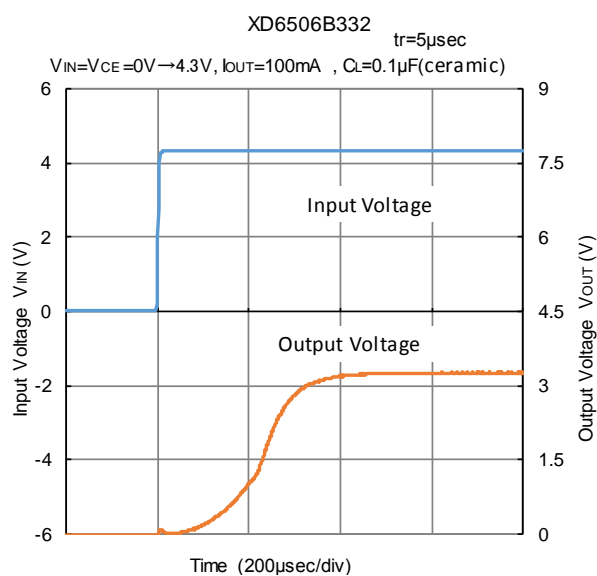
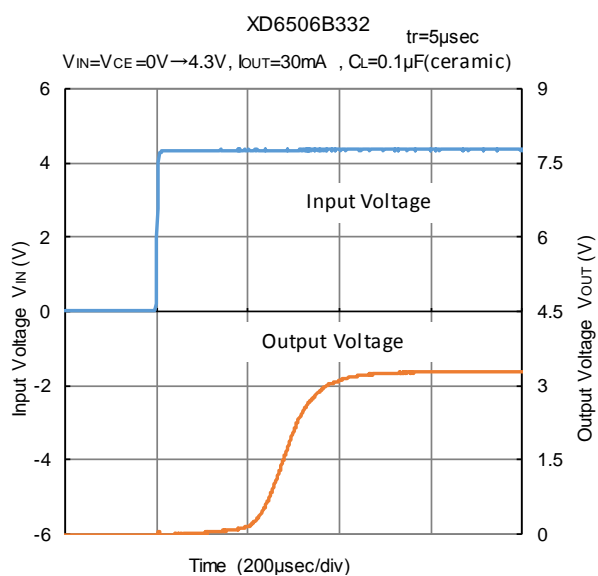
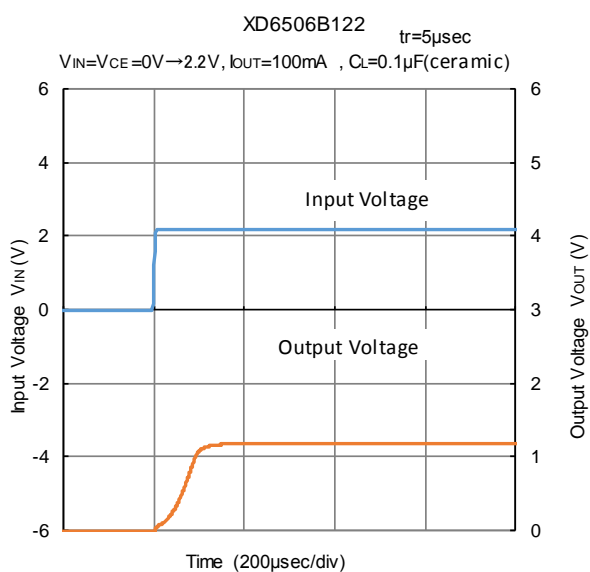
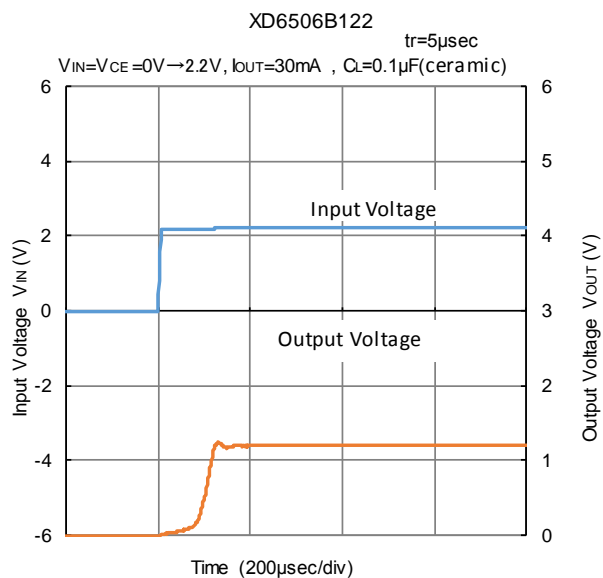
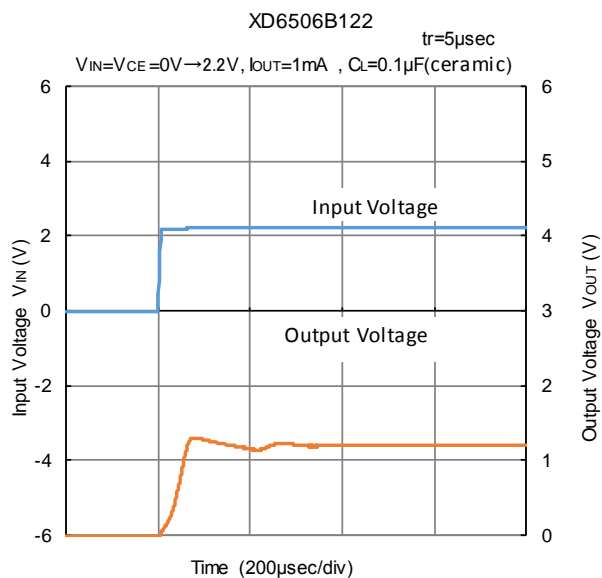
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (9) Load Transient Response (Continued)



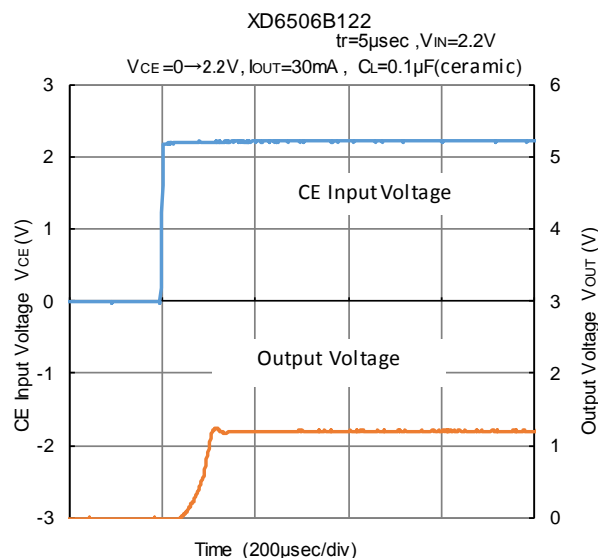
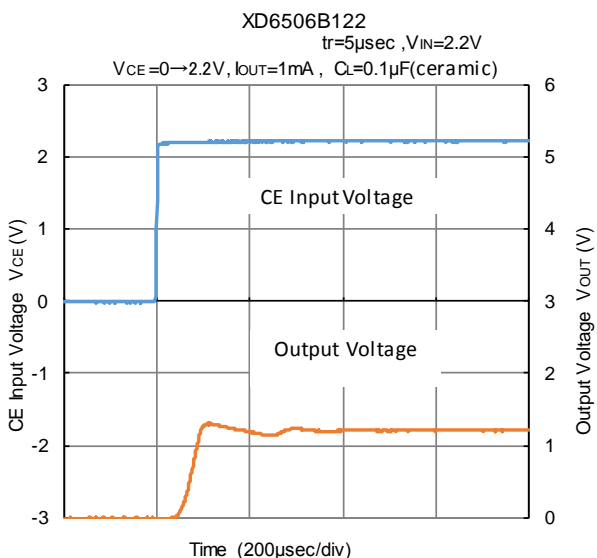
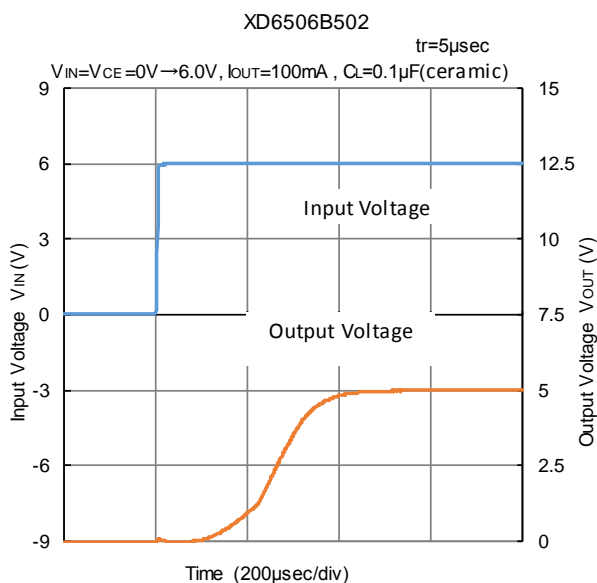
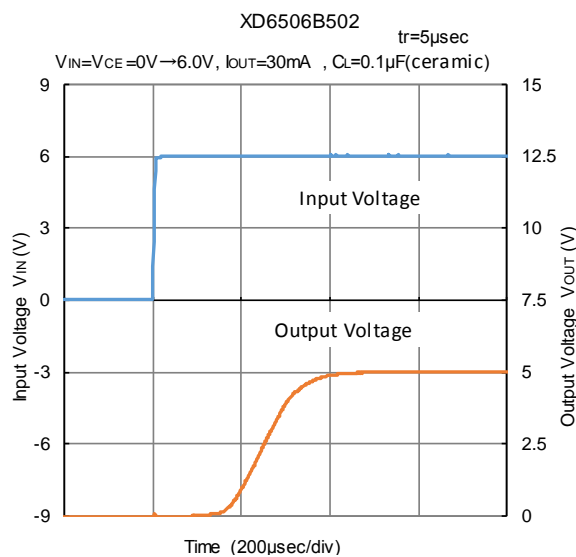
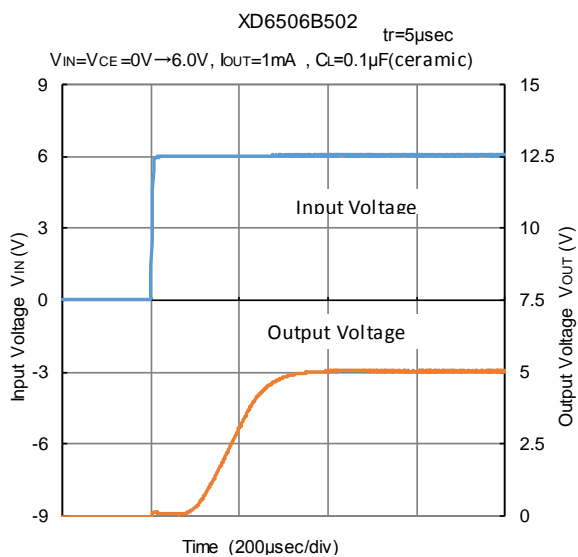
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (10) Rising Response Time



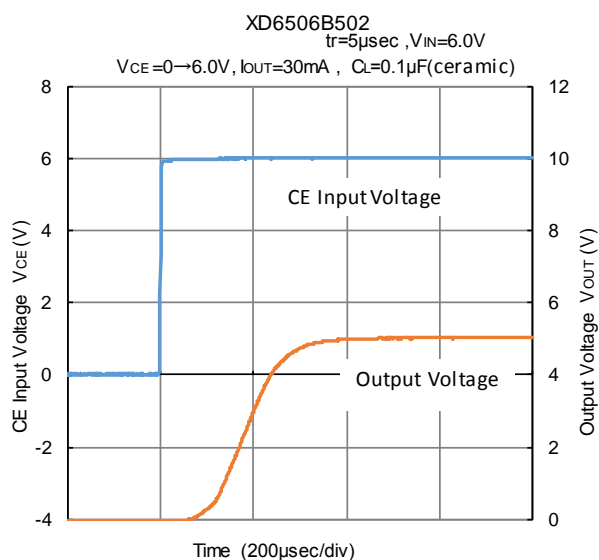
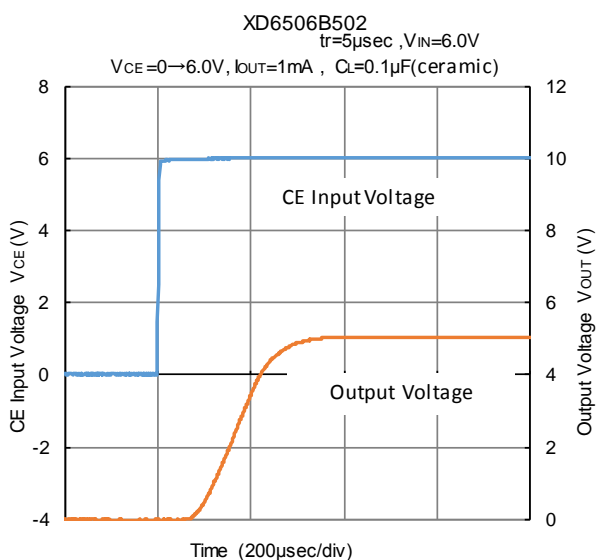
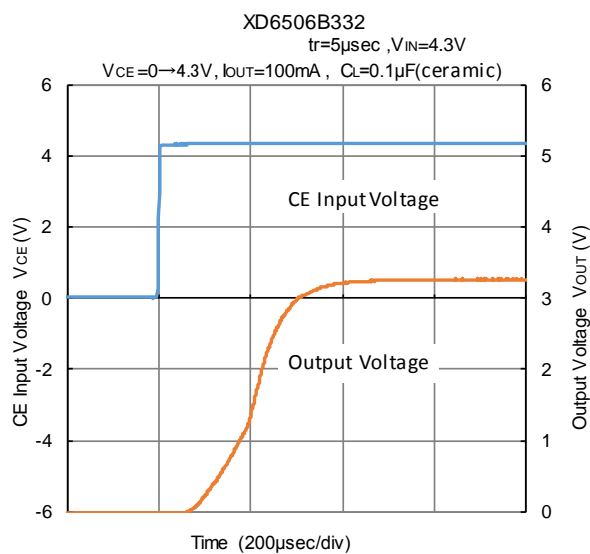
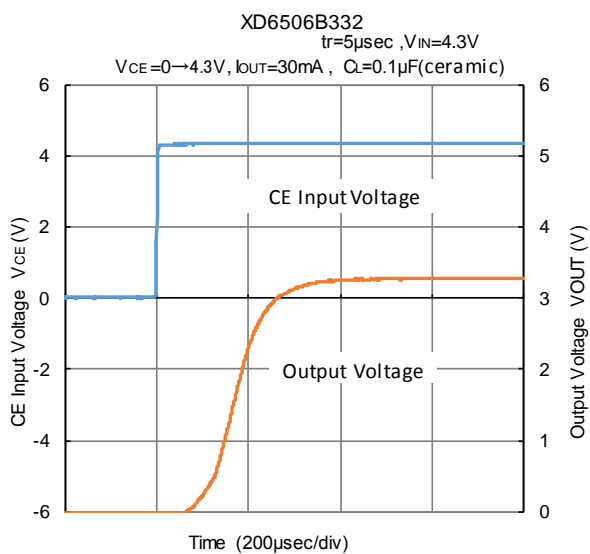
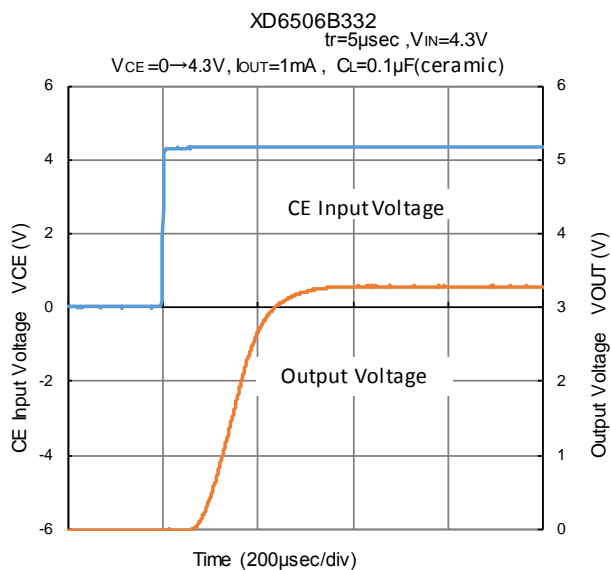
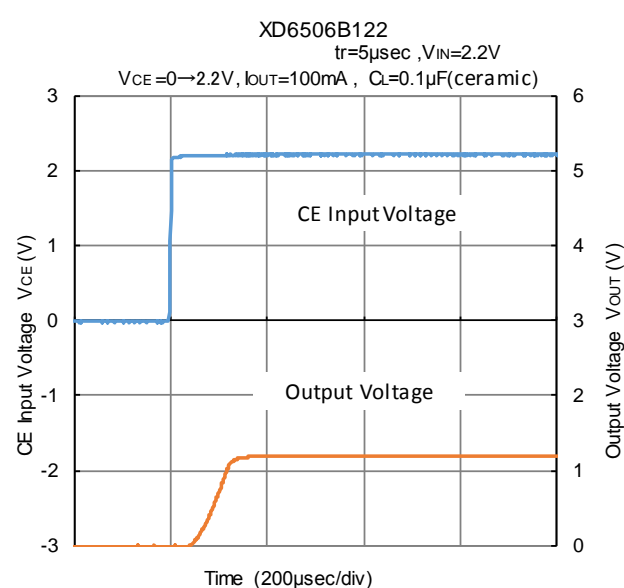
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (10) Rising Response Time (Continued)



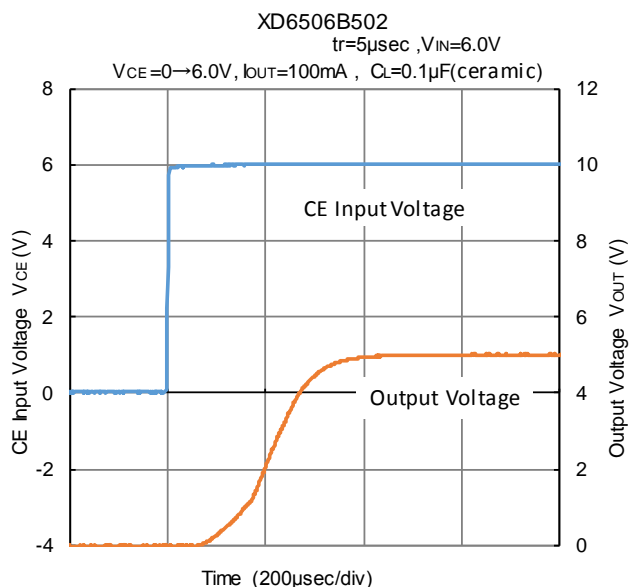
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (11) CE Rising Response Time (Continued)

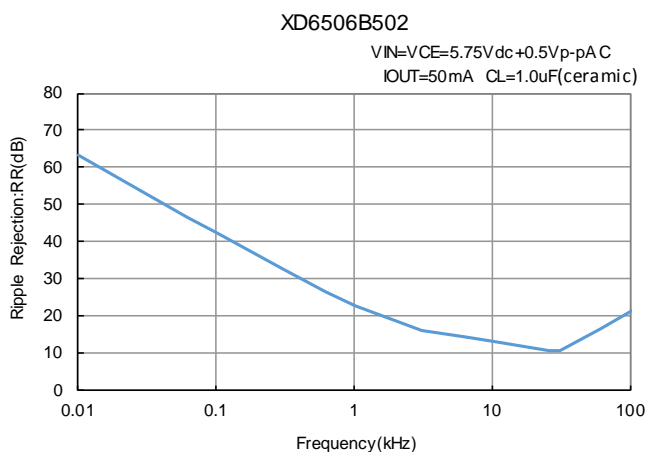
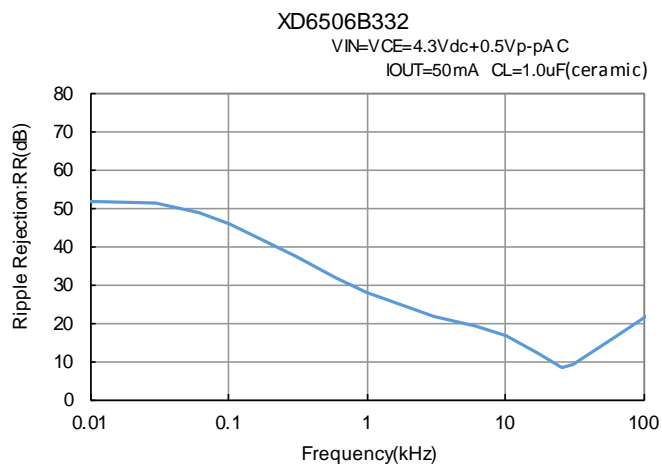
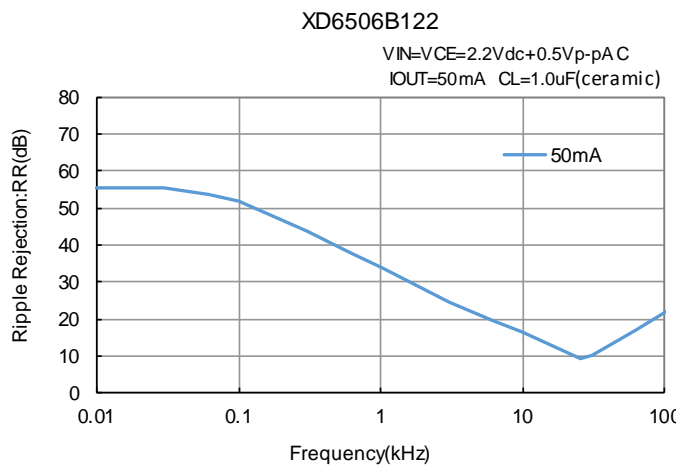


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(11) CE Rising Response Time (Continued)



(12) Ripple Rejection Rate



## ■ PACKAGING INFORMATION

For the latest package information go to, [www.torexsemi.com/technical-support/packages](http://www.torexsemi.com/technical-support/packages)

PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-25	<a href="#">SOT-25 PKG</a>	Standard Board	<a href="#">SOT-25 Power Dissipation</a>
		JESD51-7 Board	

## MARKING RULE

### ●SOT-25

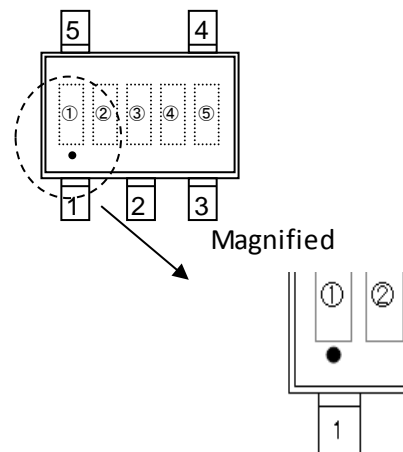
① represents the product series

MARK	PRODUCT SERIES
E	XD6506xxxxxx-Q

② represents the output voltage range

MARK	Type	VOLTAGE (V)	PRODUCT SERIES
0	with CE function	1.2~3.0	XD6506Bxxxxx-Q
1		3.1~5.0	

SOT-25(Under dot)



③ represents the output voltage

MARK	VOLTAGE(V)		MARK	VOLTAGE(V)	
0	-	3.1	F	1.6	4.6
1	-	3.2	H	1.7	4.7
2	-	3.3	K	1.8	4.8
3	-	3.4	L	1.9	4.9
4	-	3.5	M	2.0	5.0
5	-	3.6	N	2.1	-
6	-	3.7	P	2.2	-
7	-	3.8	R	2.3	-
8	-	3.9	S	2.4	-
9	-	4.0	T	2.5	-
A	-	4.1	U	2.6	-
B	1.2	4.2	V	2.7	-
C	1.3	4.3	X	2.8	-
D	1.4	4.4	Y	2.9	-
E	1.5	4.5	Z	3.0	-

④⑤ represents assembly lot number

01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to AZ, B1 to ZZ repeated (G, I, J, O, Q, W excluded)

Note: No character inversion used.

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[MD5130](#)