CMOS Digital Integrated Circuits Silicon Monolithic

74HC164D

1. Functional Description

- 8-Bit Shift Register (S-IN, P-OUT)

2. General

The 74HC164D is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CK input and an overriding $\overline{CLR}$ input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

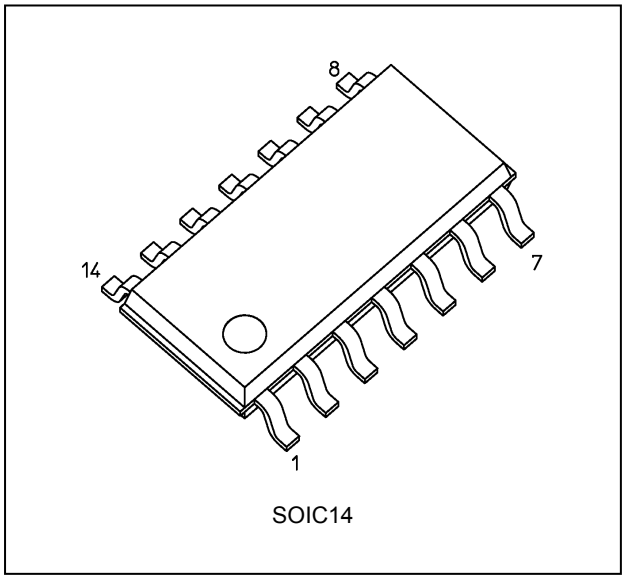
(1) High speed: f_{MAX} = 58 MHz (typ.) at V_{CC} = 5 V

(2) Low power dissipation: I_{CC} = 4.0 μA (max) at T_a = 25 °C

(3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(4) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 to 6.0 V

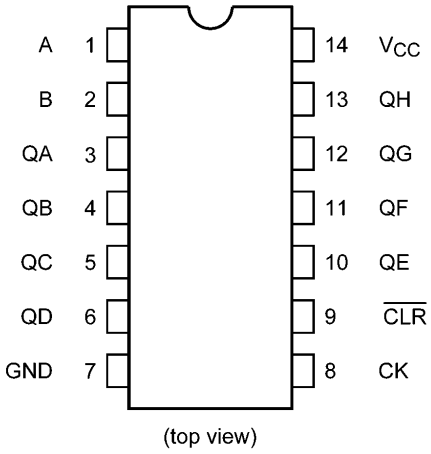
4. Packaging



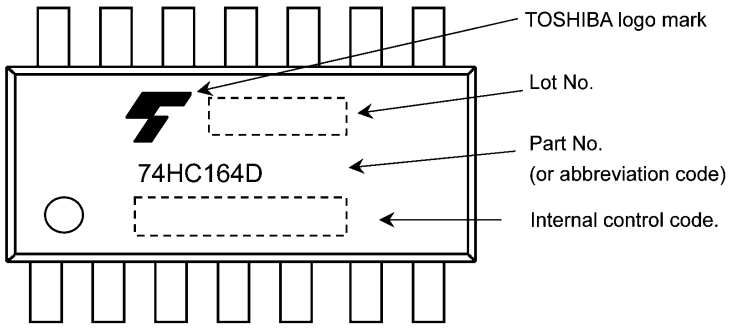
SOIC14

Start of commercial production
2016-02

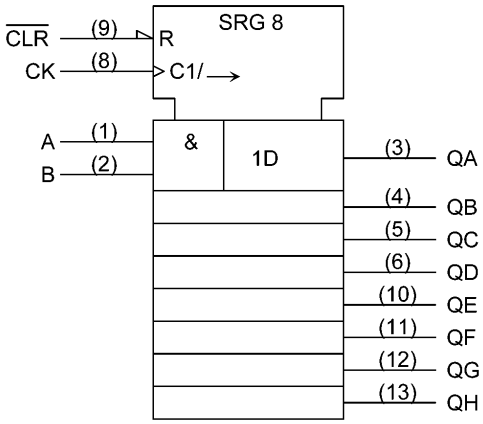
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



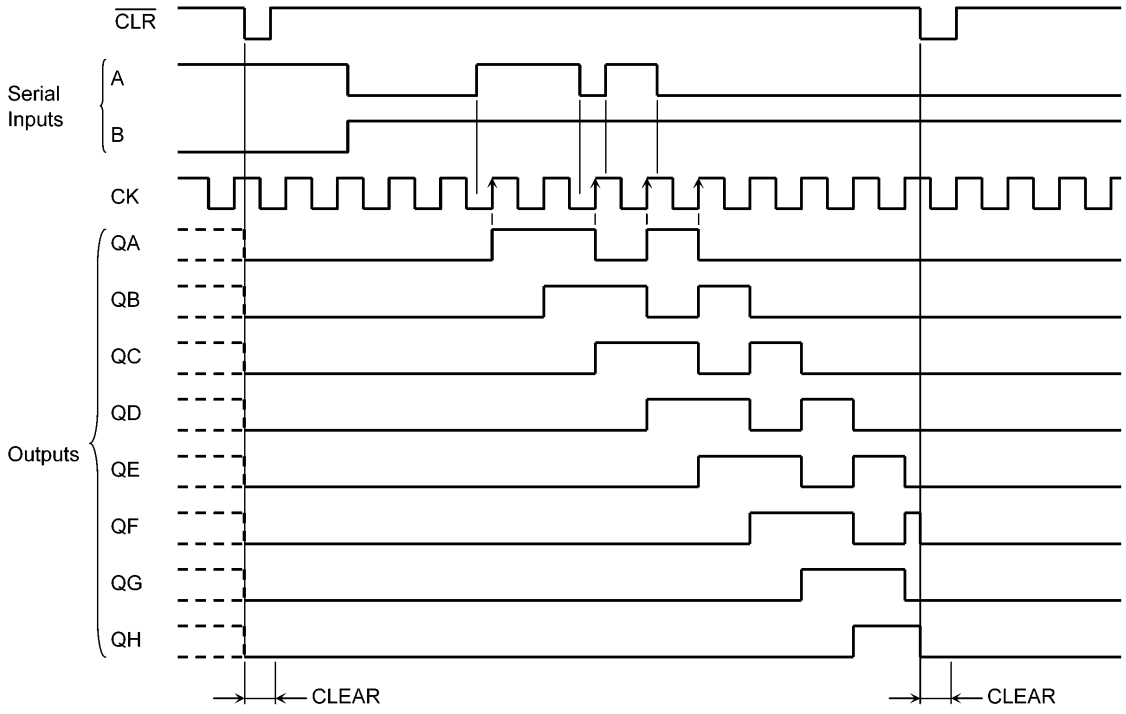
8. Truth Table

Inputs				Outputs			
$\overline{CLR}$	CK	Serial IN		QA	QB	···	QH
		A	B				
L	X	X	X	L	L	···	L
H	↓	X	X	No Change			
H	↑	L	X	L	QAn	···	QGn
H	↑	X	L	L	QAn	···	QGn
H	↑	H	H	H	QAn	···	QGn

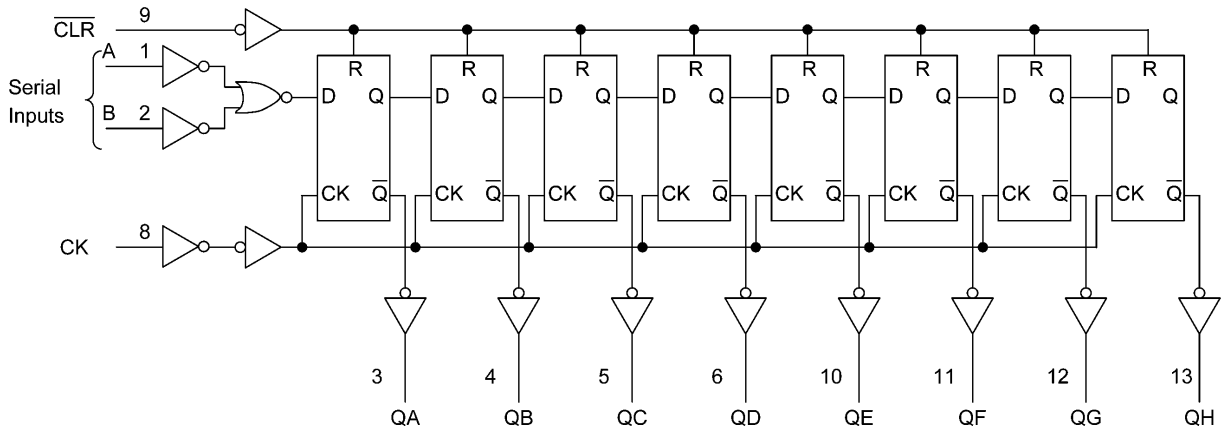
X: Don't care

QAn to QGn: The level of QA to QG, respectively, before the most recent positive edge of the CK.

9. Timing Diagrams



10. System Diagram



11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		±20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±25	mA
V_{CC}/ground current	I_{CC}		±50	mA
Power dissipation	P_D	(Note 1)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: P_D derates linearly with -8 mW/°C above 85 °C

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}	—	2.0 to 6.0	V
Input voltage	V_{IN}	—	0 to V_{CC}	V
Output voltage	V_{OUT}	—	0 to V_{CC}	V
Operating temperature	T_{opr}	—	-40 to 125	°C
Input rise and fall times	t_r,t_f	—	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			I_{OH} = -4 mA	4.5	4.18	4.31	—	
			I_{OH} = -5.2 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	μA

13.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -4 mA	4.5	4.13	—	
			I_{OH} = -5.2 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	40.0	μA

13.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.5	5.9	—	
			I_{OH} = -4 mA	4.5	3.7	—	
			I_{OH} = -5.2 mA	6.0	5.2	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.4	
			I_{OL} = 5.2 mA	6.0	—	0.4	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	160	μA

13.4. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	—	2.0	80	ns
			4.5	16	
			6.0	14	
Minimum setup time (A, B)	t_S	—	2.0	50	ns
			4.5	10	
			6.0	9	
Minimum hold time (A, B)	t_h	—	2.0	5	ns
			4.5	5	
			6.0	5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	2.0	5	ns
			4.5	5	
			6.0	5	
Clock frequency	f	—	2.0	6	MHz
			4.5	31	
			6.0	36	

13.5. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	—	2.0	100	ns
			4.5	20	
			6.0	17	
Minimum setup time (A, B)	t_S	—	2.0	65	ns
			4.5	13	
			6.0	11	
Minimum hold time (A, B)	t_h	—	2.0	5	ns
			4.5	5	
			6.0	5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	2.0	5	ns
			4.5	5	
			6.0	5	
Clock frequency	f	—	2.0	5	MHz
			4.5	25	
			6.0	29	

13.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	—	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum setup time (A, B)	t_S	—	2.0	90	ns
			4.5	18	
			6.0	15	
Minimum hold time (A, B)	t_h	—	2.0	5	ns
			4.5	5	
			6.0	5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	2.0	5	ns
			4.5	5	
			6.0	5	
Clock frequency	f	—	2.0	4	MHz
			4.5	20	
			6.0	24	

13.7. AC Characteristics
(Unless otherwise specified, C_L = 15 pF, V_{CC} = 5 V, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}	—	—	4	8	ns
Propagation delay time (CK-Qn)	t_{PLH},t_{PHL}	—	—	15	27	
Propagation delay time ($\overline{CLR}$-Qn)	t_{PHL}	—	—	16	30	
Maximum clock frequency	f_{MAX}	—	33	58	—	MHz

13.8. AC Characteristics
(Unless otherwise specified, C_L = 50 pF, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	V_{CC} (V)	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		2.0	—	25	75	ns
			4.5	—	7	15	
			6.0	—	6	13	
Propagation delay time (CK-Qn)	t_{PLH},t_{PHL}		2.0	—	57	160	ns
			4.5	—	19	32	
			6.0	—	16	27	
Propagation delay time ($\overline{CLR}$-Qn)	t_{PHL}		2.0	—	60	175	ns
			4.5	—	20	35	
			6.0	—	17	30	
Maximum clock frequency	f_{MAX}		2.0	6	18	—	MHz
			4.5	31	53	—	
			6.0	36	62	—	
Input capacitance	C_{IN}		—	—	3	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—	—	30	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

13.9. AC Characteristics
(Unless otherwise specified, C_L = 50 pF, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

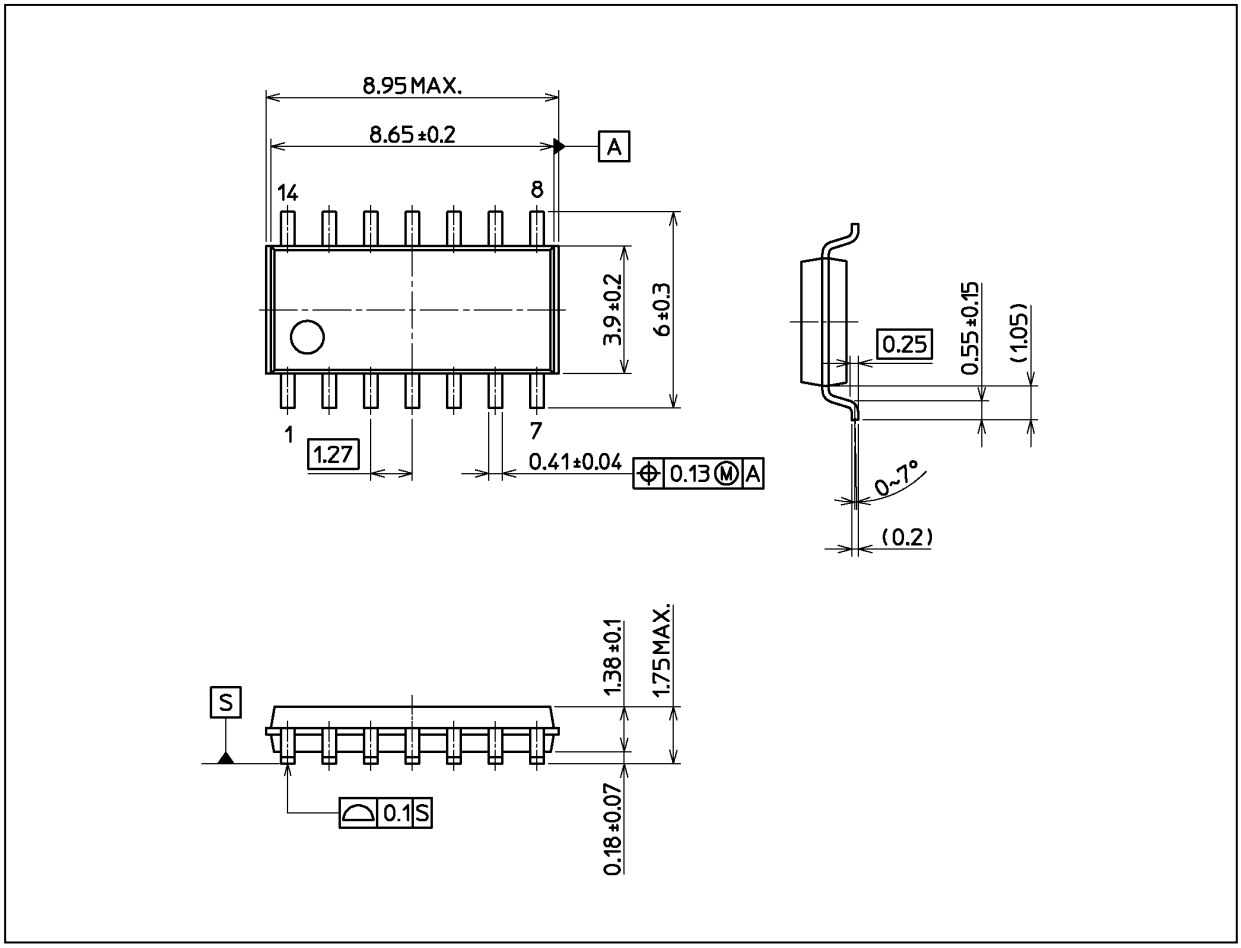
Characteristics	Symbol	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	2.0	—	95	ns
		4.5	—	19	
		6.0	—	16	
Propagation delay time (CK-Qn)	t_{PLH},t_{PHL}	2.0	—	200	ns
		4.5	—	40	
		6.0	—	34	
Propagation delay time ($\overline{CLR}$-Qn)	t_{PHL}	2.0	—	220	ns
		4.5	—	44	
		6.0	—	37	
Maximum clock frequency	f_{MAX}	2.0	5	—	MHz
		4.5	25	—	
		6.0	29	—	

13.10. AC Characteristics
(Unless otherwise specified, C_L = 50 pF, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	2.0	—	110	ns
		4.5	—	22	
		6.0	—	19	
Propagation delay time (CK-Qn)	t_{PLH},t_{PHL}	2.0	—	240	ns
		4.5	—	48	
		6.0	—	41	
Propagation delay time ($\overline{CLR}$-Qn)	t_{PHL}	2.0	—	265	ns
		4.5	—	53	
		6.0	—	45	
Maximum clock frequency	f_{MAX}	2.0	4	—	MHz
		4.5	20	—	
		6.0	24	—	

Package Dimensions

Unit: mm



Weight: 0.13 g (typ.)

Package Name(s)
Nickname: SOIC14

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