TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

74HC595D

8-Bit Shift Register/Latch (3-state)

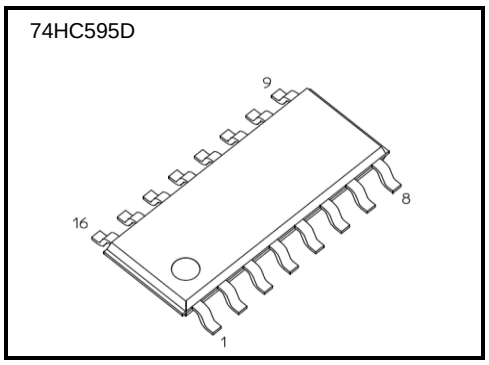
The 74HC595D is a high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C^2MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC595D contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation.

And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.



Weight

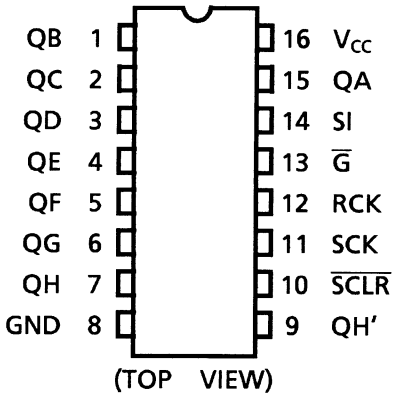
P-SOP16-0410-1.27-005 : 0.15 g (typ.)

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} = 55 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads for QA to QH
  10 LSTTL loads for QH'
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
  For QA to QH
  $|I_{OH}| = I_{OL}$ = 4 mA (min)
  For QH'
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V

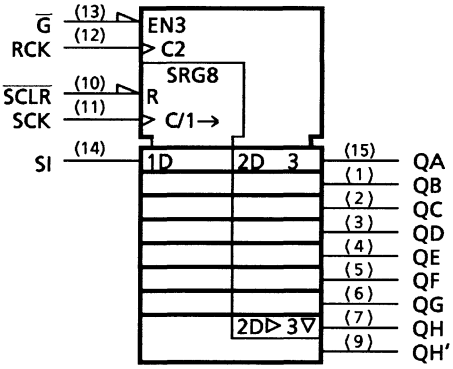
Pin Assignment



Marking

TBD

IEC Logic Symbol

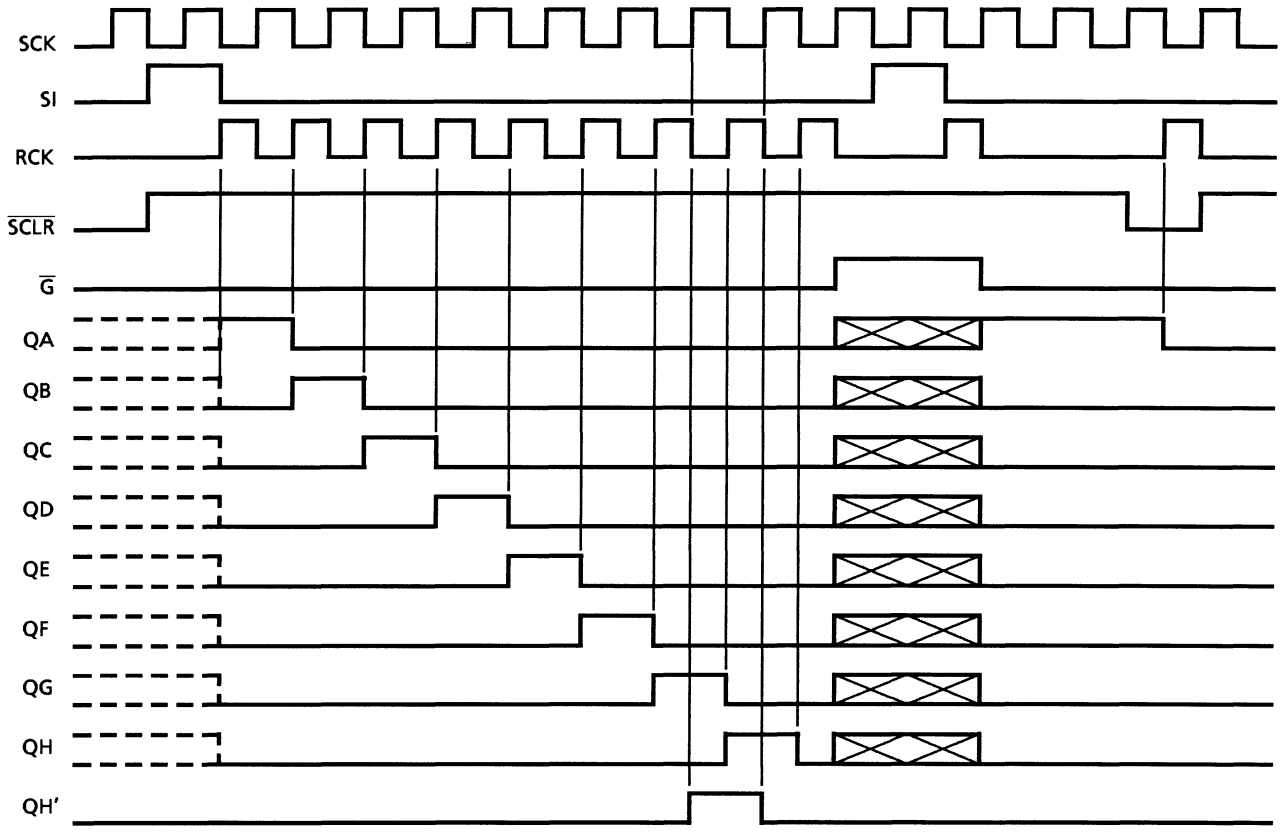


Truth Table

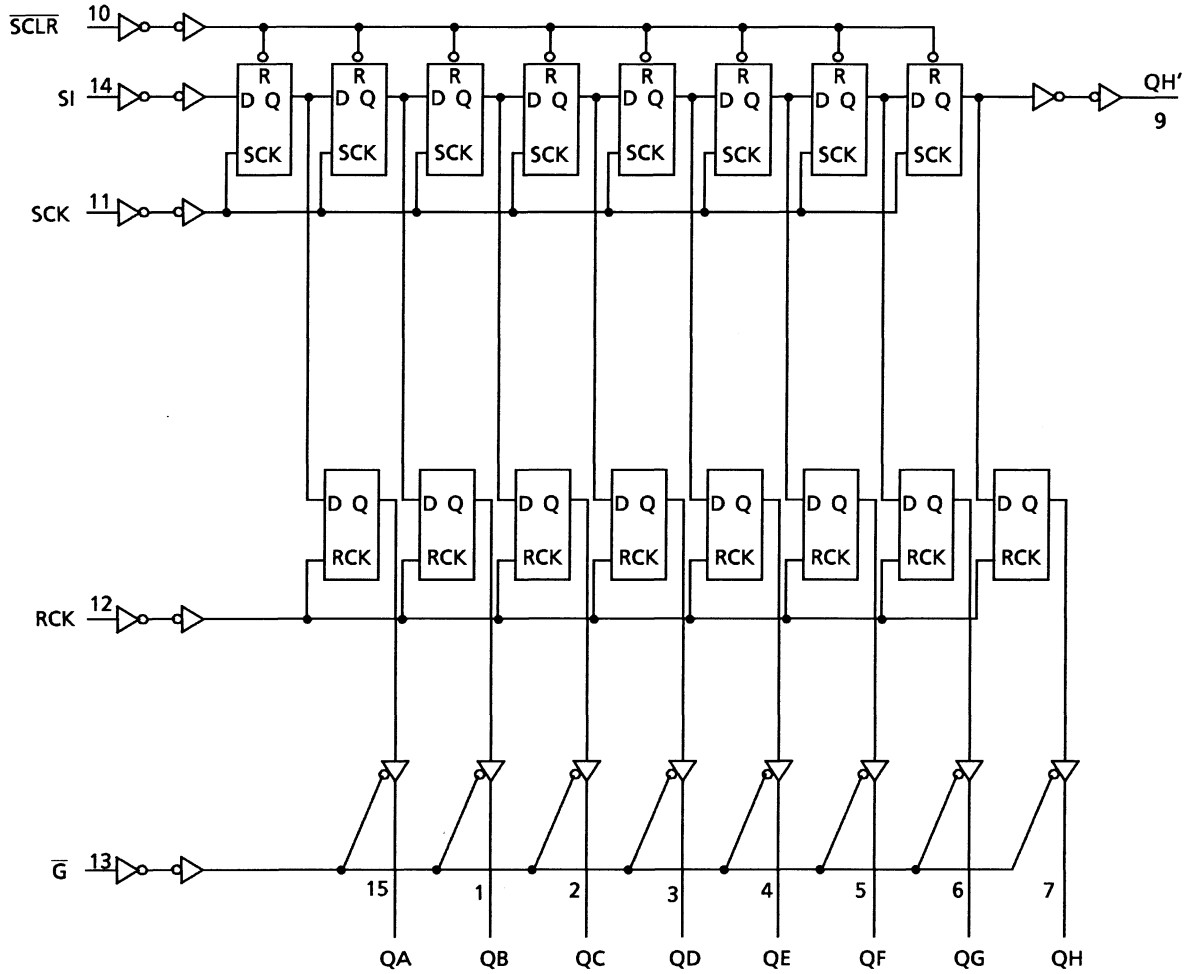
Inputs					Function
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes “L”. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes “H”. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register stage is not changed.

X: Don’t care

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current (QH') (QA to QH)	I_{OUT}	±25 ±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 125	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Ta = −40 to 125°C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	Min	Max	
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	3.15	—	
				6.0	4.20	—	—	4.20	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	5.9	—	
		QH'	I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	3.7	—	V
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	5.2	—	
		QA to QH	I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	3.7	—	
			I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	5.2	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	—	0.1	
		QH'	I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	—	0.4	V
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	—	0.4	
		QA to QH	I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	—	0.4	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	—	0.4	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	—	±10.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	—	160.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Ta = −40 to 125°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	Limit	
Minimum pulse width (SCK, RCK)	$t_{W\ (H)}$ $t_{W\ (L)}$	—	2.0	—	75	95	110	ns
			4.5	—	15	19	22	
			6.0	—	13	16	19	
Minimum pulse width ($\overline{SCLR}$)	$t_{W\ (L)}$	—	2.0	—	75	95	110	ns
			4.5	—	15	19	22	
			6.0	—	13	16	19	
Minimum set-up time (SI-SCK)	t_s	—	2.0	—	50	65	75	ns
			4.5	—	10	13	15	
			6.0	—	9	11	13	
Minimum set-up time (SCK-RCK)	t_s	—	2.0	—	75	95	110	ns
			4.5	—	15	19	22	
			6.0	—	13	16	19	
Minimum set-up time ($\overline{SCLR}$ -RCK)	t_s	—	2.0	—	100	125	150	ns
			4.5	—	20	25	30	
			6.0	—	17	21	26	
Minimum hold time	t_h	—	2.0	—	0	0	0	ns
			4.5	—	0	0	0	
			6.0	—	0	0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	—	2.0	—	50	65	75	ns
			4.5	—	10	13	15	
			6.0	—	9	11	13	
Clock frequency	f	—	2.0	—	6	5	4	MHz
			4.5	—	30	25	20	
			6.0	—	35	28	24	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time (QH')	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (SCK-QH')	t_{pLH} t_{pHL}	—	—	12	21	ns
Propagation delay time ($\overline{SCLR}$ -QH')	t_{pHL}	—	—	15	30	ns
Maximum clock frequency	f_{max}	—	35	77	—	MHz

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Ta = −40 to 125°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	Min	Max	
Output transition time (Q_n)	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	—	90	ns
				4.5	—	7	12	—	15	—	18	
				6.0	—	6	10	—	13	—	15	
Output transition time (QH')	t_{TLH} t_{THL}	—	50	2.0	—	30	75	—	95	—	115	ns
				4.5	—	8	15	—	19	—	23	
				6.0	—	7	13	—	16	—	20	
Propagation delay time (SCK-QH')	t_{pLH} t_{pHL}	—	50	2.0	—	45	125	—	155	—	240	ns
				4.5	—	15	25	—	31	—	48	
				6.0	—	13	21	—	26	—	31	
Propagation delay time ($\overline{SCLR}$ -QH')	t_{pHL}	—	50	2.0	—	60	175	—	220	—	265	ns
				4.5	—	18	35	—	44	—	53	
				6.0	—	15	30	—	37	—	45	
Propagation delay time (RCK-Q_n)	t_{pLH} t_{pHL}	—	50	2.0	—	60	150	—	190	—	265	ns
				4.5	—	20	30	—	38	—	53	
				6.0	—	17	26	—	32	—	45	
			150	2.0	—	75	190	—	240	—	285	
				4.5	—	25	38	—	48	—	57	
				6.0	—	22	32	—	41	—	48	
Output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	—	45	135	—	170	—	225	ns
				4.5	—	15	27	—	34	—	45	
				6.0	—	13	23	—	29	—	38	
			150	2.0	—	60	175	—	220	—	265	
				4.5	—	20	35	—	44	—	53	
				6.0	—	17	30	—	37	—	45	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	—	30	150	—	190	—	225	ns
				4.5	—	15	30	—	38	—	45	
				6.0	—	14	26	—	33	—	38	
Maximum clock frequency	f_{max}	—	50	2.0	6	17	—	5	—	4	—	MHz
				4.5	30	50	—	25	—	20	—	
				6.0	35	59	—	28	—	24	—	
Input capacitance	C_{IN}	—			—	3	—	—	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	41	—	—	—	—	—	pF

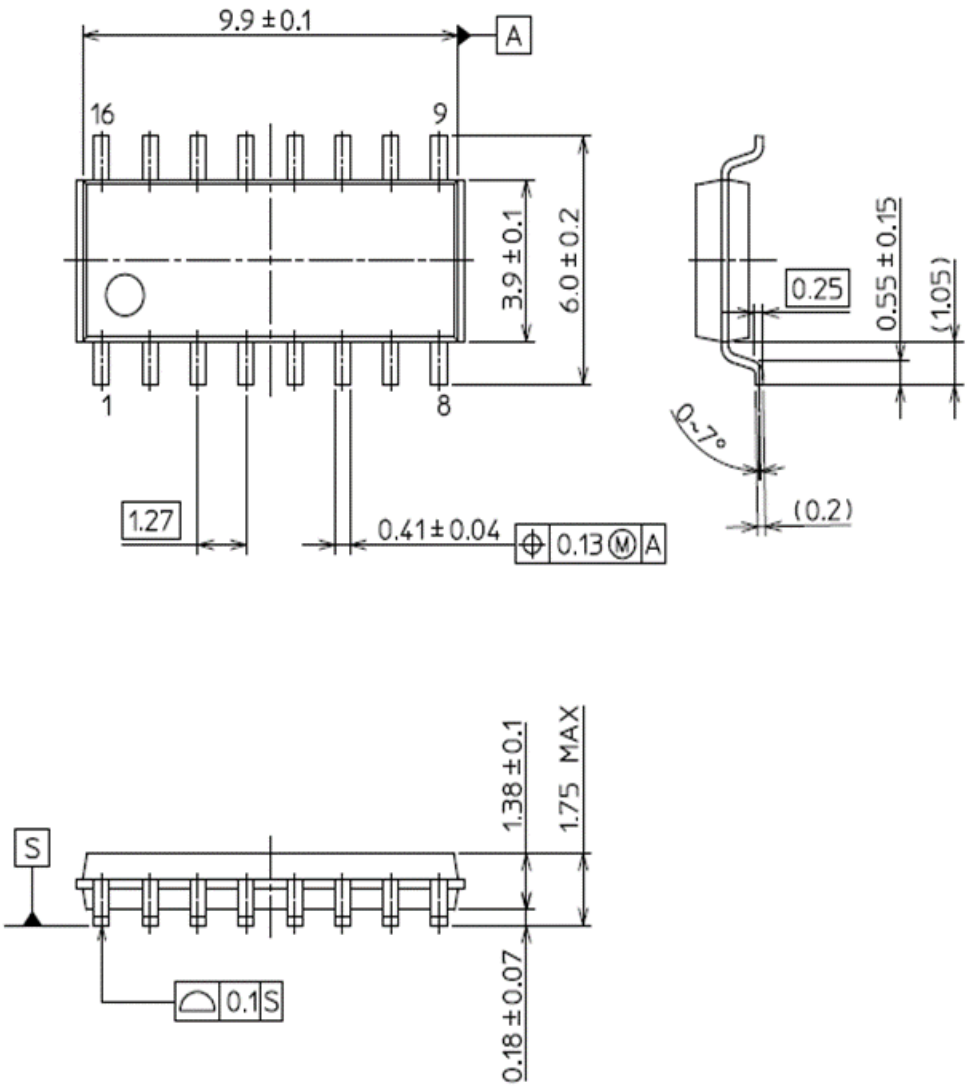
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

P-SOP16-0410-1.27-005 Unit:mm



Weight: 0.15 g (typ.)

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