

# 74LCX373FT

## 1. Functional Description

- Low-Voltage Octal D-Type Latch with 5-V Tolerant Inputs and Outputs

## 2. General

The 74LCX373FT is a high-performance CMOS octal D-type latch. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ).

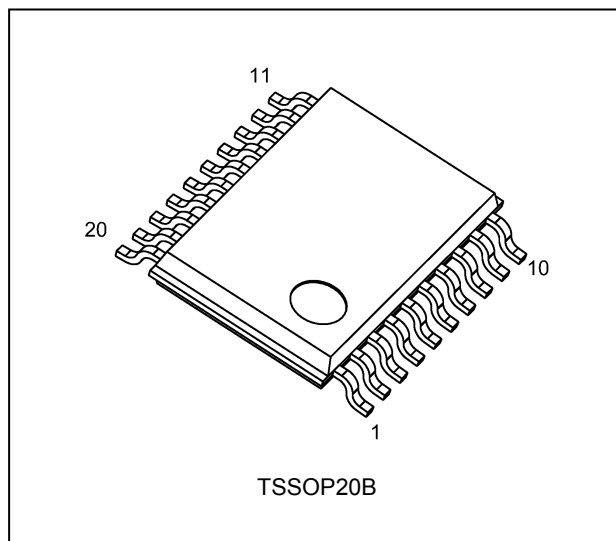
When the  $\overline{OE}$  input is high, the eight outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

## 3. Features

- (1) Low-voltage operation:  $V_{CC} = 1.65$  to 3.6 V
- (2) High-speed operation:  $t_{pd} = 8.0$  ns (max) ( $V_{CC} = 3.0$  to 3.6 V)
- (3) Output current:  $|I_{OH}|/I_{OL} = 24$  mA (min) ( $V_{CC} = 3.0$  to 3.6 V)
- (4) Power-down protection provided on all inputs and outputs
- (5) Pin and function compatible with the 74 series  
(74LVC/ALVC/ etc.) 373 type

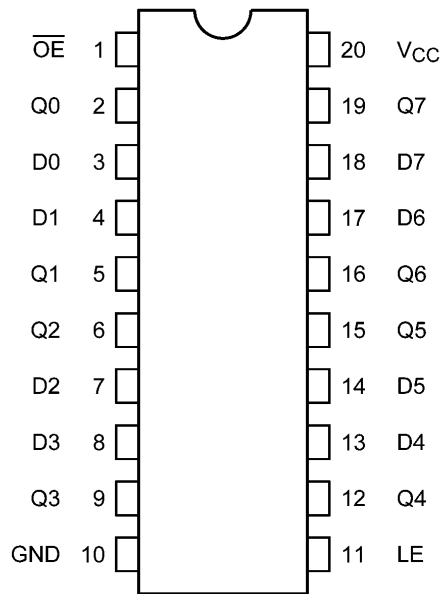
## 4. Packaging



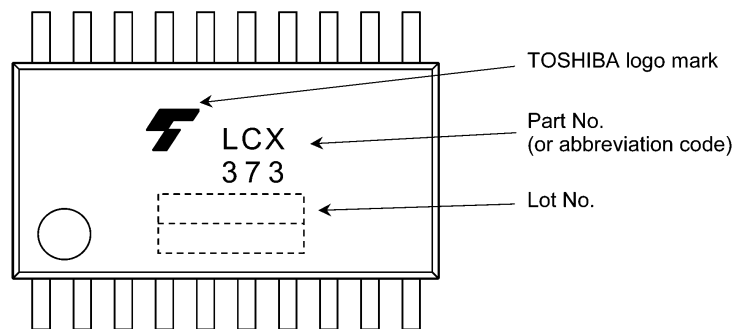
Start of commercial production

2013-11

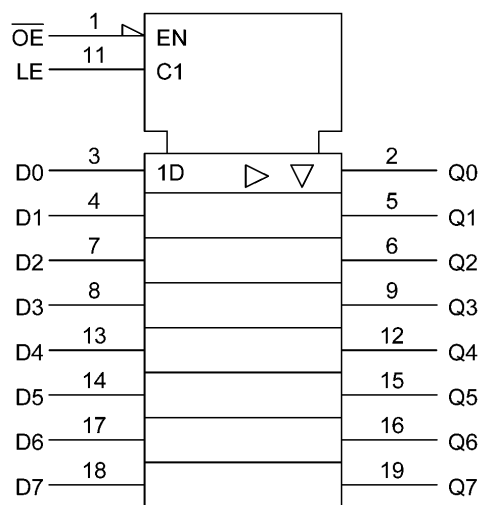
**5. Pin Assignment**



**6. Marking**



**7. IEC Logic Symbol**



**8. Truth Table**

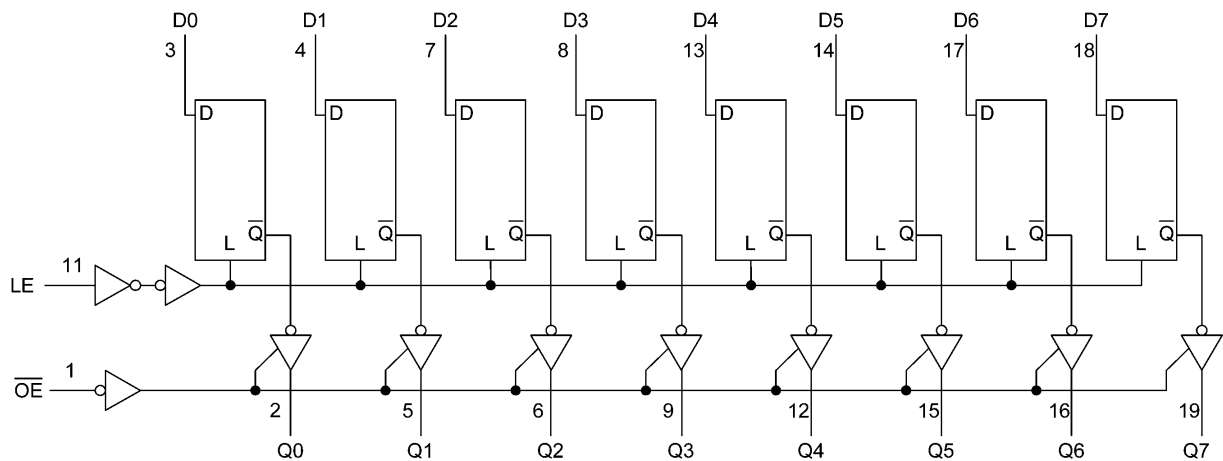
Input $\overline{OE}$	Input LE	Input D	Outputs
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

**9. System Diagram**



**10. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 6.5	V
Input voltage	$V_{IN}$		-0.5 to 6.5	V
Output voltage	$V_{OUT}$	(Note 1)	-0.5 to 6.5	V
		(Note 2)	-0.5 to $V_{CC} + 0.5$	
Input diode current	$I_{IK}$		-50	mA
Output diode current	$I_{OK}$	(Note 3)	$\pm 50$	mA
Output current	$I_{OUT}$		$\pm 50$	mA
Power dissipation	$P_D$		180	mW
$V_{CC}$ /ground current	$I_{CC}/I_{GND}$		$\pm 100$	mA
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 3:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

**11. Operating Ranges (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		1.65 to 3.6	V
		(Note 1)	1.5 to 3.6	
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$	(Note 2)	0 to 5.5	V
		(Note 3)	0 to $V_{CC}$	
Output current	$I_{OUT}$	(Note 4)	$\pm 24$	mA
		(Note 5)	$\pm 12$	
Operating temperature	$T_{opr}$		-40 to 85	$^{\circ}C$
Input rise and fall times	dt/dv	(Note 6)	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 1: Data retention only

Note 2: Output in OFF state

Note 3: High or low state

Note 4:  $V_{CC} = 3.0$  to  $3.6$  V

Note 5:  $V_{CC} = 2.7$  to  $3.0$  V

Note 6:  $V_{IN} = 0.8$  to  $2.0$  V ,  $V_{CC} = 3.0$  V

**12. Electrical Characteristics**

**12.1. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	1.65 to 2.3	$V_{CC} \times 0.9$	—	V	
			2.3 to 2.7	1.7	—		
			2.7 to 3.6	2.0	—		
Low-level input voltage	$V_{IL}$	—	1.65 to 2.3	—	$V_{CC} \times 0.1$		
			2.3 to 2.7	—	0.7		
			2.7 to 3.6	—	0.8		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -100 \mu\text{A}$	1.65 to 3.6	$V_{CC} - 0.2$	—	V
			$I_{OH} = -4 \text{ mA}$	1.65	1.05	—	
			$I_{OH} = -8 \text{ mA}$	2.3	1.7	—	
			$I_{OH} = -12 \text{ mA}$	2.7	2.2	—	
			$I_{OH} = -18 \text{ mA}$	3.0	2.4	—	
			$I_{OH} = -24 \text{ mA}$	3.0	2.2	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 100 \mu\text{A}$	1.65 to 3.6	—	0.2	
			$I_{OL} = 4 \text{ mA}$	1.65	—	0.45	
			$I_{OL} = 8 \text{ mA}$	2.3	—	0.7	
			$I_{OL} = 12 \text{ mA}$	2.7	—	0.4	
			$I_{OL} = 16 \text{ mA}$	3.0	—	0.4	
			$I_{OL} = 24 \text{ mA}$	3.0	—	0.55	
Input leakage current	$I_{IN}$	$V_{IN} = 0$ to $5.5 \text{ V}$	1.65 to 3.6	—	$\pm 5.0$	$\mu\text{A}$	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = 0$ to $5.5 \text{ V}$	1.65 to 3.6	—	$\pm 5.0$	$\mu\text{A}$	
Power-OFF leakage current	$I_{OFF}$	$V_{IN}/V_{OUT} = 5.5 \text{ V}$	0	—	10.0	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	1.65 to 3.6	—	10.0	$\mu\text{A}$	
		$V_{IN}/V_{OUT} = 3.6$ to $5.5 \text{ V}$	1.65 to 3.6	—	$\pm 10.0$		
Quiescent supply current	$\Delta I_{CC}$	$V_{IH} = V_{CC} - 0.6 \text{ V}$ (per input)	2.7 to 3.6	—	500		

**12.2. AC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Max	Unit
Propagation delay time (D-Q)	$t_{PLH}, t_{PHL}$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.1, Table 12.6.1	$1.8 \pm 0.15$	—	30.0	ns
				$2.5 \pm 0.2$	—	10.0	
				2.7	—	9.0	
				$3.3 \pm 0.3$	1.5	8.0	
Propagation delay time (LE-Q)	$t_{PLH}, t_{PHL}$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.1, Table 12.6.1	$1.8 \pm 0.15$	—	30.0	ns
				$2.5 \pm 0.2$	—	10.5	
				2.7	—	9.5	
				$3.3 \pm 0.3$	1.5	8.5	
Output enable time	$t_{PZL}, t_{PZH}$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.2, Table 12.6.1	$1.8 \pm 0.15$	—	34.0	ns
				$2.5 \pm 0.2$	—	17.0	
				2.7	—	9.5	
				$3.3 \pm 0.3$	1.5	8.5	
Output disable time	$t_{PLZ}, t_{PHZ}$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.2, Table 12.6.1	$1.8 \pm 0.15$	—	32.0	ns
				$2.5 \pm 0.2$	—	16.0	
				2.7	—	8.5	
				$3.3 \pm 0.3$	1.5	7.5	
Minimum pulse width (LE)	$t_{w(H)}$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.1, Table 12.6.1	$1.8 \pm 0.15$	12.0	—	ns
				$2.5 \pm 0.2$	6.0	—	
				2.7	4.0	—	
				$3.3 \pm 0.3$	3.3	—	
Minimum setup time	$t_s$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.1, Table 12.6.1	$1.8 \pm 0.15$	10.0	—	ns
				$2.5 \pm 0.2$	5.0	—	
				2.7	2.5	—	
				$3.3 \pm 0.3$	2.5	—	
Minimum hold time	$t_h$		See 12.5 AC Test Circuit, Table 12.5.1, Fig. 12.6.1, Table 12.6.1	$1.8 \pm 0.15$	1.5	—	ns
				$2.5 \pm 0.2$	1.5	—	
				2.7	1.5	—	
				$3.3 \pm 0.3$	1.5	—	
Output skew	$t_{osLH}, t_{osHL}$	(Note 1)	—	2.7	—	—	ns
				$3.3 \pm 0.3$	—	1.0	

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{osHL} = |t_{PHLm} - t_{PHLn}|$ )

**12.3. Dynamic Switching Characteristics (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ , Input:  $t_r = t_f = 2.5$  ns,  $C_L = 50$  pF,  $R_L = 500 \Omega$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$V_{IH} = 3.3$ V, $V_{IL} = 0$ V	3.3	0.8	V
Quiet output minimum dynamic $V_{OL}$	$ V_{OLV} $	$V_{IH} = 3.3$ V, $V_{IL} = 0$ V	3.3	0.8	V

**12.4. Capacitive Characteristics (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Typ.	Unit
Input capacitance	$C_{IN}$		—	3.3	7	pF
Output capacitance	$C_{OUT}$		—	3.3	8	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	$f_{IN} = 10$ MHz	3.3	25	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per bit)}$$

12.5. AC Test Circuit

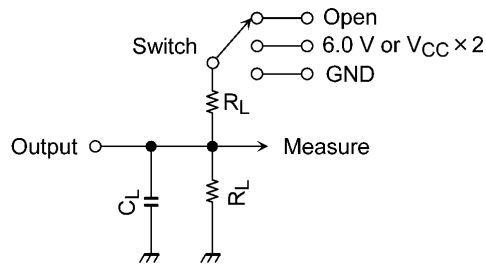
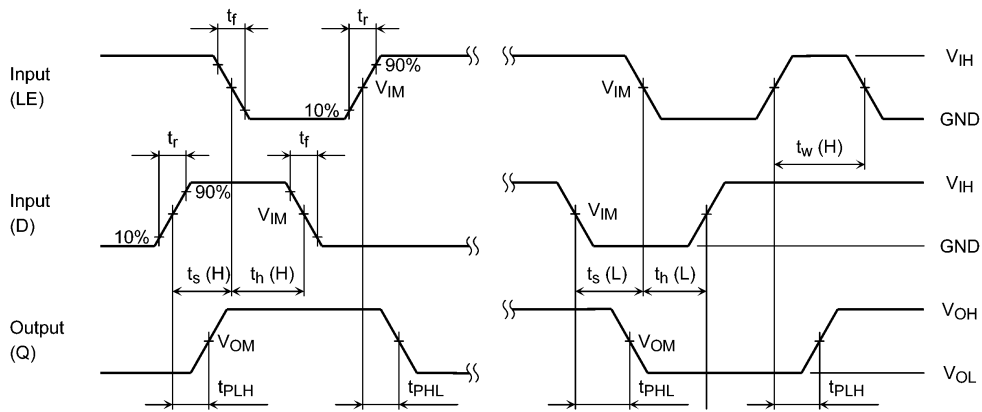


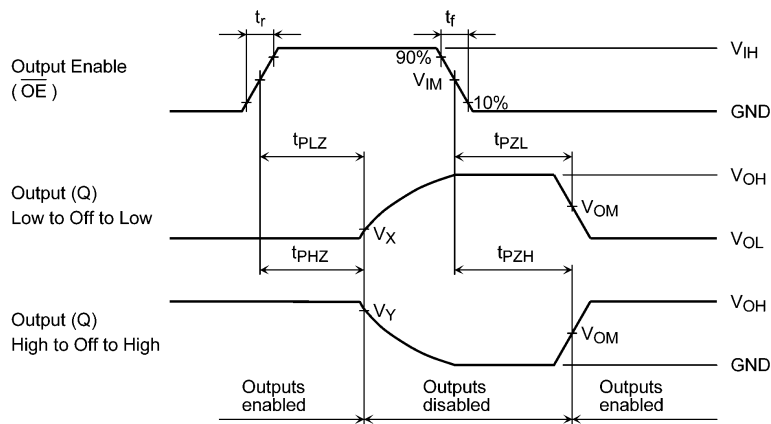
Table 12.5.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
$t_{PLH}, t_{PHL}$	OPEN	—
$t_{PLZ}, t_{PZL}$	6.0 V	$V_{CC} = 3.3 \pm 0.3 \text{ V}$
		$V_{CC} = 2.7 \text{ V}$
	$V_{CC} \times 2$	$V_{CC} = 2.5 \pm 0.2 \text{ V}$
		$V_{CC} = 1.8 \pm 0.15 \text{ V}$
$t_{PHZ}, t_{PZH}$	GND	—
$t_w, t_s, t_h$	OPEN	—

**12.6. AC Waveform**



**Fig. 12.6.1  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$**



**Fig. 12.6.2  $t_{PLZ}$ ,  $t_{PHZ}$ ,  $t_{PZL}$ ,  $t_{PZH}$**

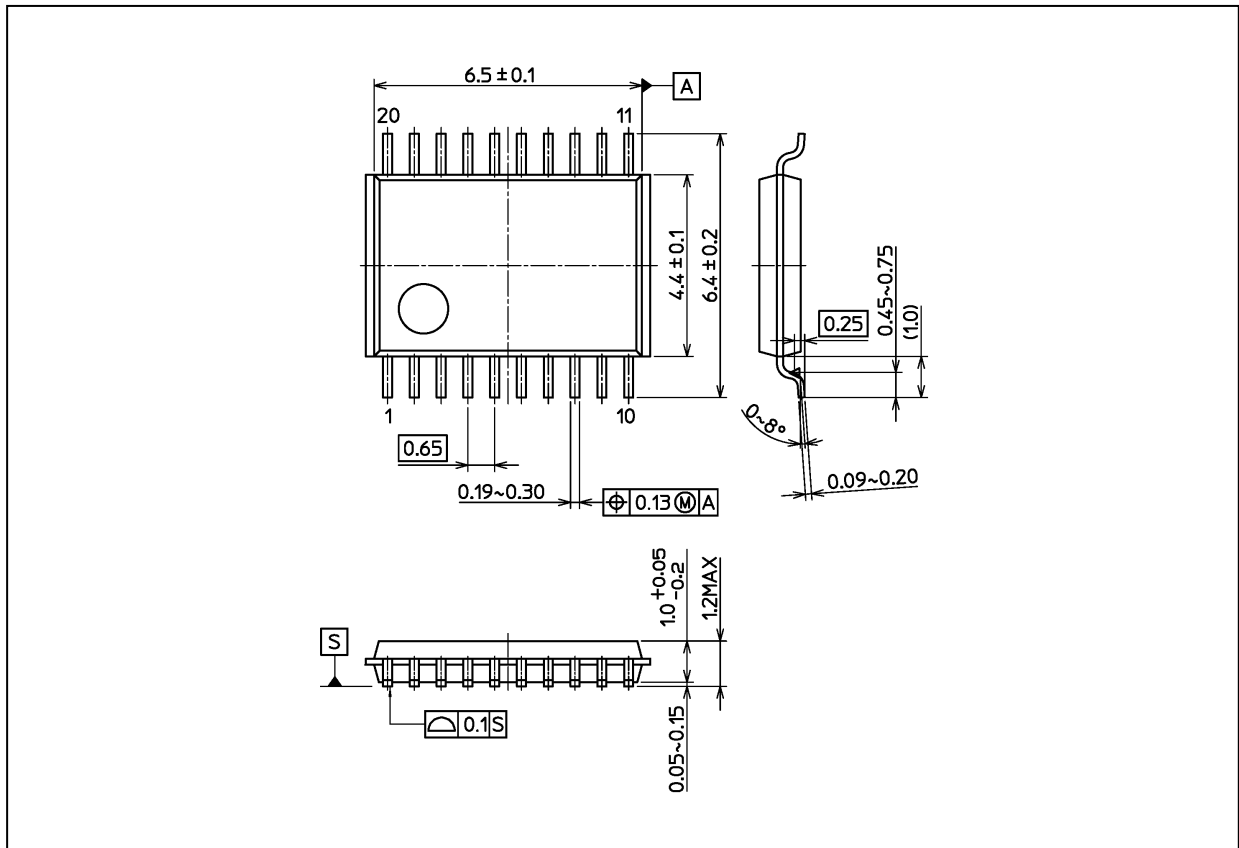
**Table 12.6.1 AC Waveform Symbols**

	Symbol	$V_{CC} = 3.3 \pm 0.3 V$ $V_{CC} = 2.7 V$	$V_{CC} = 2.5 \pm 0.2 V$	$V_{CC} = 1.8 \pm 0.15 V$
Input	$V_{IH}$	2.7 V	$V_{CC}$	$V_{CC}$
	$V_{IM}$	1.5 V	$V_{CC}/2$	$V_{CC}/2$
	$t_r, t_f$	2.5 ns	2.0 ns	2.0 ns
Output	$V_{OM}$	1.5 V	$V_{OH}/2$	$V_{OH}/2$
	$V_X$	$V_{OL} + 0.3 V$	$V_{OL} + 0.15 V$	$V_{OL} + 0.15 V$
	$V_Y$	$V_{OH} - 0.3 V$	$V_{OL} - 0.15 V$	$V_{OL} - 0.15 V$
Load	$C_L$	50 pF	30 pF	30 pF
	$R_L$	500 $\Omega$	500 $\Omega$	1 k $\Omega$



Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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