

CMOS Digital Integrated Circuits Silicon Monolithic

# 74VHC9125FT,74VHC9126FT

## 1. Functional Description

- 5-Bit Universal Schmitt Buffer with 3-State Outputs

## 2. General

The 74VHC9125FT/74VHC9126FT are an ultra-high-speed 5-bit Schmitt buffer fabricated using silicon-gate CMOS technology. The 74VHC9125FT/74VHC9126FT combines low power consumption of CMOS with Schottky TTL speeds.

Y1 to Y4 outputs can be put in the high-impedance state by placing a logic HIGH on the Enable ( $\overline{G}$ ) input. The CONT input determines the logical inversion of data. A logic LOW on the CONT input configures the 74VHC9125FT/74VHC9126FT as an inverter; a logic HIGH on the CONT input configures the 74VHC9125FT/74VHC9126FT as a buffer.

74VHC9125FT Y5 output is an inverting type, and the 74VHC9126FT Y5 output is a non-inverting type.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHC9125FT/74VHC9126FT are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

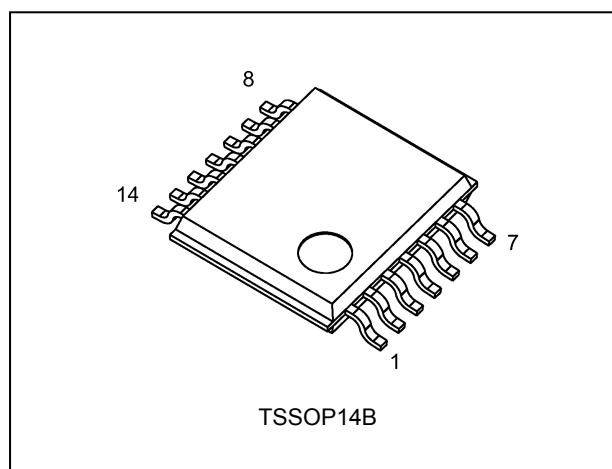
Additionally, all the inputs have a newly developed protection circuit without a diode returned to  $V_{CC}$ . This enables the inputs to be tolerant of up to 5 volts even when power supply is down. The input power-down protection capability makes the 74VHC9125FT/74VHC9126FT ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

## 3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed:  $t_{pd} = 5.0$  ns (typ.) at  $V_{CC} = 5.0$  V
- (4) Low supply current:  $I_{CC} = 2.0$   $\mu$ A (max) ( $T_a = 25$  °C)
- (5) All inputs are provided with power-down protection.
- (6) Symmetrical rise and fall delays:  $t_{PLH} \approx t_{PHL}$
- (7) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to  $5.5$  V

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

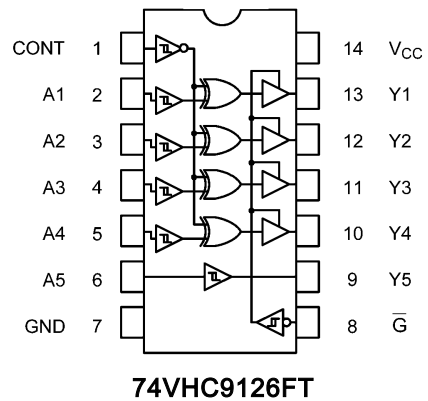
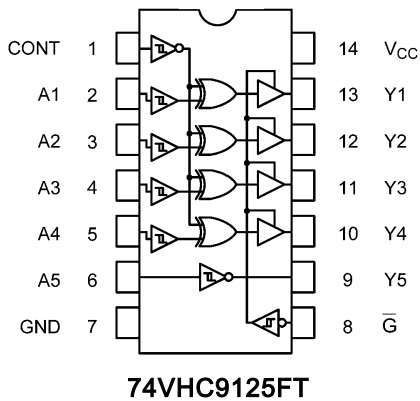
## 4. Packaging



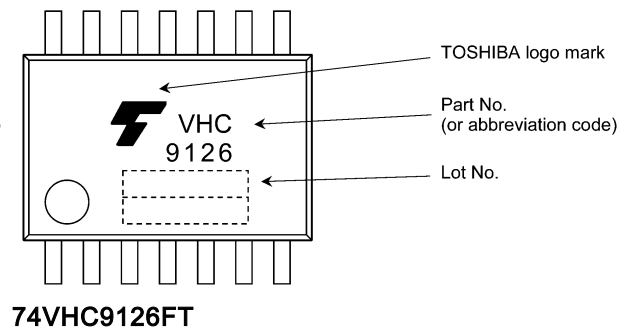
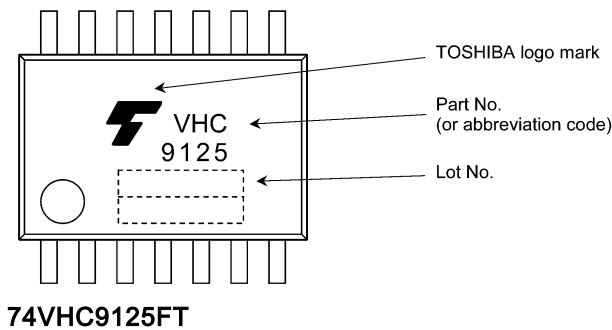
Start of commercial production

2014-06

### 5. Pin Assignment



### 6. Marking



### 7. Truth Table

Inputs			Outputs
$\bar{G}$	CONT	A1 to 4	Y1 to 4
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

Inputs	Outputs	
A5	Y5(9125)	Y5(9126)
L	H	L
H	L	H

X: Don't care (L or H)  
Z: High impedance

### 8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85$  °C. From  $T_a = 85$  to  $125$  °C a derating factor of  $-3.25$  mW/°C shall be applied until 50 mW.

### 9. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 125	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

### 10. Electrical Characteristics

#### 10.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit		
Positive threshold voltage	$V_P$	—	3.0	—	—	2.20	V		
			4.5	—	—	3.15			
			5.5	—	—	3.85			
Negative threshold voltage	$V_N$	—	3.0	0.90	—	—	V		
			4.5	1.35	—	—			
			5.5	1.65	—	—			
Hysteresis voltage	$V_H$	—	3.0	0.30	—	1.20	V		
			4.5	0.40	—	1.40			
			5.5	0.50	—	1.60			
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V	
				3.0	2.9	3.0	—		
			$I_{OH} = -4\text{ mA}$	4.5	4.4	4.5	—		
				$I_{OH} = -8\text{ mA}$	3.0	2.58	—		—
					4.5	3.94	—		—
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V	
				3.0	—	0.0	0.1		
				4.5	—	0.0	0.1		
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36		
				4.5	—	—	0.36		
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 0.25$	$\mu\text{A}$		
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$		
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	$\mu\text{A}$		

### 10.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85$ °C)

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
Positive threshold voltage	$V_P$	—		3.0	—	2.20	V
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	$V_N$	—		3.0	0.90	—	V
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	$V_H$	—		3.0	0.30	1.20	V
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4$ mA	3.0	2.48	—	
			$I_{OH} = -8$ mA	4.5	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4$ mA	3.0	—	0.44	
			$I_{OL} = 8$ mA	4.5	—	0.44	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	$\pm 2.50$	$\mu A$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	$\pm 1.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	20.0	$\mu A$

### 10.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125$ °C)

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
Positive threshold voltage	$V_P$	—		3.0	—	2.20	V
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	$V_N$	—		3.0	0.90	—	V
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	$V_H$	—		3.0	0.30	1.20	V
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V
				3.0	2.9	—	
			4.5	4.4	—	$I_{OH} = -4$ mA	
			4.5	3.70	—		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			3.0	—	0.55	$I_{OL} = 4$ mA	
			4.5	—	0.55		
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	$\pm 10.0$	$\mu A$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	$\pm 2.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	$\mu A$

### 10.4. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 3\text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time (A1 to A4 - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	6.0	8.0	ns
					50	—	9.0	12.5	
				$5.0 \pm 0.5$	15	—	5.0	5.5	
					50	—	7.0	8.5	
Propagation delay time (CONT - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	8.5	11.5	ns
					50	—	13.0	17.0	
				$5.0 \pm 0.5$	15	—	6.5	8.0	
					50	—	10.5	12.5	
Propagation delay time (A5 - Y5)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	6.0	8.0	ns
					50	—	9.0	12.5	
				$5.0 \pm 0.5$	15	—	5.0	5.5	
					50	—	7.0	8.5	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	—	6.0	8.0	ns
					50	—	10.5	13.5	
				$5.0 \pm 0.5$	15	—	4.5	5.5	
					50	—	9.0	10.5	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	—	12.5	13.5	ns
				$5.0 \pm 0.5$	50	—	9.0	9.5	
Output skew (A1 to A4 - Y1 to Y4)	$t_{oS LH}, t_{oS HL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	—	1.5	ns
				$5.0 \pm 0.5$	50	—	—	1.0	
Input capacitance	$C_{IN}$		—			—	4	10	pF
Output capacitance	$C_{OUT}$		—			—	6	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 2)	$f_{IN} = 1\text{ MHz}$			—	10	—	pF

Note 1: Parameter guaranteed by design. ( $t_{oS LH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$ )

Note 2:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/5 \text{ (per bit)}$$

### 10.5. AC Characteristics

(Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (A1 to A4 - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	10.0	ns
					50	1.0	15.0	
				$5.0 \pm 0.5$	15	1.0	7.0	
					50	1.0	10.0	
Propagation delay time (CONT - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	13.5	ns
					50	1.0	20.5	
				$5.0 \pm 0.5$	15	1.0	9.5	
					50	1.0	15.0	
Propagation delay time (A5 - Y5)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	10.0	ns
					50	1.0	15.0	
				$5.0 \pm 0.5$	15	1.0	7.0	
					50	1.0	10.0	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	1.0	9.5	ns
					50	1.0	16.5	
				$5.0 \pm 0.5$	15	1.0	6.5	
					50	1.0	12.5	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	1.0	16.0	ns
				$5.0 \pm 0.5$	50	1.0	11.0	
Output skew (A1 to A4 - Y1 to Y4)	$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	1.5	ns
				$5.0 \pm 0.5$	50	—	1.0	
Input capacitance	$C_{IN}$		—			—	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{osHL} = |t_{PHLm} - t_{PHLn}|$ )



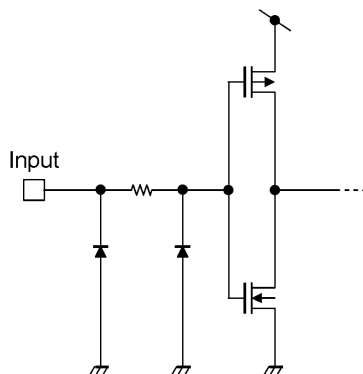
### 10.6. AC Characteristics

(Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (A1 to A4 - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	11.5	ns
					50	1.0	17.0	
				$5.0 \pm 0.5$	15	1.0	8.0	
					50	1.0	11.0	
Propagation delay time (CONT - Y1 to Y4)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	15.0	ns
					50	1.0	23.0	
				$5.0 \pm 0.5$	15	1.0	10.5	
					50	1.0	17.0	
Propagation delay time (A5 - Y5)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	11.5	ns
					50	1.0	17.0	
				$5.0 \pm 0.5$	15	1.0	8.0	
					50	1.0	11.0	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	15	1.0	10.5	ns
					50	1.0	18.5	
				$5.0 \pm 0.5$	15	1.0	7.5	
					50	1.0	14.0	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	50	1.0	18.0	ns
				$5.0 \pm 0.5$	50	1.0	12.0	
Output skew (A1 to A4 - Y1 to Y4)	$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	1.5	ns
				$5.0 \pm 0.5$	50	—	1.0	
Input capacitance	$C_{IN}$		—			—	10	pF

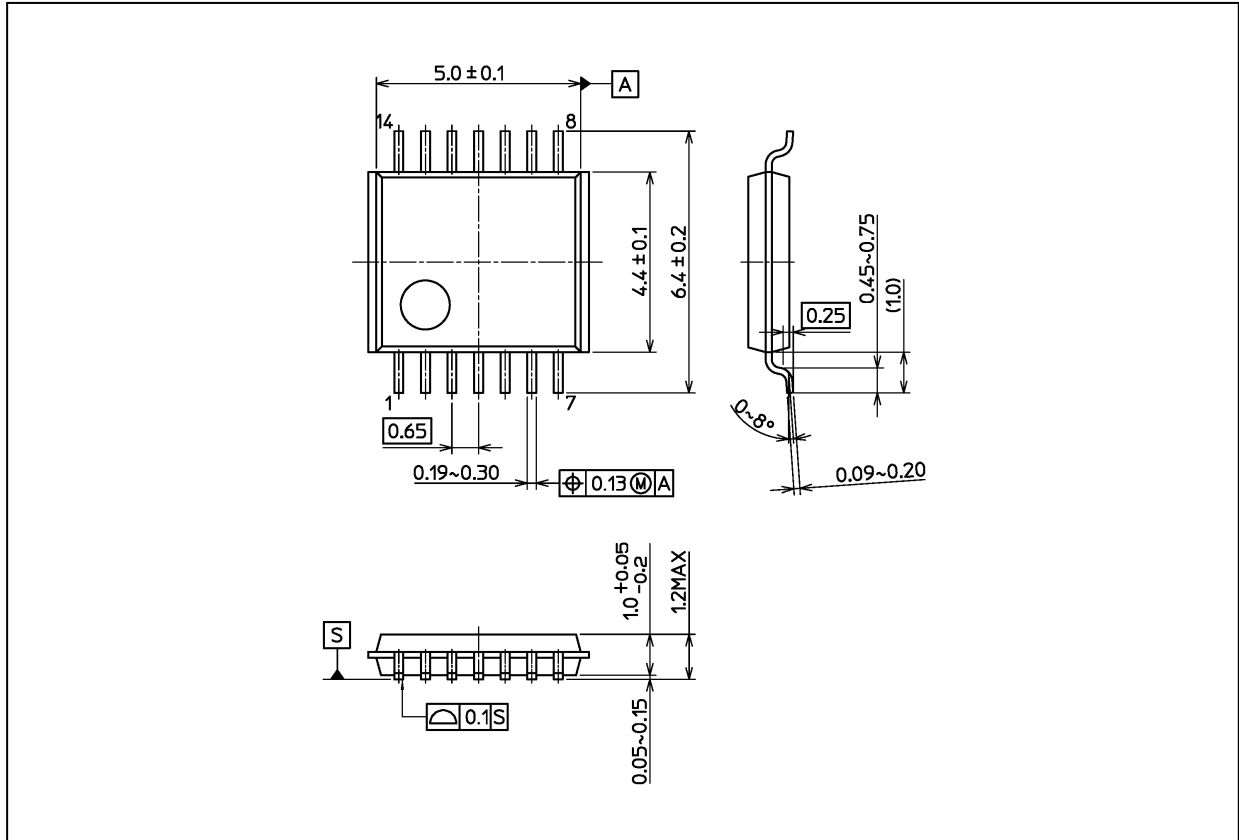
Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{osHL} = |t_{PHLM} - t_{PHLN}|$ )

### 11. Internal Equivalent Circuit



## Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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[7](#) [TC74HC4050AP\(F\)](#) [74LVCE1G07FZ4-7](#) [NLX3G16DMUTCG](#) [NLX2G06AMUTCG](#) [NLVVHC1G50DFT2G](#) [NLU2G17AMUTCG](#)  
[LE87100NQC](#) [LE87290YQC](#) [LE87290YQCT](#) [LE87511NQC](#) [LE87511NQCT](#) [LE87557NQC](#) [LE87557NQCT](#) [LE87614MQC](#)  
[LE87614MQCT](#) [74AUP1G125FW5-7](#) [NLU2G16CMUTCG](#) [MC74LCX244MN2TWG](#) [NLV74VHC125DTR2G](#) [NL17SG126DFT2G](#)