CMOS Digital Integrated Circuits Silicon Monolithic

74VHCT9541AFT

1. Functional Description

- Octal Universal Schmitt Buffer with 3-State Outputs

2. General

The 74VHCT9541AFT is an ultra-high-speed octal Schmitt buffer fabricated using silicon-gate CMOS technology.
The 74VHCT9541AFT combines low power consumption of CMOS with Schottky TTL speeds.
The input voltage are compatible with TTL output voltage.
This device may be used as a level converter for interfacing 3.3 V to 5 V system.
The outputs can be put in the high-impedance state by placing a logic HIGH on the Enable ($\overline{G}$) input. The CONT input determines the logical inversion of data. A logic LOW on the CONT input configures the 74VHCT9541AFT as an inverter; a logic HIGH on the CONT input configures the 74VHCT9541AFT as a buffer.
All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHCT9541AFT is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.
Note: Output in off-state

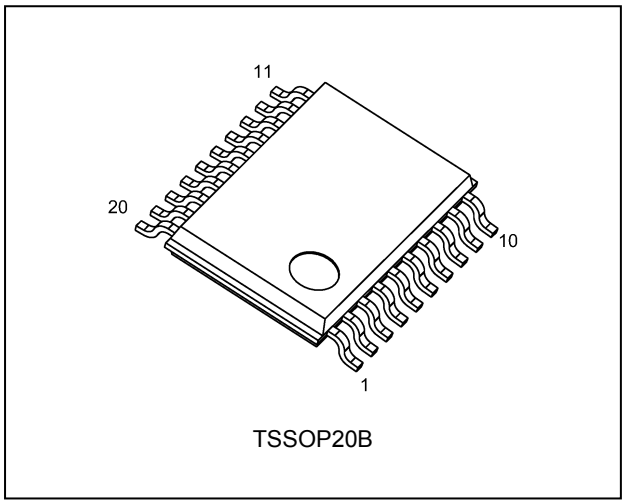
3. Features

(1) AEC-Q100 (Rev. H) (Note 1)
(2) Wide operating temperature range: T_{opr} = -40 to 125 °C
(3) High speed: t_{pd} = 6.5 ns (typ.) at V_{CC} = 5.0 V
(4) Low power dissipation: I_{CC} = 4.0 μA (max) (T_a = 25 °C)
(5) Compatible with TTL inputs: V_{IL} = 0.5 V (max)
V_{IH} = 2.1 V (min)
(6) Power down protection is provided on all inputs.
(7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(8) Input terminals are at the opposite side of Output terminals

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

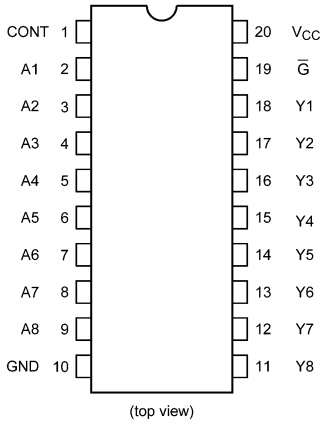
Start of commercial production
2014-12

4. Packaging

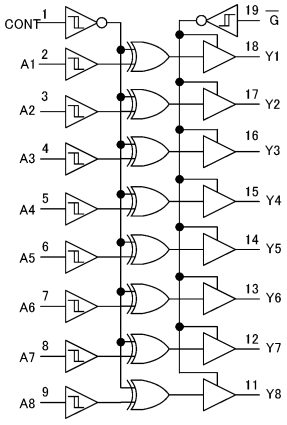


TSSOP20B

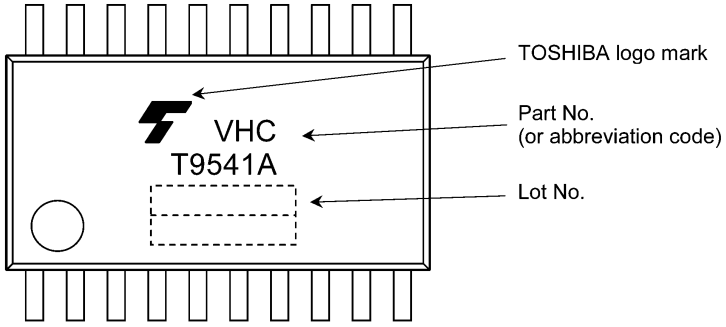
5. Pin Assignment



(top view)



6. Marking



7. Truth Table

Input $\overline{G}$	Input CONT	Input An	Output Yn
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

X: Don't care
Z: High impedance

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 7.0	V
		(Note 2)	-0.5 to V_{CC} + 0.5	
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}	(Note 3)	±20	mA
Output current	I_{OUT}		±25	mA
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 4)	180	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 3: V_{OUT} < GND, V_{OUT} > V_{CC}

Note 4: 180 mW in the range of T_a = -40 to 85 °C. From T_a = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		4.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}	(Note 1)	0 to 5.5	V
		(Note 2)	0 to V_{CC}	
Operating temperature	T_{opr}		-40 to 125	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Positive threshold voltage	V_P	—		4.5	—	—	1.90	V
				5.5	—	—	2.10	
Negative threshold voltage	V_N	—		4.5	0.50	—	—	V
				5.5	0.60	—	—	
Hysteresis voltage	V_H	—		4.5	0.40	—	1.40	V
				5.5	0.40	—	1.50	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	4.5	4.4	4.5	—	V
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	V
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	mA
Output leakage current (Power-OFF)	I_{OPD}	V_{OUT} = 5.5 V		0	—	—	0.5	μA

10.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		4.5	—	1.90	V
				5.5	—	2.10	
Negative threshold voltage	V_N	—		4.5	0.50	—	V
				5.5	0.60	—	
Hysteresis voltage	V_H	—		4.5	0.40	1.40	V
				5.5	0.40	1.50	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	4.5	4.4	—	V
			I_{OH} = -8 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.1	V
			I_{OL} = 8 mA	4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±2.5	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	40.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	1.50	mA
Output leakage current (Power-OFF)	I_{OPD}	V_{OUT} = 5.5 V		0	—	5.0	μA

10.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		4.5	—	1.90	V
				5.5	—	2.10	
Negative threshold voltage	V_N	—		4.5	0.50	—	V
				5.5	0.60	—	
Hysteresis voltage	V_H	—		4.5	0.40	1.40	V
				5.5	0.40	1.50	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	4.5	4.4	—	V
			I_{OH} = -8 mA	4.5	3.70	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.1	V
			I_{OL} = 8 mA	4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±10.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±2.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	80.0	μA
Quiescent supply current	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	1.50	mA
Output leakage current (Power-OFF)	I_{OPD}	V_{OUT} = 5.5 V		0	—	20.0	μA

10.4. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (An - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	—	6.5	8.5	ns
					50	—	8.6	11.5	
Propagation delay time (CONT - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	—	8.2	10.5	ns
					50	—	10.8	14.5	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	5.0 ± 0.5	15	—	6.9	8.5	ns
					50	—	9.1	12.5	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	5.0 ± 0.5	50	—	7.4	11.5	ns
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	5.0 ± 0.5	50	—	—	1.0	ns
Input capacitance	C_{IN}		—			—	4	10	pF
Output capacitance	C_{OUT}		—			—	9	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)	f_{IN} = 1 MHz			—	16	—	pF

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

10.5. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (An - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	1.0	10.0	ns
					50	1.0	13.0	
Propagation delay time (CONT - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	1.0	12.0	ns
					50	1.0	17.0	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	5.0 ± 0.5	15	1.0	10.0	ns
					50	1.0	14.5	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	5.0 ± 0.5	50	1.0	13.0	ns
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	5.0 ± 0.5	50	—	1.0	ns
Input capacitance	C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.6. AC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (An - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	1.0	11.0	ns
					50	1.0	14.0	
Propagation delay time (CONT - Yn)	t_{PLH},t_{PHL}		—	5.0 ± 0.5	15	1.0	13.0	ns
					50	1.0	19.0	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	5.0 ± 0.5	15	1.0	11.0	ns
					50	1.0	16.0	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	5.0 ± 0.5	50	1.0	14.0	ns
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	5.0 ± 0.5	50	—	1.0	ns
Input capacitance	C_{IN}		—			—	10	pF

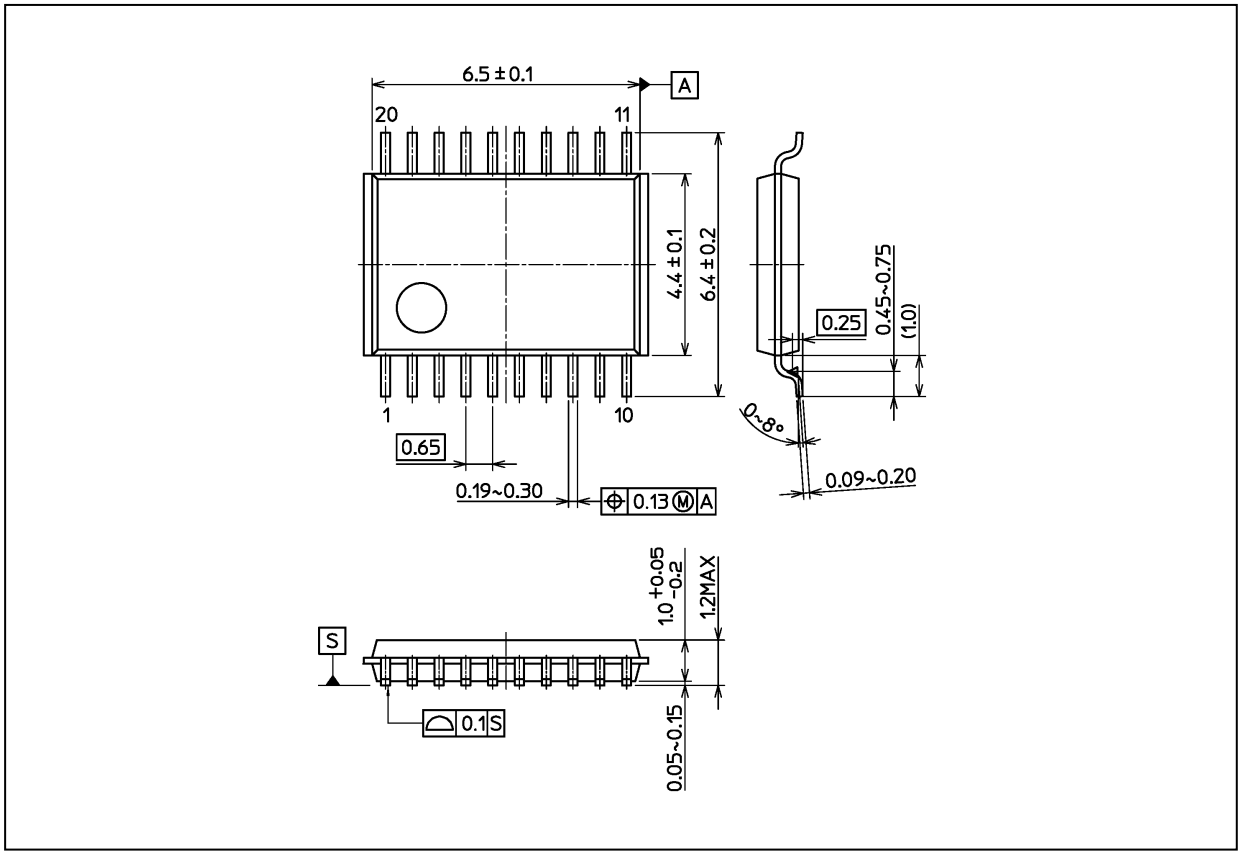
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11. Noise Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	1.0	1.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	-0.3	-1.5	V
Minimum high-level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	2.1	V
Maximum low-level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	0.5	V

Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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