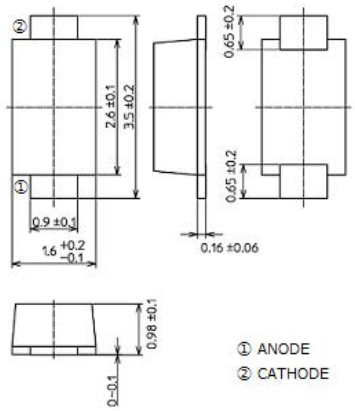
TOSHIBA High Efficiency Rectifier Silicon Epitaxial Type

CRH01

Switching Mode Power Supply Applications

- Repetitive peak reverse voltage : V_{RRM} = 200 V
- Average forward current : $I_{F\ (AV)}$ = 1 A
- Peak forward voltage : V_{FM} = 0.98 V (Max.)
- Very Fast Reverse-Recovery Time : t_{rr} = 35 ns (Max.)
- Suitable for compact assembly due to small surface-mount package "S−FLAT™" (Toshiba package name)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	3-2A1A

Weight: 0.013 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Repetitive peak reverse voltage	V_{RRM}	200	V
Average forward current	$I_{F(AV)}$	1	A
Non-repetitive peak forward surge current	I_{FSM}	15 (50 Hz)	A
Junction temperature	T_j	−40 to 150	°C
Storage temperature	T_{stg}	−40 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

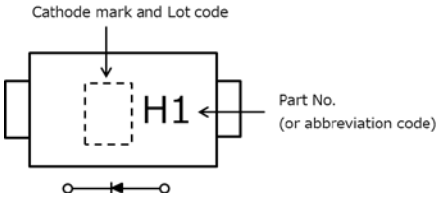
Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Peak forward voltage	$V_{FM\ (1)}$	I_{FM} = 0.1 A (pulse test)	—	0.71	—	V
	$V_{FM\ (2)}$	I_{FM} = 0.7 A (pulse test)	—	0.86	—	
	$V_{FM\ (3)}$	I_{FM} = 1 A (pulse test)	—	0.90	0.98	
Repetitive peak reverse current	I_{RRM}	V_{RRM} = 200 V (pulse test)	—	—	10	μA
Reverse recovery time	t_{rr}	I_F = 1 A, di/dt = −30 A/μs	—	—	35	ns
Forward recovery time	t_{fr}	I_F = 1 A	—	—	100	ns
Thermal resistance (junction to ambient)	$R_{th\ (j-a)}$	Device mounted on a ceramic board board size : 50 mm × 50 mm soldering land size : 2 mm × 2 mm board thickness : 0.64 mm	—	—	65	°C/W
		Device mounted on a glass-epoxy board board size : 50 mm × 50 mm soldering land size : 6 mm × 6 mm board thickness : 1.6 mm	—	—	130	

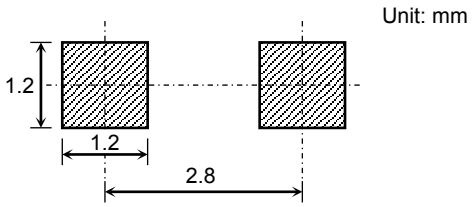
Start of commercial production
1999-07

Marking

Abbreviation Code	Part No.
H1	CRH01



Land pattern dimensions for reference only



Handling Precaution

1) The absolute maximum ratings are rated values that must not be exceeded during operation, even for an instant. The following are the recommended general derating methods for designing a circuit board using this device.

   VRRM : We recommend that the worst case voltage, including surge voltage, be no greater than 80% of the absolute maximum rating of V_{RRM} for a DC circuit and be no greater than 50% of that of V_{RRM} for an AC circuit. V_{RRM} has a temperature coefficient of 0.1%/°C. Take this temperature coefficient into account designing a device at low temperature.

   $I_{F\ (AV)}$:We recommend that the worst case current be no greater than 80% of the absolute maximum rating of $I_{F\ (AV)}$ and T_j be below 120°C. When using this device, take the margin into consideration by using an allowable Ta max-$I_{F\ (AV)}$ curve.

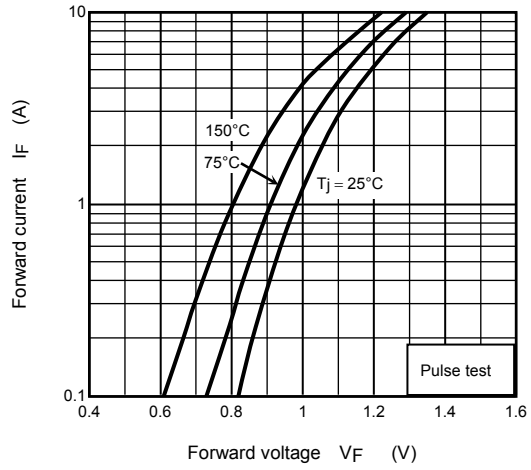
   IFSM :This rating specifies peak non-repetitive forward surge current. This only applies to an abnormal operation, which seldom occurs during the lifespan of a device.

   Tj :Derate device parameters in proportion to this rating in order to ensure high reliability. We recommend that the junction temperature (Tj) of a device be kept below 120°C.

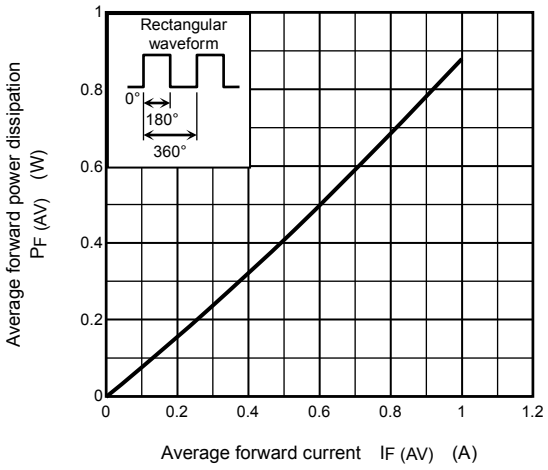
2) Thermal resistance (junction-to-ambient) varies with the mounting conditions of a device on a circuit board. An appropriate thermal resistance value should be used, considering the circuit board design and land pattern dimensions (provided for reference only).

3) For other design considerations, see the Rectifiers databook or the Toshiba website.

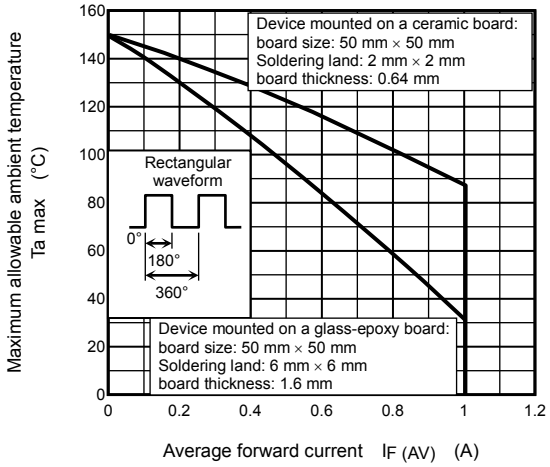
$I_F - V_F$



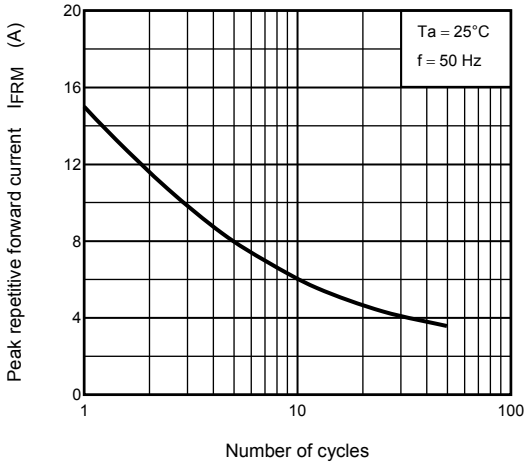
$P_{F\,(AV)} - I_{F\,(AV)}$



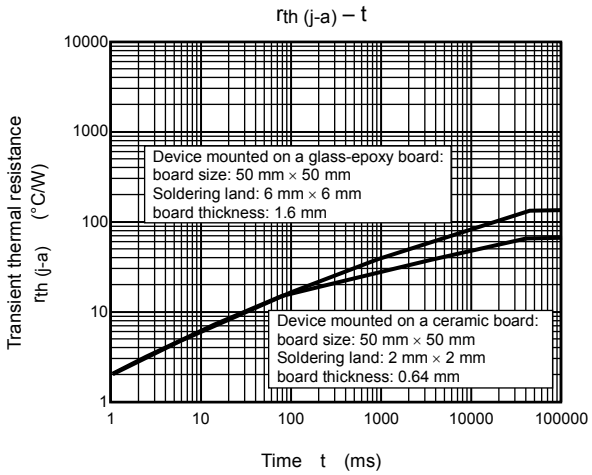
Ta max – $I_{F\,(AV)}$



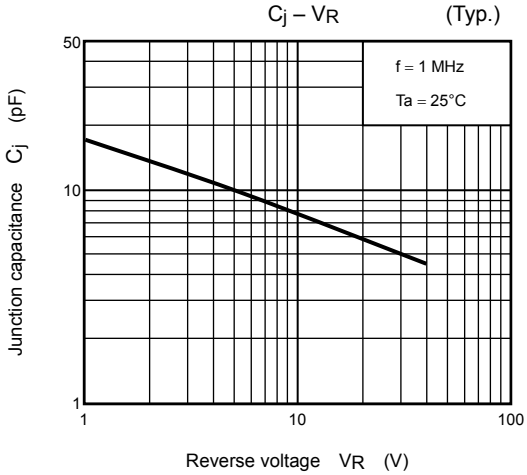
Peak repetitive forward current



$r_{th\,(j\text{-}a)} - t$



$C_j - V_R$ (Typ.)



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