

# DF2B20M4SL

## 1. General

The DF2B20M4SL is a bidirectional TVS diode with high  $V_{RWM}$  (18.5V) designed to protect high speed line or differential signal line from the damage caused by ESD and other transients voltage. This TVS diode can protect the latter part well by the low dynamic resistance, improve the system reliability level by the high  $V_{ESD}$  performance. It is optimum for antennal application such as NFC for the low capacitance performance. And the small package size (0.62 mm × 0.32 mm) is ideal for high-density mounting.

## 2. Applications

Mobile Equipment

- Smartphones
- Tablets
- Notebook PCs

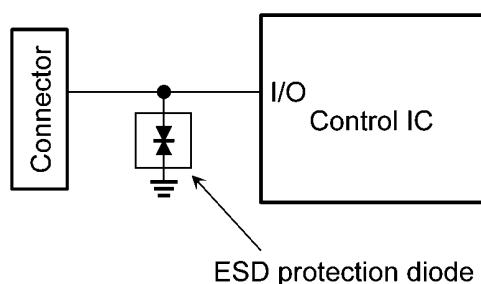
Desktop PCs

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

## 3. Features

- (1) Suitable for high working voltage line. ( $V_{RWM} \leq 18.5 \text{ V}$ )
- (2) Protects devices with its high ESD performance.  
( $V_{ESD} = \pm 15 \text{ kV (Contact / Air) @ IEC61000-4-2}$ )
- (3) Low dynamic resistance protects semiconductor devices from static electricity and noise.  
( $R_{DYN} = 0.2 \Omega$  (typ.))
- (4) Snapback characteristics realizing low clamping voltage protects semiconductor devices.  
( $V_C = 26 \text{ V @ } I_{PP} = 0.5 \text{ A}$  (typ.))
- (5) Compact package is suitable for use in high density board layouts such as in mobile devices.  
(0.62 mm × 0.32 mm size (Toshiba package name: SL2))

## 4. Example of Circuit Diagram



Start of commercial production  
2016-09

### 5. Quick Reference Data

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	$V_{RWM}$	(Note 1)	—	—	—	18.5	V
Total capacitance	$C_t$		$V_R = 0\text{ V}, f = 1\text{ MHz}$	—	0.2	0.5	pF
Dynamic resistance	$R_{DYN}$	(Note 2)	—	—	0.2	—	$\Omega$
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	$V_{ESD}$	(Note 3)	—	—	—	15	kV

Note 1: Recommended operating condition.

Note 2: TLP parameters:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristics between  $I_{PP1} = 8\text{ A}$  and  $I_{PP2} = 16\text{ A}$ .

Note 3: Criterion: No damage to devices.

#### 5.1. ESD Clamp Waveform (Note)

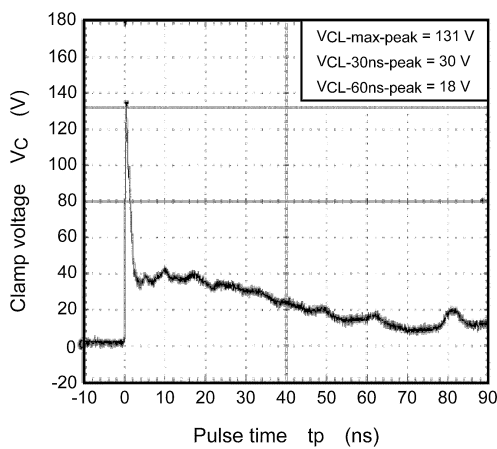


Fig. 5.1.1 +8 kV

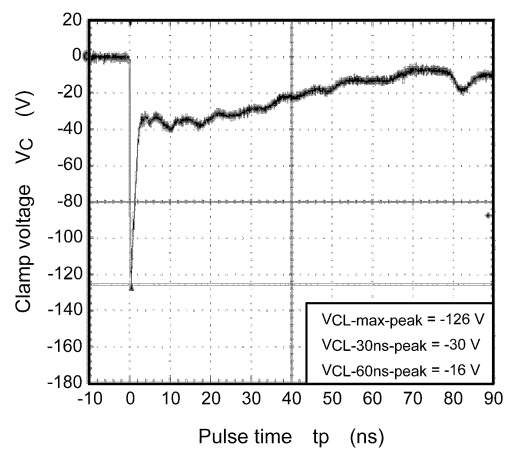


Fig. 5.1.2 -8 kV

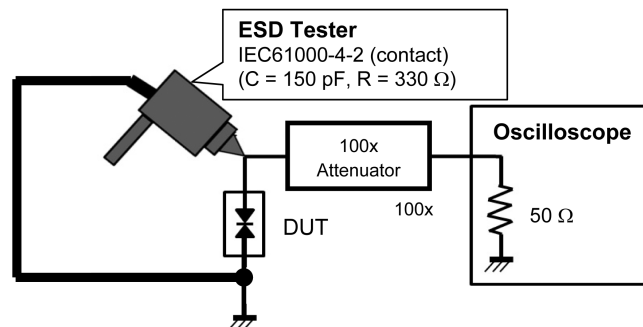
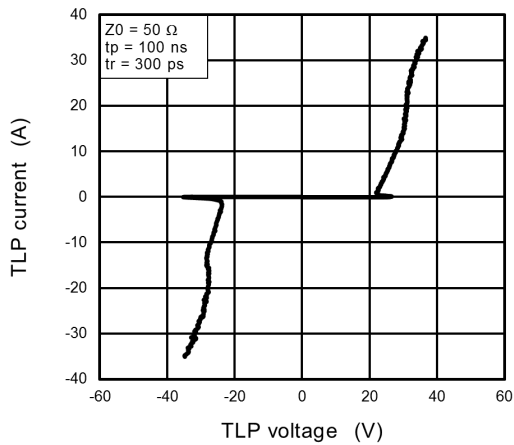


Fig. 5.1.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 5.2. TLP Characteristics (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 5.3. Clamp Voltage - Peak Pulse Current ( $V_C - I_{PP}$ ) (Note)

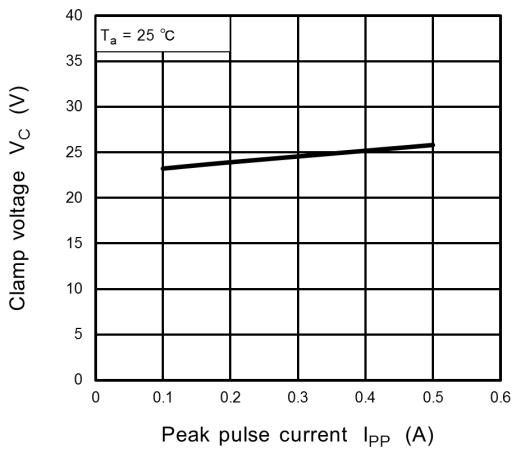


Fig. 5.3.1  $V_C - I_{PP}$

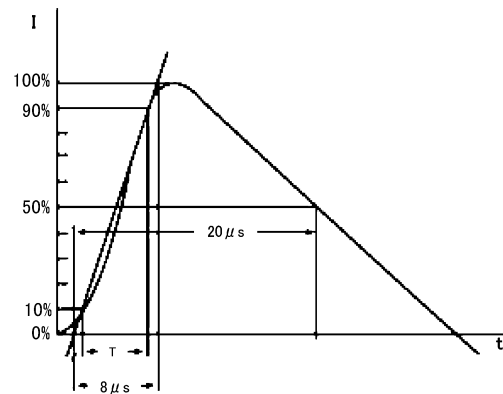


Fig. 5.3.2 Based on IEC61000-4-5 8/20  $\mu\text{s}$  pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 6. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	$V_{ESD}$	(Note 1)	$\pm 15$	kV
Electrostatic discharge voltage (IEC61000-4-2) (Air)			$\pm 15$	kV
Peak pulse power ( $t_p = 8/20\ \mu\text{s}$ )	$P_{PK}$		15	W
Peak pulse current ( $t_p = 8/20\ \mu\text{s}$ )	$I_{PP}$	(Note 2)	0.5	A
Junction temperature	$T_j$		150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to IEC61000-4-5.

### 7. Electrical Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

$V_{RWM}$ : Working peak reverse voltage  
 $V_{BR}$ : Reverse breakdown voltage  
 $I_{BR}$ : Reverse breakdown current  
 $I_R$ : Reverse current  
 $V_C$ : Clamp voltage  
 $I_{PP}$ : Peak pulse current  
 $R_{DYN}$ : Dynamic resistance

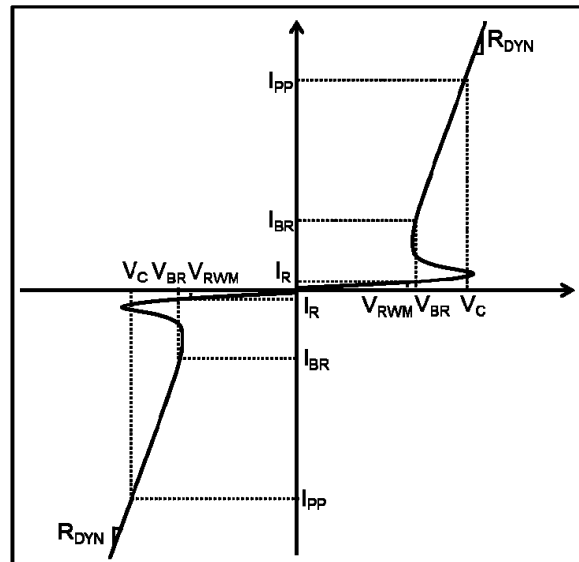


Fig. 7.1 Definitions of Electrical Characteristics

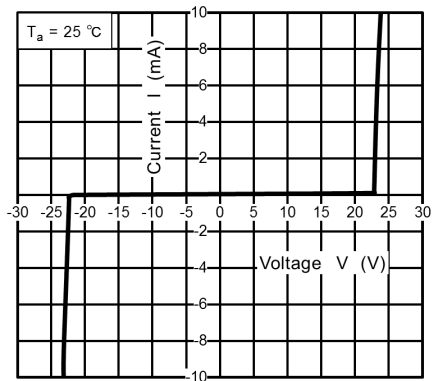
Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	$V_{RWM}$	(Note 1)	—	—	—	18.5	V
Total capacitance	$C_t$		$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$	—	0.2	0.5	pF
Dynamic resistance	$R_{DYN}$	(Note 2)	—	—	0.2	—	$\Omega$
Reverse breakdown voltage	$V_{BR}$		$I_{BR} = 1\text{ mA}$	19.5	22.5	26	V
Reverse current	$I_R$		$V_{RWM} = 18.5\text{ V}$	—	—	100	nA
Clamp voltage	$V_C$	(Note 3)	$I_{PP} = 0.5\text{ A}$	—	26	30	V
		(Note 2)	$I_{TLP} = 8\text{ A}$	—	26	—	
		(Note 2)	$I_{TLP} = 16\text{ A}$	—	27.6	—	

Note 1: Recommended operating condition.

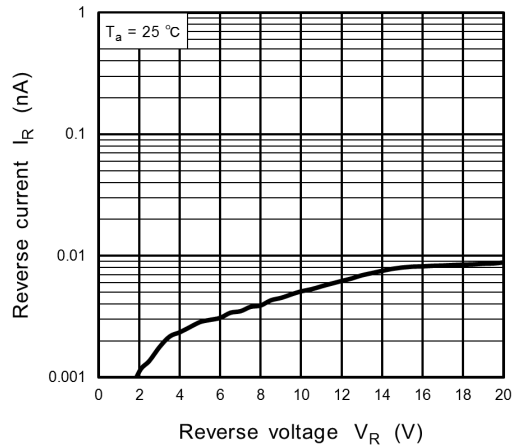
Note 2: TLP parameters:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristics between  $I_{PP1} = 8\text{ A}$  and  $I_{PP2} = 16\text{ A}$ .

Note 3: Based on IEC61000-4-5 8/20  $\mu\text{s}$  pulse.

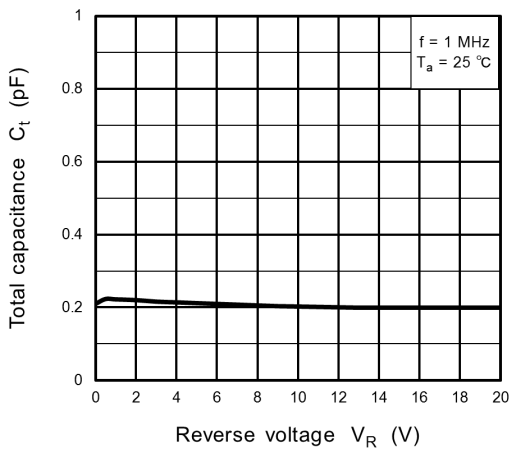
## 8. Characteristics Curves (Note)



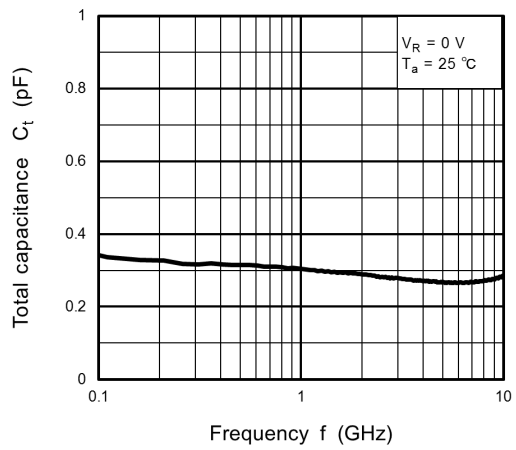
**Fig. 8.1 I - V**



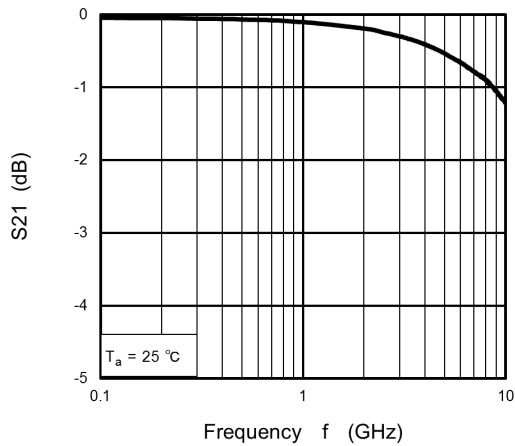
**Fig. 8.2  $I_R - V_R$**



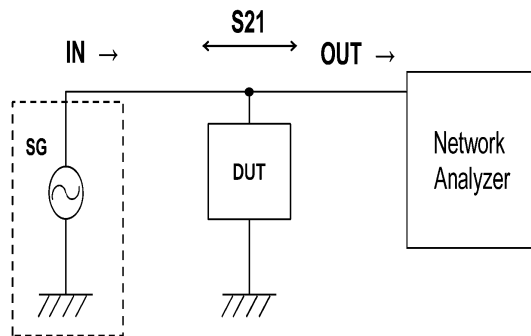
**Fig. 8.3  $C_t - V_R$**



**Fig. 8.4  $C_t - f$**

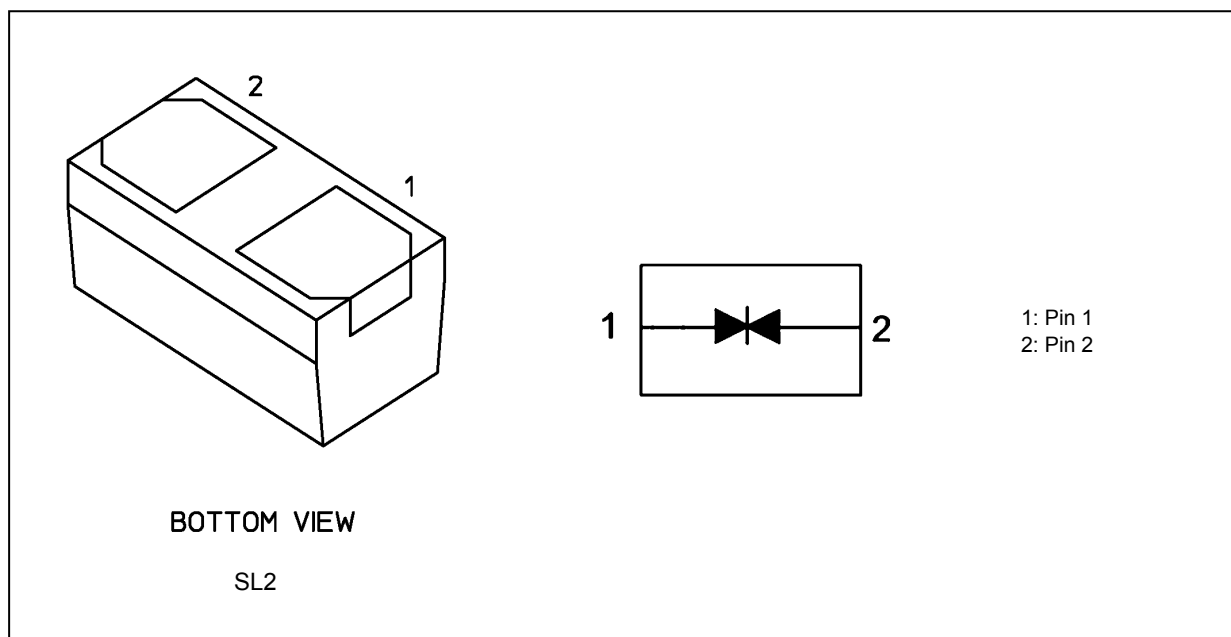


**Fig. 8.5  $S_{21} - f$**



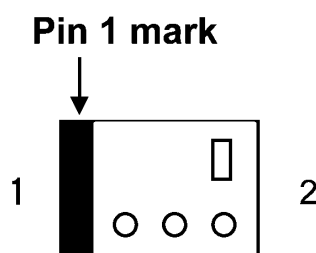
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 9. Packaging and Internal Circuit (Note)

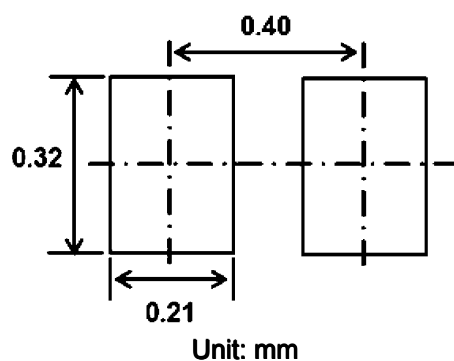


Note: Connect Pin 2 to GND when using Pin 1 for I/O.  
Connect Pin 1 to GND when using Pin 2 for I/O.

## 10. Marking (Top view)

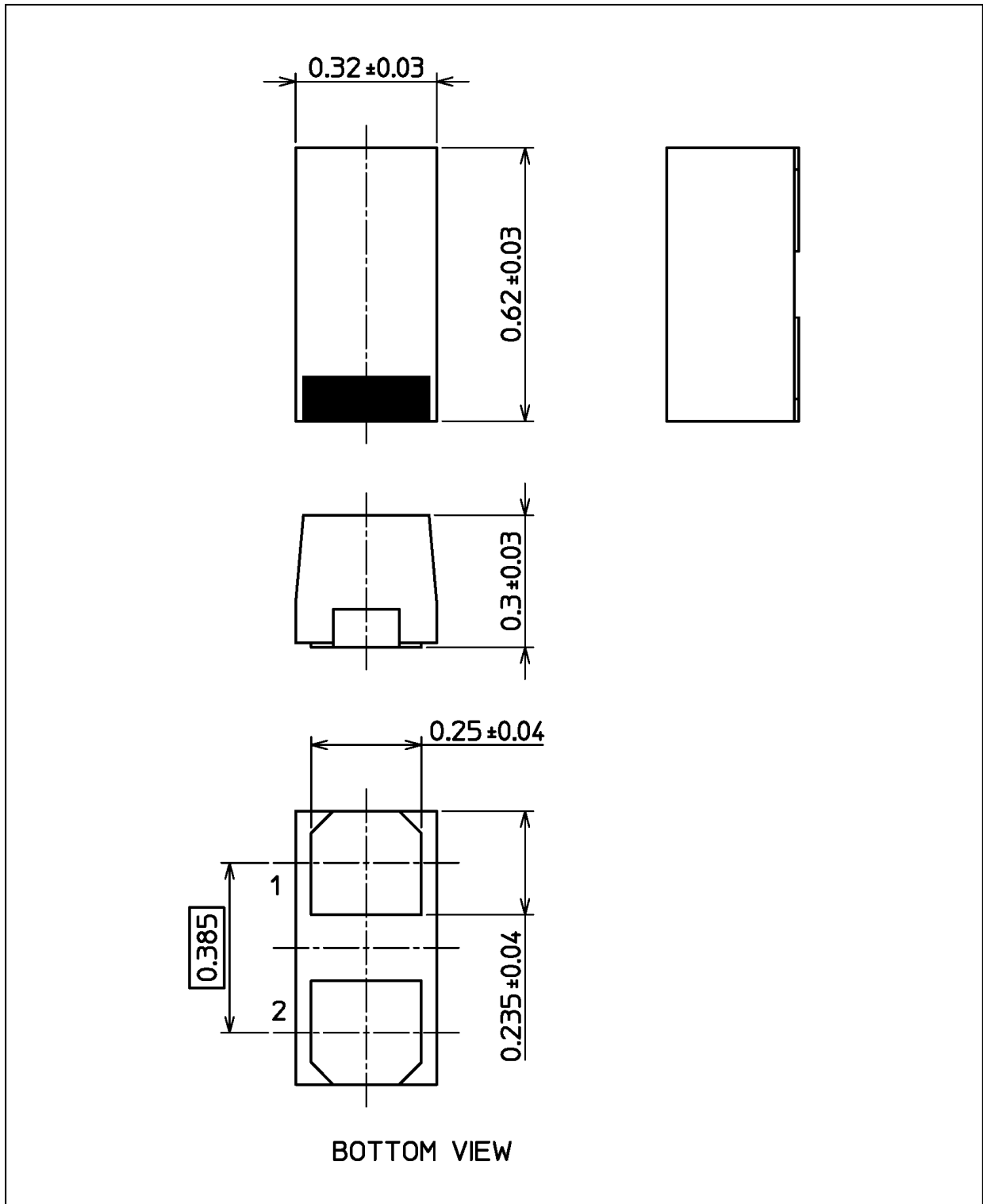


## 11. Land Pattern Dimensions (for reference only)



## Package Dimensions

Unit: mm



Weight: 0.2 mg (typ.)

Package Name(s)
Nickname: SL2

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