

ESD Protection Diodes Silicon Epitaxial Planar

DF2S14P2CTC

General

The DF2S14P2CTC is a TVS diode (ESD protection diode) protects semiconductor devices used in mobile device interfaces and other applications to protect against static electricity and noise.

The DF2S14P2CTC has realized high I_{PP}, in order to protect a semiconductor devices from the indirect lightning stroke and the transition voltage (at the time of power activation).

Furthermore, the DF2S14P2CTC is housed in an ultra-compact package (1.6 mm \times 0.8 mm) to meet applications that require a small footprint.

2. Applications

Mobile Equipment

- · Smartphones
- · Tablets
- · Notebook PCs

Desktop PCs

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

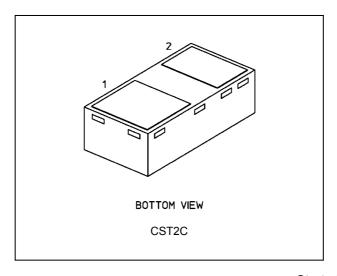
3. Features

- (1) Suitable for use with a 12 V signal line. ($V_{RWM} \le 12.6 \text{ V}$)
- (2) Protects devices with its high ESD performance.

 $(\ensuremath{\mathrm{V_{ESD}}} = \pm 30~\ensuremath{\mathrm{kV}}$ (Contact / Air) @IEC61000-4-2)

- (3) Low dynamic resistance protects semiconductor devices from static electricity and noise. $(R_{DYN} = 0.08 \Omega \text{ (typ.)})$
- (4) Snapback characteristics realizing low clamping voltage protects semiconductor devices. $(V_C = 28 \text{ V@I}_{PP} = 50 \text{ A (typ.)})$
- (5) Compact package is suitable for use in high density board layouts such as in mobile devices. $(1.6 \text{ mm} \times 0.8 \text{ mm} \text{ size} \text{ (Nickname: CST2C))}$

4. Packaging

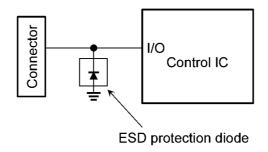


Start of commercial production

2017-07



5. Example of Circuit Diagram

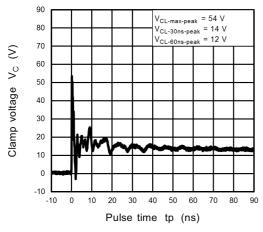


6. Quick Reference Data

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	_	_	_	12.6	V
Dynamic resistance	R_{DYN}	(Note 2)	_	_	0.08	_	Ω
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V _{ESD}	(Note 3)	_		-	30	kV

- Note 1: Recommended operating condition.
- Note 2: TLP parameters: $Z0 = 50 \Omega$, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 16$ A and $I_{PP2} = 30$ A.
- Note 3: Criterion: No damage to devices.

6.1. ESD Clamp Waveform (Note)





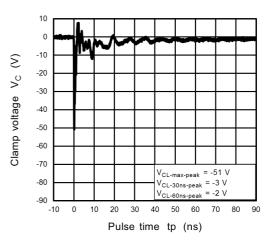


Fig. 6.1.2 -8 kV

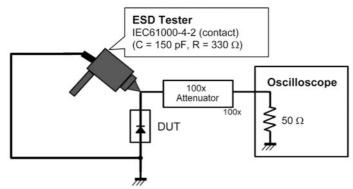
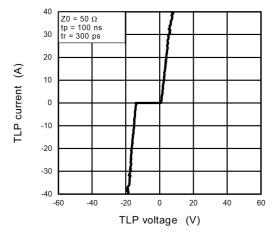


Fig. 6.1.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

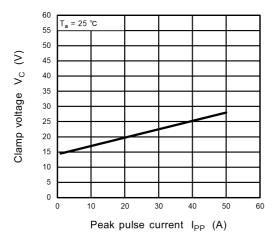


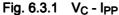
6.2. TLP Characteristics (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.3. Clamp Voltage - Peak Pulse Current (V_C - I_{PP}) (Note)





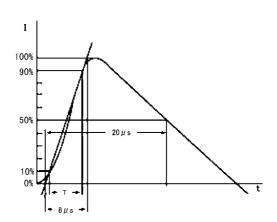


Fig. 6.3.2 Based on IEC61000-4-5 8/20 μs pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V _{ESD}	(Note 1)	±30	kV
Electrostatic discharge voltage (IEC61000-4-2) (Air)			±30	
Peak pulse power (tp = 8/20 μs)	P _{PK}		1600	W
Peak pulse current (tp = 8/20 μs)	I _{PP}	(Note 2)	50	Α
Junction temperature	Tj		150	°C
Storage temperature	T _{stg}		-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to IEC61000-4-5.

8. Electrical Characteristics (Unless otherwise specified, T_a = 25 °C)

 V_{RWM} : Working peak reverse voltage V_{BR} : Reverse breakdown voltage I_{BR} : Reverse breakdown current

I_R: Reverse current
V_C: Clamp voltage
I_{PP}: Peak pulse current
R_{DYN}: Dynamic resistance

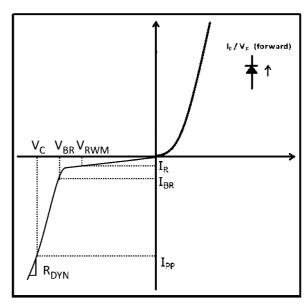


Fig. 8.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	_	_	_	12.6	V
Total capacitance	Ct		V _R = 0 V, f = 1 MHz	_	270	_	pF
Dynamic resistance	R_{DYN}	(Note 2)	_	_	0.08	_	Ω
Reverse breakdown voltage	V_{BR}		I _{BR} = 1 mA	12.9	13.5	15.5	V
Reverse current	I _R		V _{RWM} = 12.6 V	_	_	0.1	μΑ
Clamp voltage	V _C	(Note 3)	I _{PP} = 1 A	_	14.5	_	V
			I _{PP} = 50 A	_	28	32	
		(Note 2)	I _{TLP} = 16 A	_	15.5	_	V
			I _{TLP} = 30 A	_	17	_	

Note 1: Recommended operating condition.

Note 2: TLP parameters: $Z0 = 50 \Omega$, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 16$ A and $I_{PP2} = 30$ A.

Note 3: Based on IEC61000-4-5 $8/20 \mu s$ pulse.

2018-12-06



9. Characteristics Curves (Note)

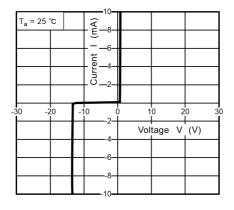


Fig. 9.1 I - V

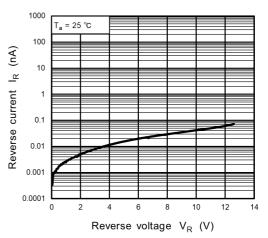


Fig. 9.2 I_R - V_R

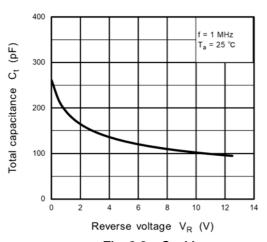
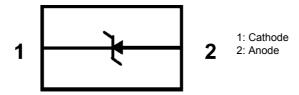


Fig. 9.3 $C_t - V_R$

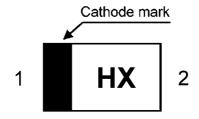
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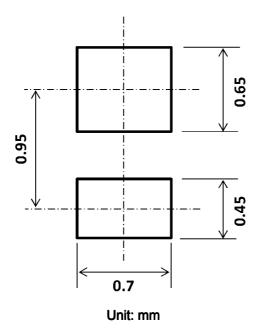
10. Internal Circuit



11. Marking (Top view)



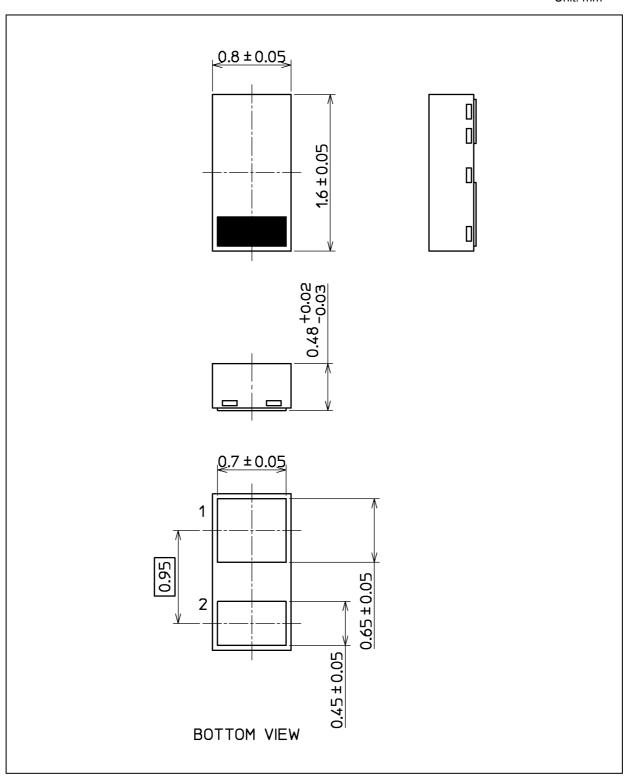
12. Land Pattern Dimensions (for reference only)





Package Dimensions

Unit: mm



Weight: 1.5 mg (typ.)

	Package Name(s)
Nickname: CST2C	

Rev.3.0



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