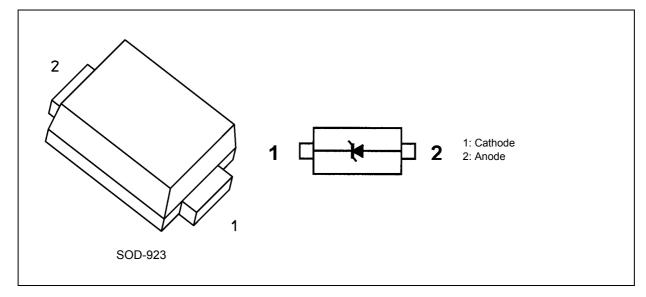
ESD Protection Diodes Silicon Epitaxial Planar

DF2S6.8MFS

1. Applications

- ESD Protection
- Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

2. Packaging and Internal Circuit



3. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^{\circ}$ C)

Characteristics	Symbol	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V _{ESD}	±12	kV
Electrostatic discharge voltage(IEC61000-4-2)(Air)	V _{ESD}	±15	kV
Peak pulse power	P _{PK}	45	W
Peak pulse current	I _{PP}	3	А
Junction temperature	Tj	150	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

4. Electrical Characteristics (Unless otherwise specified, $T_a = 25^{\circ}C$)

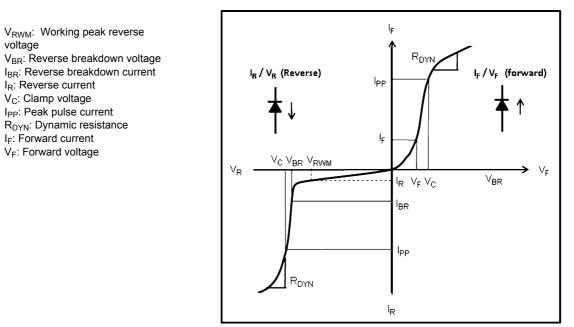


Fig. 4.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V _{RWM}		_	_	_	5.0	V
Reverse breakdown voltage	V _{BR}		I _{BR} = 5 mA	6.0			V
Reverse current	I _R		V _{RWM} = 5 V			0.5	μA
Clamp voltage	V _C	(Note 1)	I _{PP} = 1 A		9.5	_	V
			I _{PP} = 3 A	_	12	15	
Clamp voltage	V _C	(Note 2)	I _{TLP} = 16 A	_	14.5	_	
			I _{TLP} = 25 A	_	17.7	_	
Dynamic resistance	R _{DYN}	(Note 2)	_		0.35		Ω
Total capacitance	Ct	(Note 3)	V _R = 0 V, f = 1 MHz		0.45	0.9	pF

Note 1: Based on IEC61000-4-5 8/20 μs pulse.

Note 2: TLP parameter: Z0 = 50 Ω , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns,

extraction of dynamic resistance using a least-squares fit of TLP characteristics at I_{PP} between 8 A to 16 A. Note 3: Guaranteed by design.

5. Marking

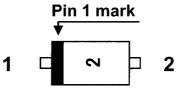


Fig. 5.1 Marking

6. Land Pattern Dimensions (for reference only)

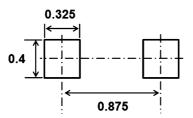


Fig. 6.1 Land Pattern Dimensions (Unit: mm)

7. Characteristics Curves (Note)

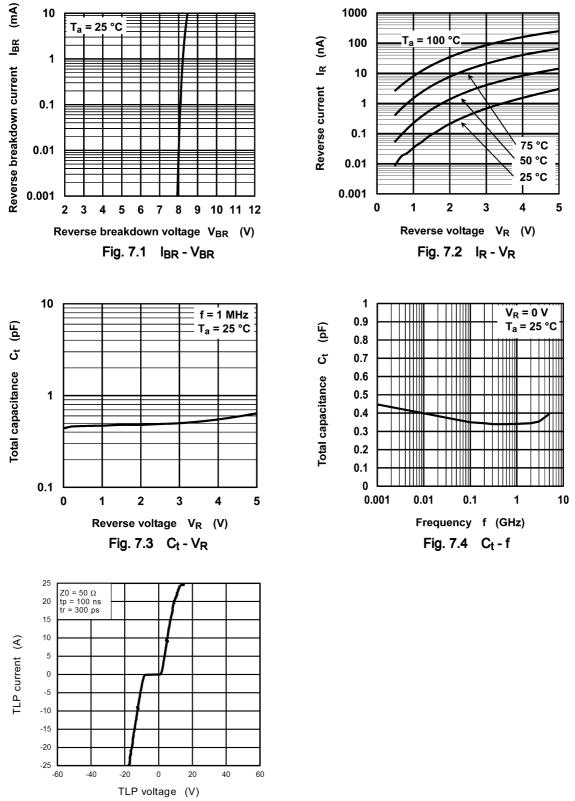
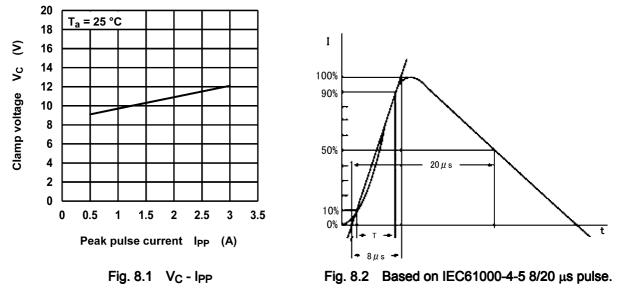


Fig. 7.5 TLP

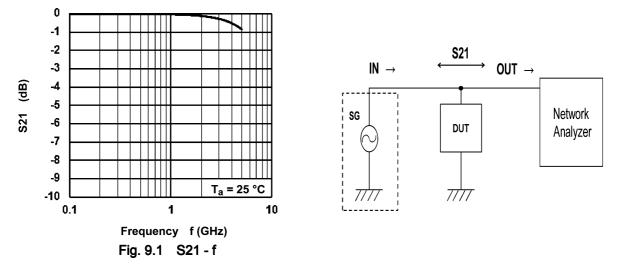
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

8. Clamp Voltage - Peak Pulse Current (V_C - I_{PP}) (Note)



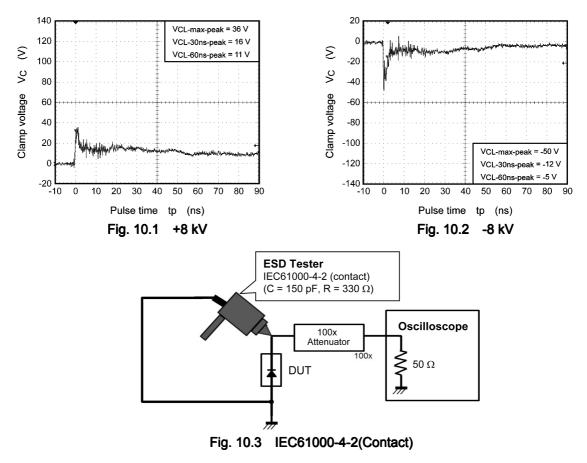
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

9. Insertion Loss (S21) (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

10. ESD Clamp Waveform (Note)

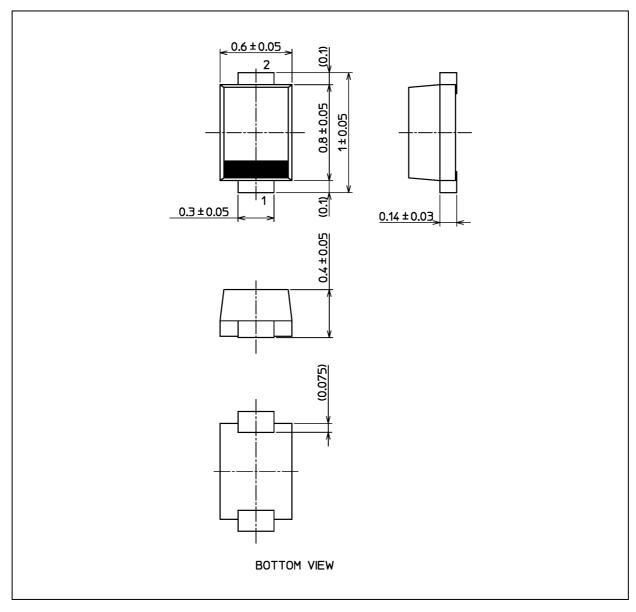


Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.55 mg (typ.)

Package Name(s)

Nickname: SOD-923

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