

TOSHIBA Diode Silicon Epitaxial Planar Type

HN1D01FE

Ultra High Speed Switching Application

- HN1D02FU is composed of 2 unit of cathode common.
- Low forward voltage : $V_F(3) = 0.92V$ (typ.)
- Fast reverse recovery time : $t_{rr} = 1.6ns$ (typ.)
- Small total capacitance : $C_T = 2.2pF$ (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	300*	mA
Average forward current	I_O	100*	mA
Surge current (10ms)	I_{FSM}	2*	A
Power dissipation	P	100**	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

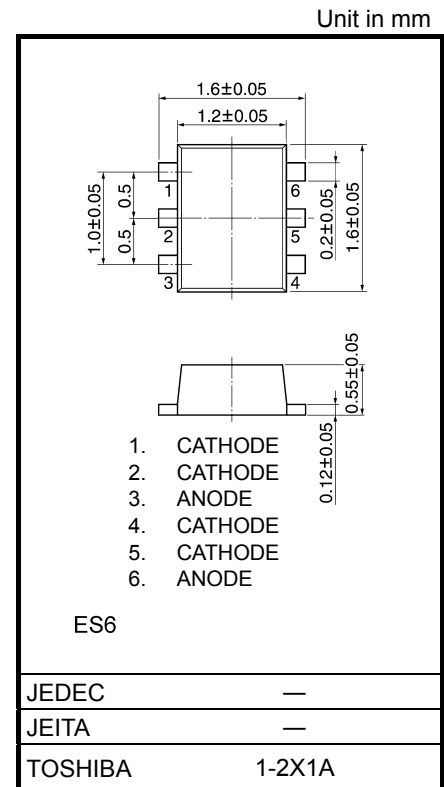
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

*: These are the Absolute Maximum Ratings for a single diode (Q1, Q2, Q3 or Q4).

Where Unit 1 and Unit 2 are used independently or simultaneously, the Absolute Maximum Ratings per diode are 75% of those for a single diode.

** : Total rating.



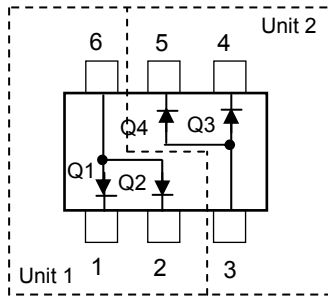
Weight: 0.003g (typ.)

Electrical Characteristics (Q1, Q2, Q3, Q4 Common; Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 1mA$	—	0.61	—	V
	$V_F(2)$	—	$I_F = 10mA$	—	0.74	—	
	$V_F(3)$	—	$I_F = 100mA$	—	0.92	1.20	
Reverse current	$I_R(1)$	—	$V_R = 30V$	—	—	0.1	μA
	$I_R(2)$	—	$V_R = 80V$	—	—	0.5	
Total capacitance	C_T	—	$V_R = 0, f = 1MHz$	—	2.2	—	pF
Reverse recovery time	t_{rr}	—	$I_F = 10mA$ (fig.1)	—	1.6	—	ns

Start of commercial production
2002-04

Pin Assignment (Top View)



Marking

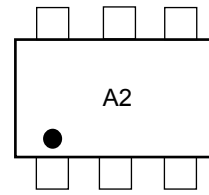
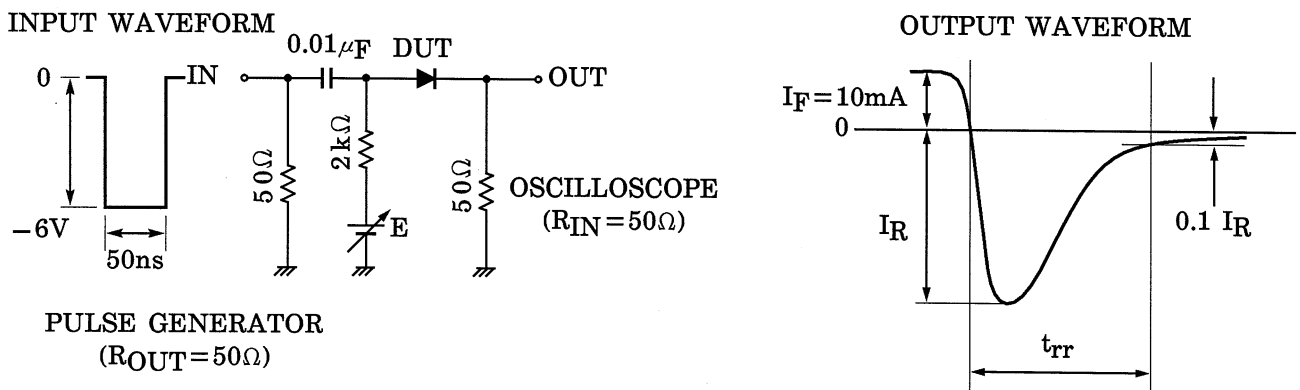
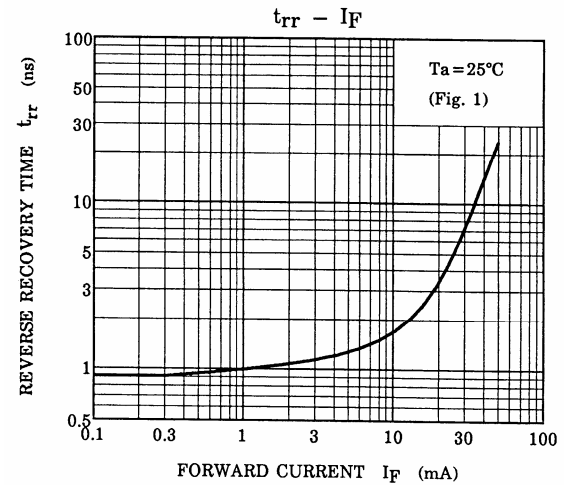
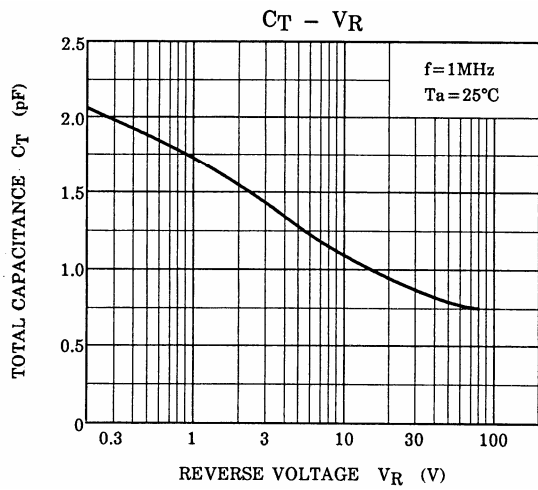
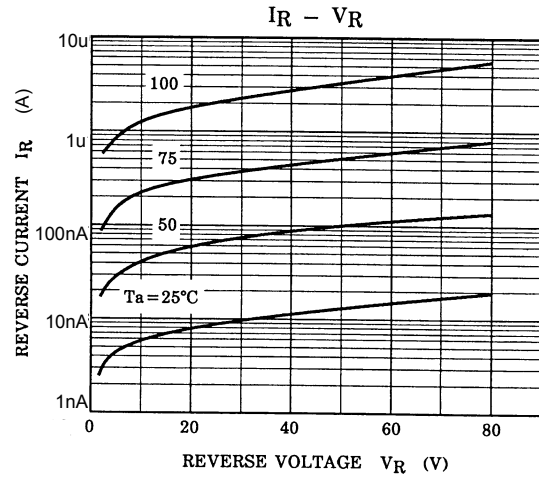
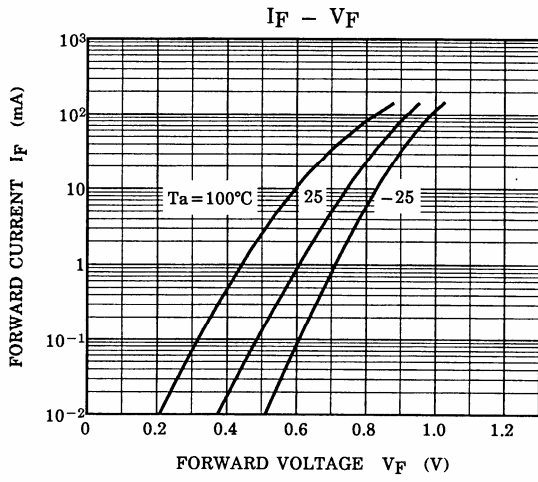


Fig. 1 Reverse Recovery Time (t_{rr}) Test Circuit





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