TOSHIBA Diode Silicon Epitaxial Planar Type

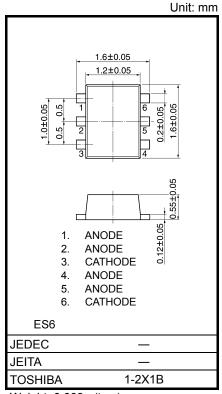
HN1D02FE

Ultra High Speed Switching Application

- The HN1D02FU is composed of 2 common cathode units.
- Low forward voltage $: V_{F(3)} = 0.90V (typ.)$
- Fast reverse recovery time : t_{rr} = 1.6ns (typ.)
- Small total capacitance : C_T = 0.9pF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Maximum (peak) reverse voltage	V _{RM}	85	V	
Reverse voltage	V _R	80	V	
Maximum (peak) forward current	I _{FM}	300*	mA	
Average forward current	Ι _Ο	100*	mA	
Surge current (10ms)	I _{FSM}	2*	А	
Power dissipation	Р	100**	mW	
Junction temperature	Tj	150	°C	
Storage temperature	T _{stg}	–55 to 150	°C	



Weight: 0.003g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the

reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- *: These are the Absolute Maximum Ratings for a single diode (Q1, Q2, Q3 or Q4). Where Unit 1 and Unit 2 are used independently or simultaneously, the Absolute Maximum Ratings per diode are 75% of those for a single diode.
- **: Total rating.

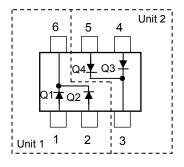
Electrical Characteristics (Q1, Q2, Q3, Q4 Common; Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Forward voltage	V _{F (1)}	_	I _F = 1mA		0.60	—	V
	V _{F (2)}	-	I _F = 10mA		0.72	—	
	V _{F (3)}	_	I _F = 100mA	-	0.90	1.20	
Reverse current	I _{R (1)}	_	V _R = 30V	_	_	0.1	μA
	I _{R (2)}	_	V _R = 80V	-	_	0.5	
Total capacitance	CT	_	V _R = 0, f = 1MHz	_	0.9	_	pF
Reverse recovery time	t _{rr}	—	I _F = 10mA (fig.1)	_	1.6	_	ns

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Pin Assignment (Top View)

Marking



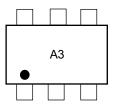
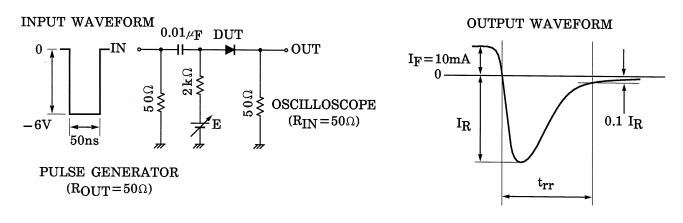
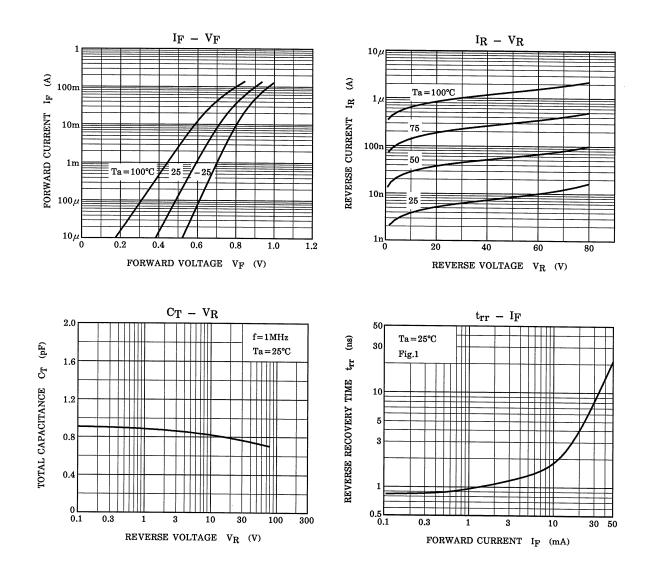


Fig. 1 Reverse Recovery Time (trr) Test Circuit



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