

TOSHIBA Diode Silicon Epitaxial Planar Type

# HN1D04FU

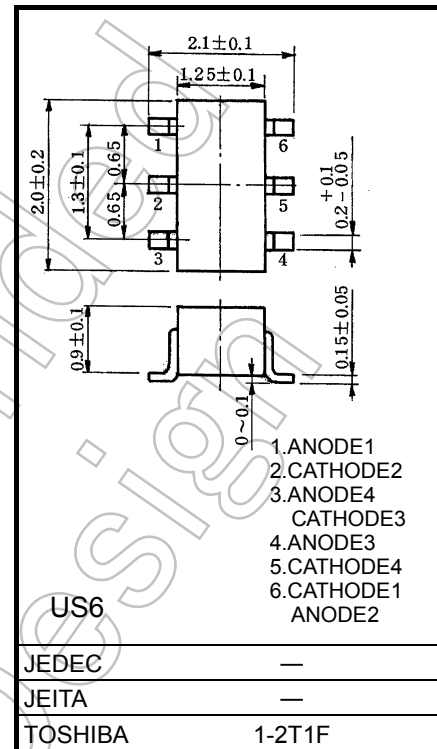
## Ultra High Speed Switching Application

Unit: mm

- Low forward voltage :  $V_{F(3)} = 0.90V$  (typ.)
- Fast reverse recovery time :  $t_{rr} = 1.6ns$  (typ.)
- Small total capacitance :  $C_T = 0.9pF$  (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	85	V
Reverse voltage	$V_R$	80	V
Maximum (peak) forward current	$I_{FM}$	300*	mA
Average forward current	$I_O$	100*	mA
Surge current (10ms)	$I_{FSM}$	2*	A
Power dissipation	P	200**	mW
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-55 to 150	°C



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

\*: Where Q1 and Q2 or Q3 and Q4 are used independently or simultaneously, the Absolute Maximum Ratings per diode are 50% of those of the single diode.

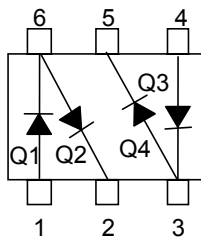
\*\* : Total rating

## Electrical Characteristics (Q1, Q2, Q3, Q4 Common; Ta = 25°C)

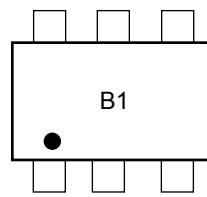
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 1mA$	—	0.60	—	V
	$V_F(2)$	—	$I_F = 10mA$	—	0.75	—	
	$V_F(3)$	—	$I_F = 100mA$	—	0.90	1.20	
Reverse current	$I_R(1)$	—	$V_R = 30V$	—	—	0.1	μA
	$I_R(2)$	—	$V_R = 80V$	—	—	0.5	
Total capacitance	$C_T$	—	$V_R = 0, f = 1MHz$	—	0.9	—	pF
Reverse recovery time	$t_{rr}$	—	$I_F = 10mA$ (fig.1)	—	1.6	—	ns

Start of commercial production  
2000-12

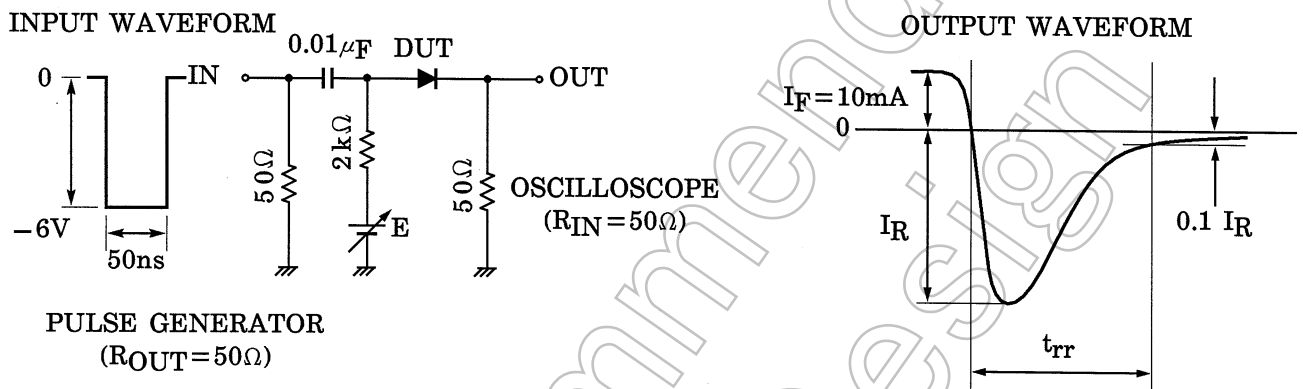
**Pin Assignment (Top View)**



**Marking**

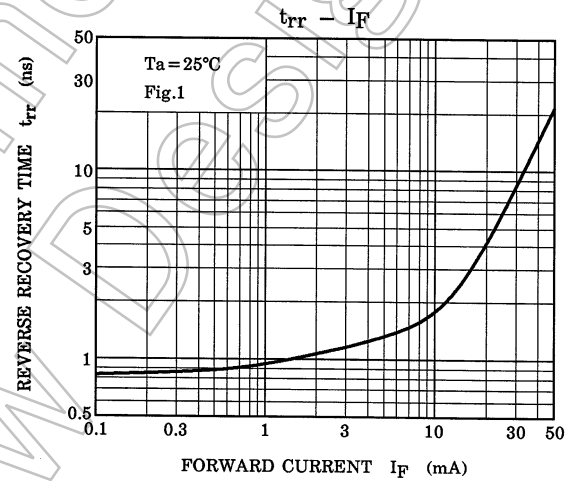
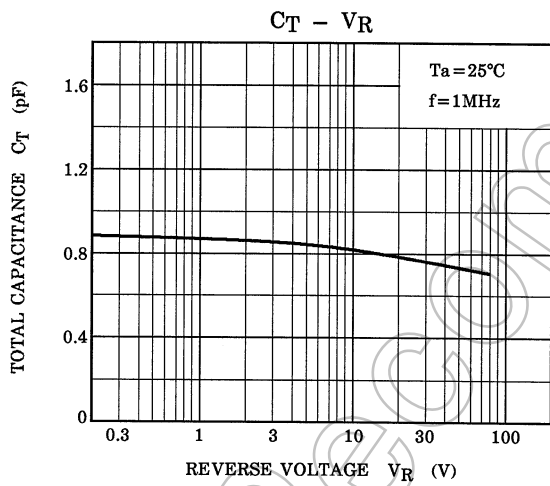
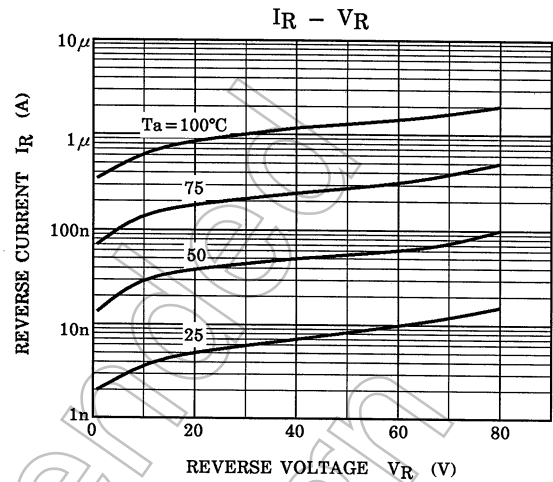
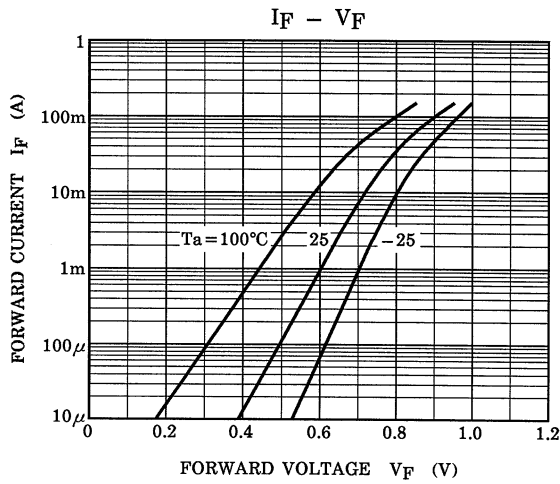


**Fig. 1 Reverse Recovery Time ( $t_{rr}$ ) Test Circuit**



Not Recommended for New Design

Q1, Q2, Q3, Q4 Common



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