TOSHIBA Transistor Silicon PNP/NPN Epitaxial Type (PCT Process) (Transistor with Built-in Bias Resistor)

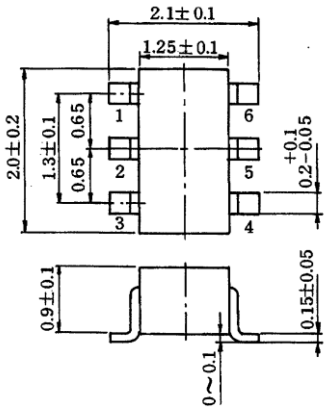
RN4903

Switching, Inverter Circuit, Interface Circuit and Driver Circuit

- AEC-Q101 Qualified (Note1)
- Including two devices in US6 (ultra super mini type with 6 leads)
- With built-in bias resistors
- Simplify circuit design
- Reduce a quantity of parts and manufacturing process and miniaturize equipment.

Note1: For detail information, please contact our sales representative.

Unit: mm



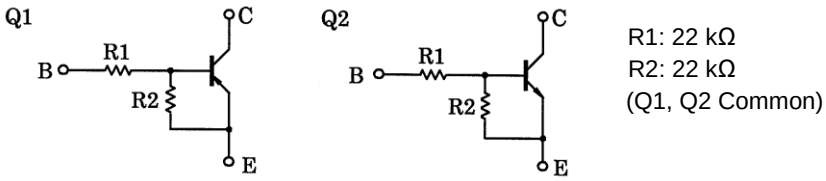
1. EMITTER 1 (E1)
2. BASE 1 (B1)
3. COLLECTOR 2 (C2)
4. EMITTER 2 (E2)
5. BASE 2 (B2)
6. COLLECTOR 1 (C1)

US6

JEDEC	—
JEITA	—
TOSHIBA	2-2J1A

Weight: 6.8mg (typ.)

Equivalent Circuit and Bias Resister Values



R1: 22 kΩ
R2: 22 kΩ
(Q1, Q2 Common)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	−50	V
Collector-emitter voltage	V_{CEO}	−50	V
Emitter-base voltage	V_{EBO}	−10	V
Collector current	I_C	−100	mA

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	50	V
Collector-emitter voltage	V_{CEO}	50	V
Emitter-base voltage	V_{EBO}	10	V
Collector current	I_C	100	mA

Start of commercial production
1990-10

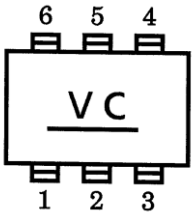
Q1, Q2 Common Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Collector power dissipation	P_C *	200	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

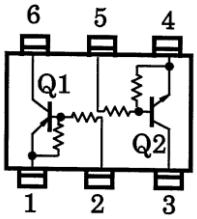
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

* Total rating

Marking



Equivalent Circuit (Top View)



Q1 Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I_{CBO}	V_{CB} = −50V, I_E = 0 mA	—	—	−100	nA
	I_{CEO}	V_{CE} = −50V, I_B = 0 mA	—	—	−500	
Emitter cut-off current	I_{EBO}	V_{EB} = −10V, I_C = 0 mA	−0.17	—	−0.33	mA
DC current gain	h_{FE}	V_{CE} = −5V, I_C = −10mA	70	—	—	—
Collector-emitter saturation voltage	$V_{CE\ (sat)}$	I_C = −5mA, I_B = −0.25mA	—	−0.1	−0.3	V
Input voltage (ON)	$V_{I\ (ON)}$	V_{CE} = −0.2V, I_C = −5mA	−1.3	—	−3.0	V
Input voltage (OFF)	$V_{I\ (OFF)}$	V_{CE} = −5V, I_C = −0.1mA	−1.0	—	−1.5	V
Transition frequency	f_T	V_{CE} = −10V, I_C = −5mA	—	200	—	MHz
Collector output capacitance	C_{ob}	V_{CB} = −10V, I_E = 0 mA, f = 1MHz	—	3	6	pF

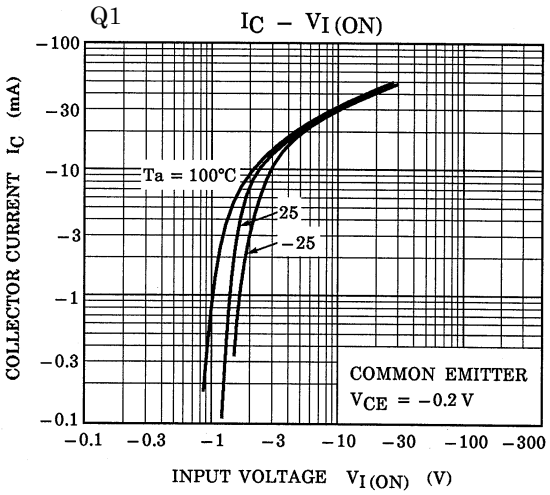
Q2 Electrical Characteristics (Ta = 25°C)

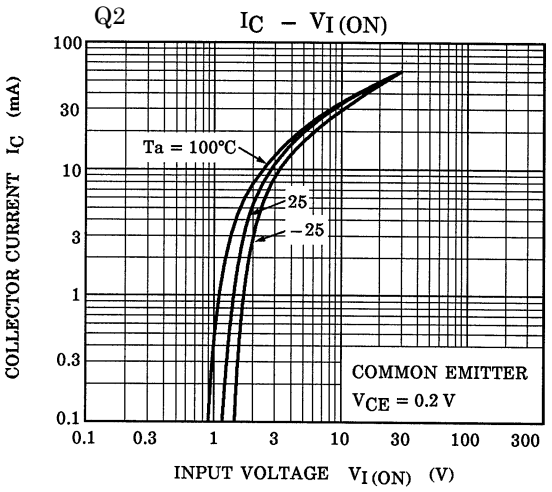
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I_{CBO}	V_{CB} = 50 V, I_E = 0 mA	—	—	100	nA
	I_{CEO}	V_{CE} = 50 V, I_B = 0 mA	—	—	500	
Emitter cut-off current	I_{EBO}	V_{EB} = 10 V, I_C = 0 mA	0.17	—	0.33	mA
DC current gain	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	70	—	—	—
Collector-emitter saturation voltage	$V_{CE\ (sat)}$	I_C = 5 mA, I_B = 0.25 mA	—	0.1	0.3	V
Input voltage (ON)	$V_{I\ (ON)}$	V_{CE} = 0.2 V, I_C = 5 mA	1.3	—	3.0	V
Input voltage (OFF)	$V_{I\ (OFF)}$	V_{CE} = 5 V, I_C = 0.1 mA	1.0	—	1.5	V
Transition frequency	f_T	V_{CE} = 10 V, I_C = 5 mA	—	250	—	MHz
Collector output capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0 mA, f = 1 MHz	—	3	6	pF

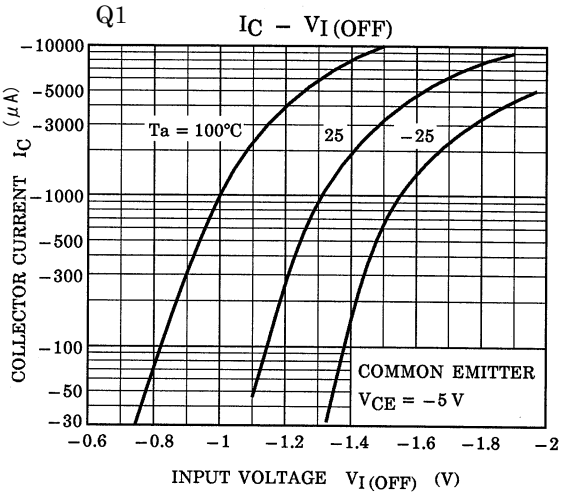
Q1, Q2 Common Electrical Characteristics (Ta = 25°C)

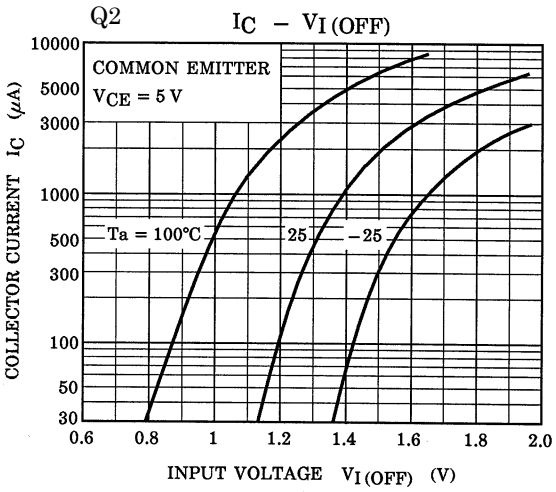
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Input resistor	R1	—	15.4	22	28.6	kΩ
Resistor ratio	R1/R2	—	0.9	1.0	1.1	—

Characteristics Curves



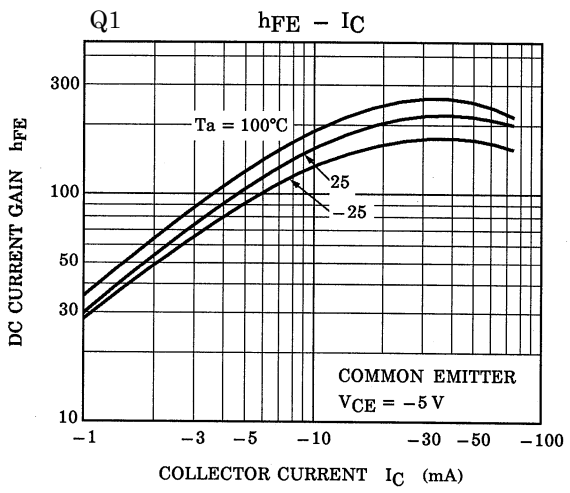


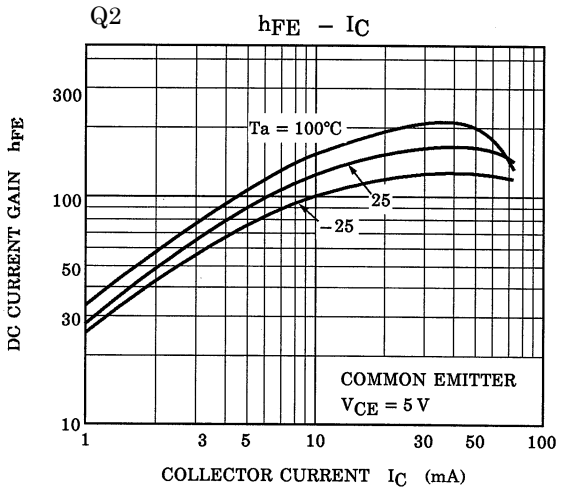


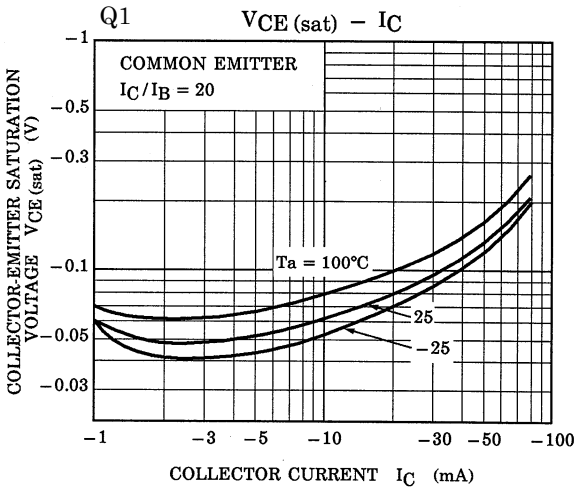


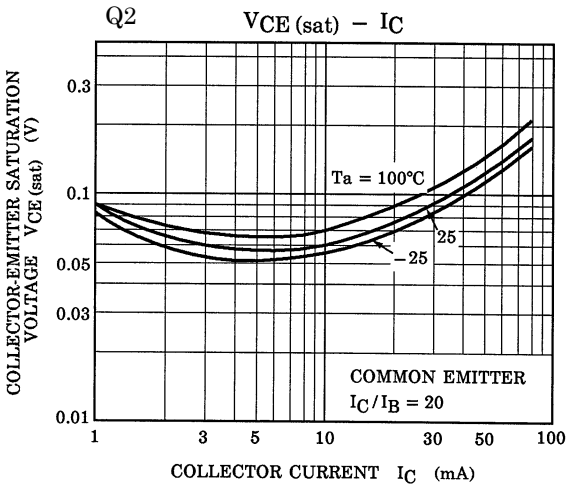
The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Characteristics Curves









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