TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

SSM3J117TU

DC-DC converter Applications

- **High-Speed Switching Applications**
- 4 V drive
- Low ON-resistance: $R_{DS(ON)} = 225 \text{ m}\Omega \text{ (max)} (@V_{GS} = -4 \text{ V})$

 $R_{DS(ON)}$ = 117 m Ω (max) (@V_{GS} = -10 V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		V _{DS}	-30	V	
Gate-source voltage		V _{GSS}	±20	V	
Drain current	DC	I _D	-2	A	
	Pulse	I _{DP}	-4		
Power dissipation		P _{D (Note 1)}	800	mW	
		P _{D (Note 2)}	500		
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

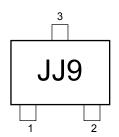
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the

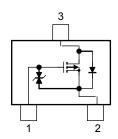
Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: Mounted on a ceramic board. (25.4 mm \times 25.4 mm \times 0.8 t, Cu Pad: 645 mm²)
- Note 2: Mounted on an FR4 board. (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 645 mm²)

Marking

Equivalent Circuit (top view)

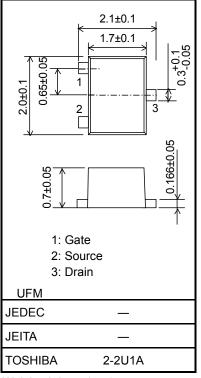




Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Start of commercial production 2005-12



Weight: 6.6 mg (typ.)

Unit: mm

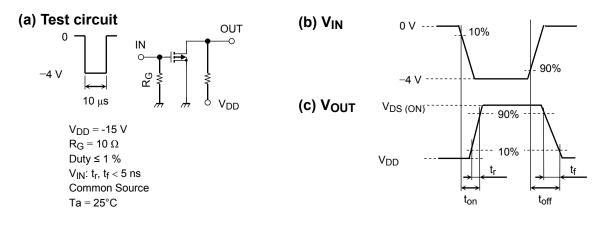
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Electrical Characteristics (Ta = 25°C)

Charac	teristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain-source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	_	_	V
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = +20 \text{ V}$	-15	_	_	
Drain cutoff currer	ıt	I _{DSS}	$V_{DS} = -30 V, V_{GS} = 0 V$	_	_	-1	μA
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	_	_	±1	μA
Gate threshold vol	tage	V _{th}	$V_{DS} = -5 V, I_D = -1 mA$	-1.2	_	-2.6	V
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = -5 V, I_D = -1 A$ (Note 3)	1.6	3.1	_	S
Drain-source ON-resistance		R _{DS (ON)}	$I_D = -1 \text{ A}, V_{GS} = -10 \text{ V}$ (Note 3)		80	117	mΩ
			$I_D = -0.5 \text{ A}, V_{GS} = -4 \text{ V}$ (Note 3)		160	225	
Input capacitance		C _{iss}	$V_{DS} = -15 V$, $V_{GS} = 0 V$, f = 1 MHz	_	280	_	pF
Output capacitanc	e	C _{oss}	$V_{DS} = -15 V$, $V_{GS} = 0 V$, f = 1 MHz	_	80	_	pF
Reverse transfer of	apacitance	C _{rss}	$V_{DS} = -15 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$		45	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -15 \text{ V}, \text{ I}_{D} = -1 \text{ A},$		16	_	ns
	Turn-off time	t _{off}	V_{GS} = 0 to -4 V, R_G = 10 Ω	_	35	—	
Drain-source forw	ard voltage	V _{DSF}	$I_D = 2 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 3)		0.8	1.2	V

Note 3: Pulse test

Switching Time Test Circuit



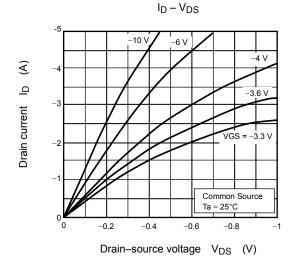
Precaution

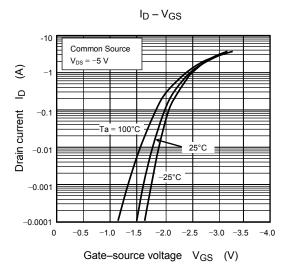
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -1$ mA for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} .

(The relationship can be established as follows: V_{GS (off)} < V_{th} < V_{GS (on)}.)

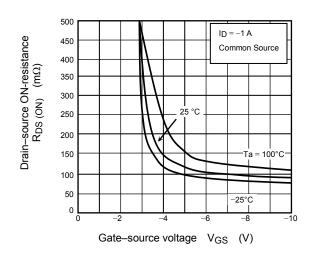
Take this into consideration when using the device.

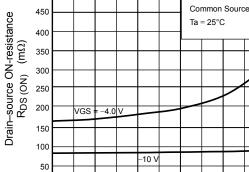
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500

0

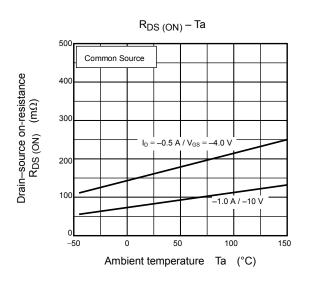
0

-1

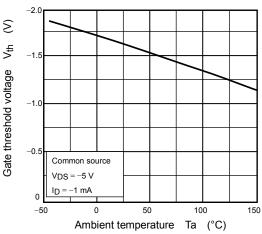


-4

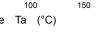
-5



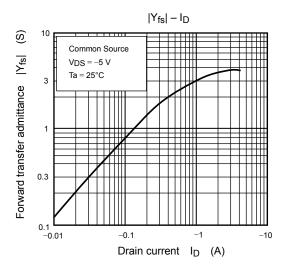
V_{th} – Ta

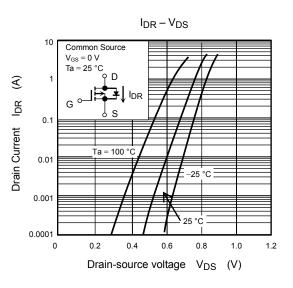


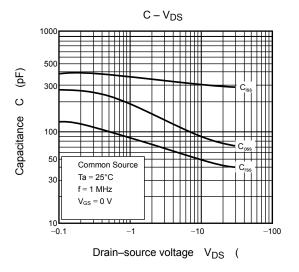
 $R_{DS(ON)} - I_D$

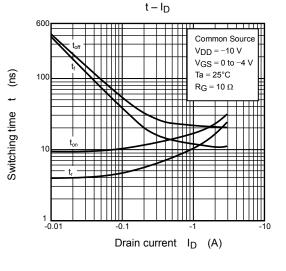


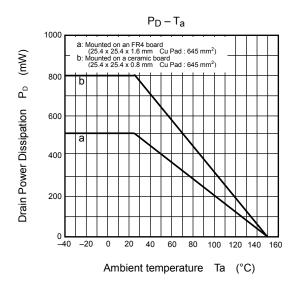
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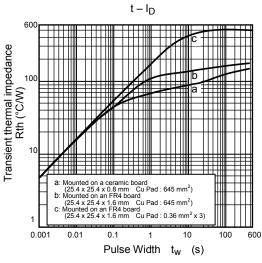












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