

# SSM3K318R

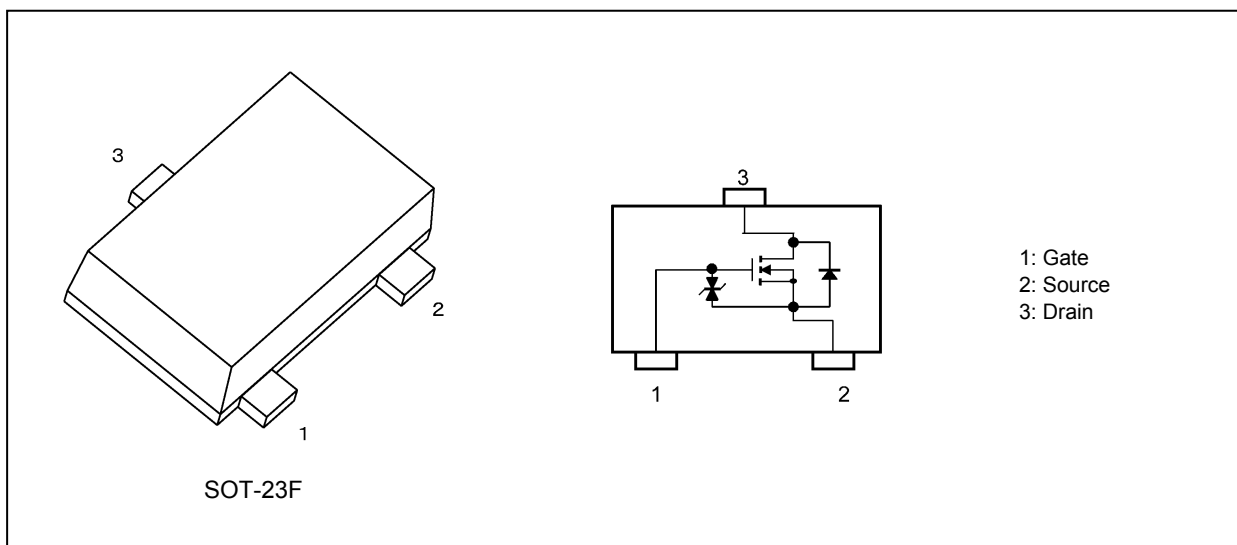
## 1. Applications

- Load Switches
- Ultra-High-Speed Switching

## 2. Features

- (1) 4.5-V gate drive voltage.
- (2) Low drain-source on-resistance  
 $R_{DS(ON)} = 145 \text{ m}\Omega$  (max) (@ $V_{GS} = 4.5 \text{ V}$ )  
 $R_{DS(ON)} = 107 \text{ m}\Omega$  (max) (@ $V_{GS} = 10 \text{ V}$ )

## 3. Packaging and Pin Assignment



Start of commercial production

2015-02

**4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T<sub>a</sub> = 25 °C)**

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V <sub>DSS</sub>	60	V
Gate-source voltage	V <sub>GSS</sub>	±20	
Drain current (Note 1)	I <sub>D</sub>	2.5	A
Drain current (pulsed) (Note 1)	I <sub>DP</sub>	5	
Power dissipation (Note 2)	P <sub>D</sub>	1	W
Power dissipation (t = 10 s) (Note 2)	P <sub>D</sub>	2	
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on an FR4 board. (25.4 mm × 25.4 mm × 1.6 mm ,Cu pad: 645 mm<sup>2</sup>)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, R<sub>th(ch-a)</sub>, and the drain power dissipation, P<sub>D</sub>, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

**5. Electrical Characteristics**

**5.1. Static Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	60	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	35	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = 5\text{ V}, I_D = 1\text{ mA}$	1.8	—	2.8	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 2.0\text{ A}, V_{GS} = 10\text{ V}$	—	83.5	107	$\text{m}\Omega$
		$I_D = 1.0\text{ A}, V_{GS} = 4.5\text{ V}$	—	101	145	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = 5\text{ V}, I_D = 2\text{ A}$	3.7	7.4	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ . Take this into consideration when using the device.

Note 3: Pulse measurement.

**5.2. Dynamic Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	235	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	23	—	
Output capacitance	$C_{oss}$		—	31	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 0\text{ to }4.5\text{ V}, R_G = 10\text{ }\Omega$	—	14	—	ns
Switching time (turn-off time)	$t_{off}$		—	9.5	—	

**5.3. Switching Time Test Circuit**

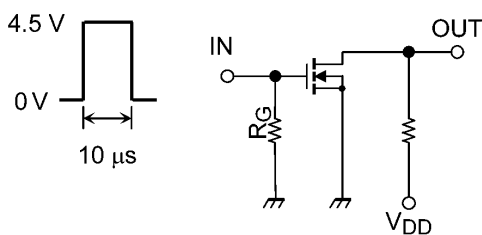


Fig. 5.3.1 Switching Time Test Circuit

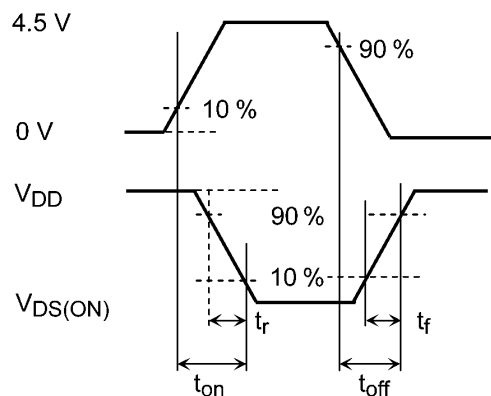


Fig. 5.3.2 Input Waveform/Output Waveform

**5.4. Gate Charge Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 30\text{ V}, I_D = 2.5\text{ A},$ $V_{GS} = 10\text{ V}$	—	7	—	nC
Gate-source charge	$Q_{gs}$		—	4.8	—	
Gate-drain charge	$Q_{gd}$		—	2.2	—	

**5.5. Source-Drain Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = -2.5\text{ A}, V_{GS} = 0\text{ V}$	—	-0.83	-1.2	V

Note 1: Pulse measurement.

**6. Marking**

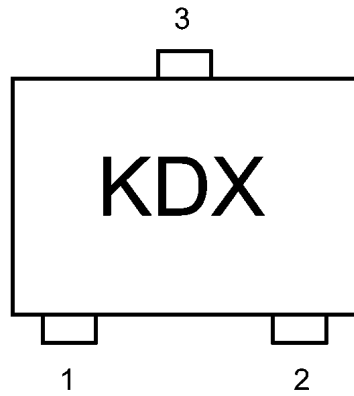
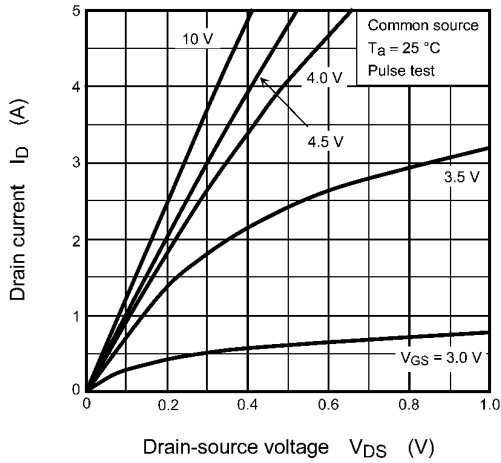
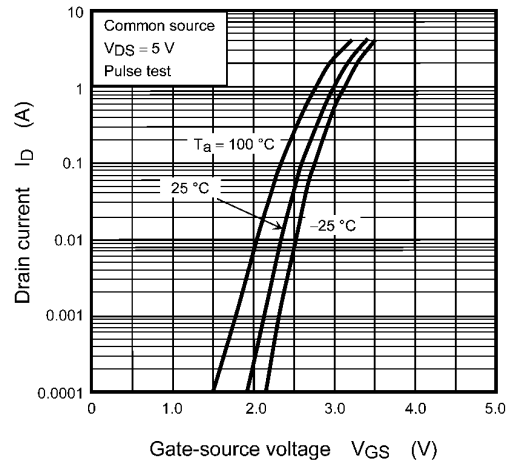


Fig. 6.1 Marking

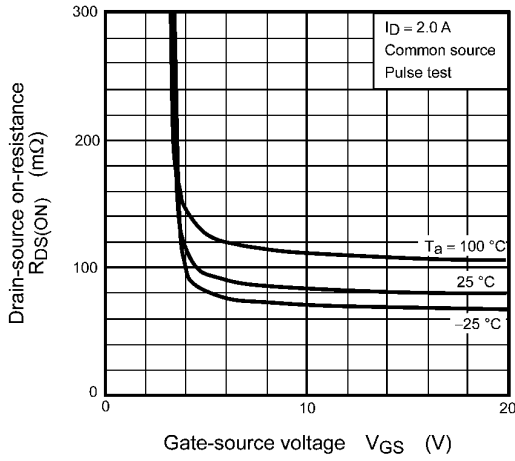
**7. Characteristics Curves (Note)**



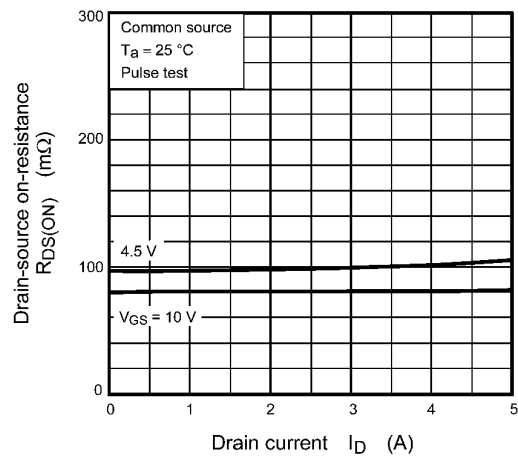
**Fig. 7.1  $I_D - V_{DS}$**



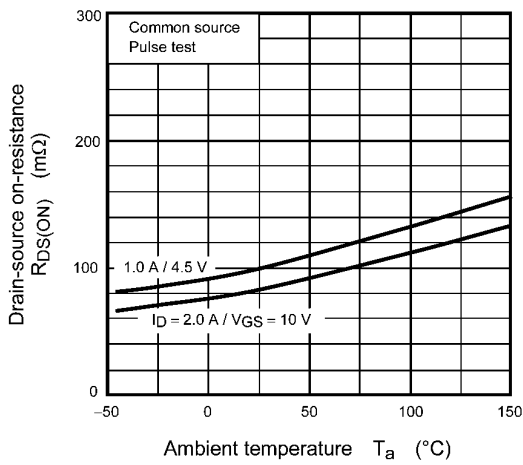
**Fig. 7.2  $I_D - V_{GS}$**



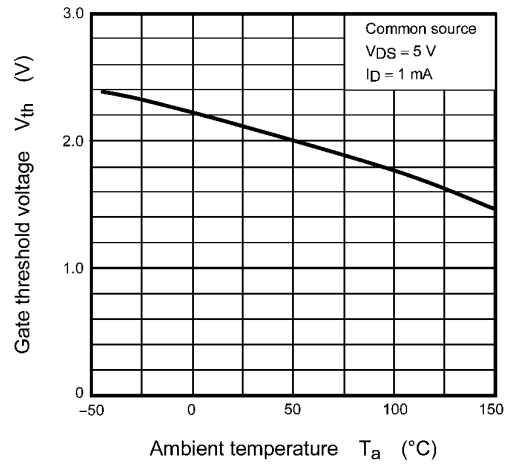
**Fig. 7.3  $R_{DS(ON)} - V_{GS}$**



**Fig. 7.4  $R_{DS(ON)} - I_D$**



**Fig. 7.5  $R_{DS(ON)} - T_a$**



**Fig. 7.6  $V_{th} - T_a$**

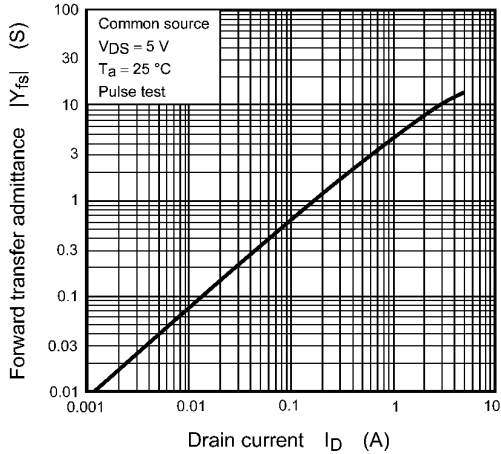


Fig. 7.7  $|Y_{fs}| - I_D$

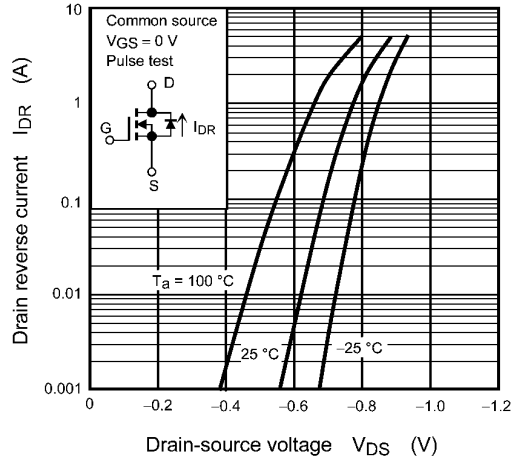


Fig. 7.8  $I_{DR} - V_{DS}$

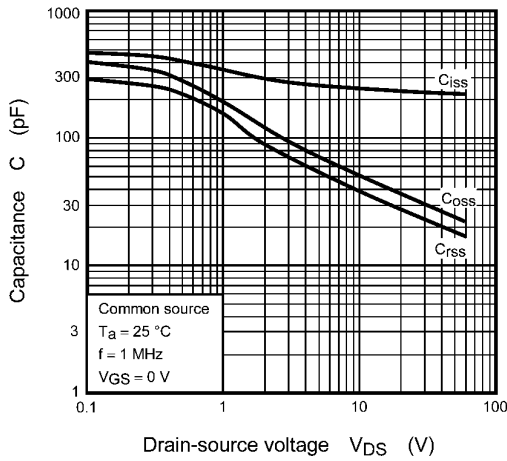


Fig. 7.9  $C - V_{DS}$

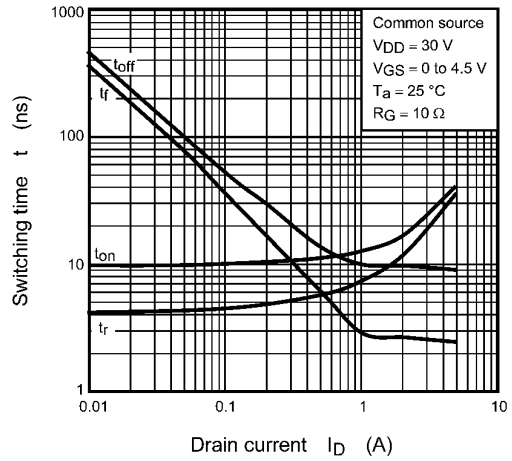


Fig. 7.10  $t - I_D$

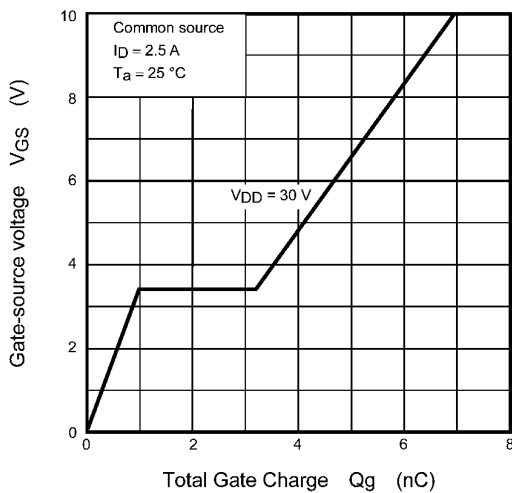


Fig. 7.11 Dynamic Input Characteristics

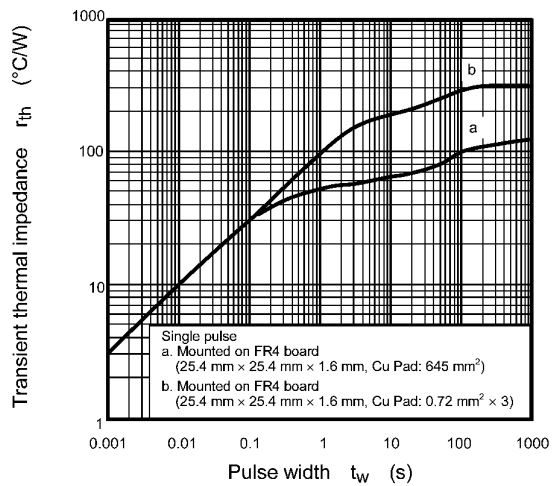


Fig. 7.12  $r_{th} - t_w$

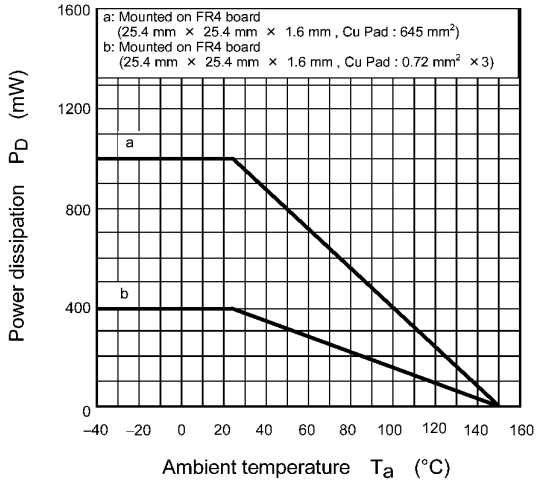


Fig. 7.13  $P_D - T_a$

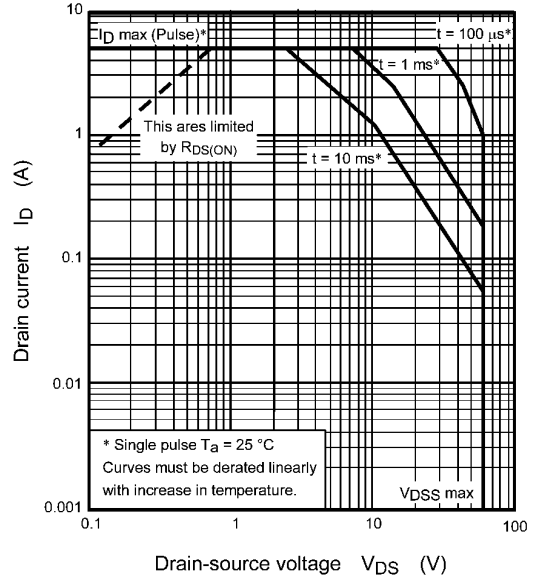


Fig. 7.14 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.011 g (typ.)

Package Name(s)
Nickname: SOT-23F



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