Unit: mm

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K37CT

- High Speed Switching Applications
- Analog Switch Applications

1.5Vdrive

Low ON-resistance $R_{DS(ON)} = 5.60 \Omega \text{ (max) (@V_{GS} = 1.5 V)}$

 $R_{DS(ON)} = 4.05 \Omega \text{ (max) (@V_{GS} = 1.8 V)}$

 $R_{DS(ON)} = 3.02 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$

 $R_{DS(ON)} = 2.20 \Omega \text{ (max) } (@V_{GS} = 4.5 \text{ V})$

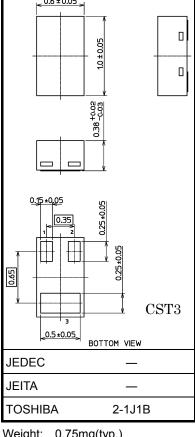
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	20	V	
Gate-Source voltage		V_{GSS}	± 10	V	
Drain current	DC	I _D	200	mA	
	Pulse	I _{DP}	400		
Power dissipation		P _D (Note1)	100	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

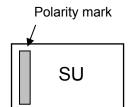


Weight: 0.75mg(typ.)

Note 1: Mounted on FR4 board

 $(10 \text{ mm} \times 10 \text{ mm} \times 1.0 \text{ mm}, \text{Cu Pad: } 100 \text{ mm}^2)$

Marking(top view)



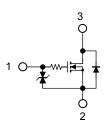
Pin Condition (top view)

Polarity mark (on the top)

- 1. Gate
- 2. Source
- 3. Drain

*Electrodes: On the bottom

Equivalent Circuit



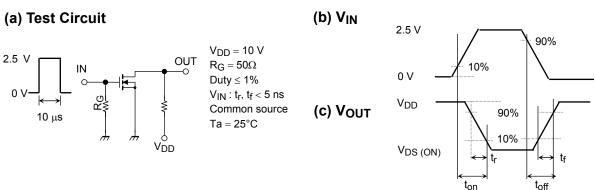
Start of commercial production 2010-11

Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain gourge brookdown voltage	V _{(BR)DSS}	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	20	_	_	· V	
Drain-source breakdown voltage		V (BR) DSX	$I_D = 1 \text{ mA}, V_{GS} = -10 \text{ V}$	12	_		_
Drain cut-off curre	nt	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	_	_	1	μА
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Gate threshold vol	tage	V _{th}	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.35	_	1.0	V
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = 3 \text{ V}, I_D = 100 \text{ mA}$ (Note2)	0.14	0.28	_	S
Drain-source ON-resistance	R _{DS} (ON)	$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$ (Note2)	_	1.65	2.20	Ω	
		$I_D = 50 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note2)	_	2.16	3.02		
		$I_D = 20 \text{ mA}, V_{GS} = 1.8 \text{ V}$ (Note2)	_	2.66	4.05		
		$I_D = 10 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note2)	_	3.07	5.60		
Input capacitance		C _{iss}		_	12	_	pF
Output capacitance	e	Coss	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	5.5	_	
Reverse transfer c	rse transfer capacitance C _{rss}		_	4.1	_	1	
Switching time	Turn-on time	t _{on}	V _{DD} = 10 V, I _D = 100 mA	_	18	_	ns
	Turn-off time	t _{off}	V_{GS} = 0 to 2.5 V, R_G = 50 Ω	_	36	_	
Drain-Source forwa	ard voltage	V _{DSF}	$I_D = -200 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note2)	_	-0.89	-1.2	V

Note2: Pulse test

Switching Time Test Circuit



Precaution

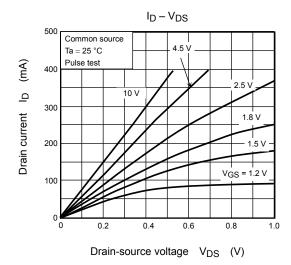
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (1mA for the SSM3K37CT). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

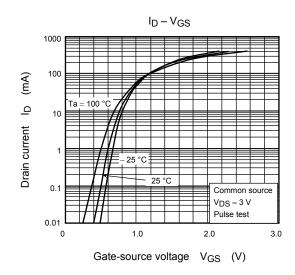
Take this into consideration when using the device.

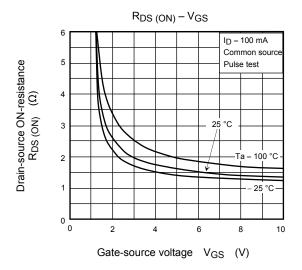
Handling Precaution

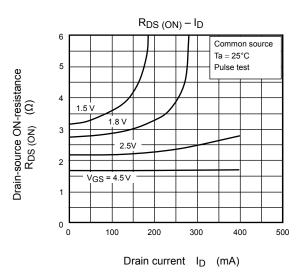
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

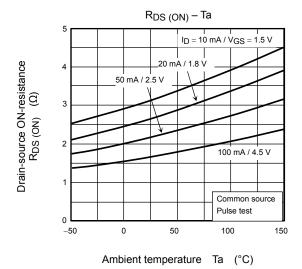
Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

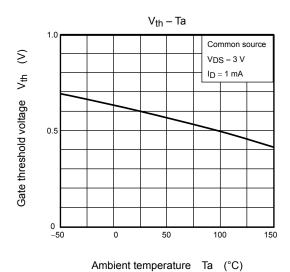






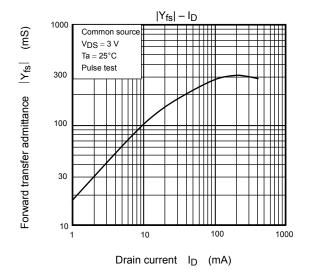


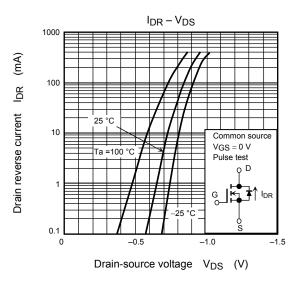


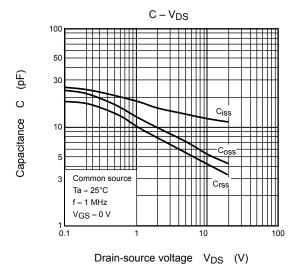


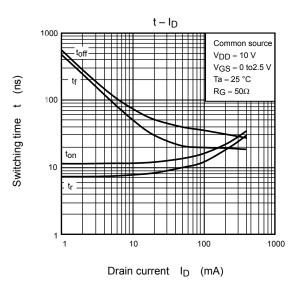
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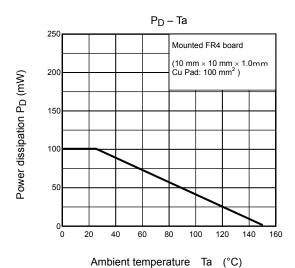
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