

SSM3K72CFS

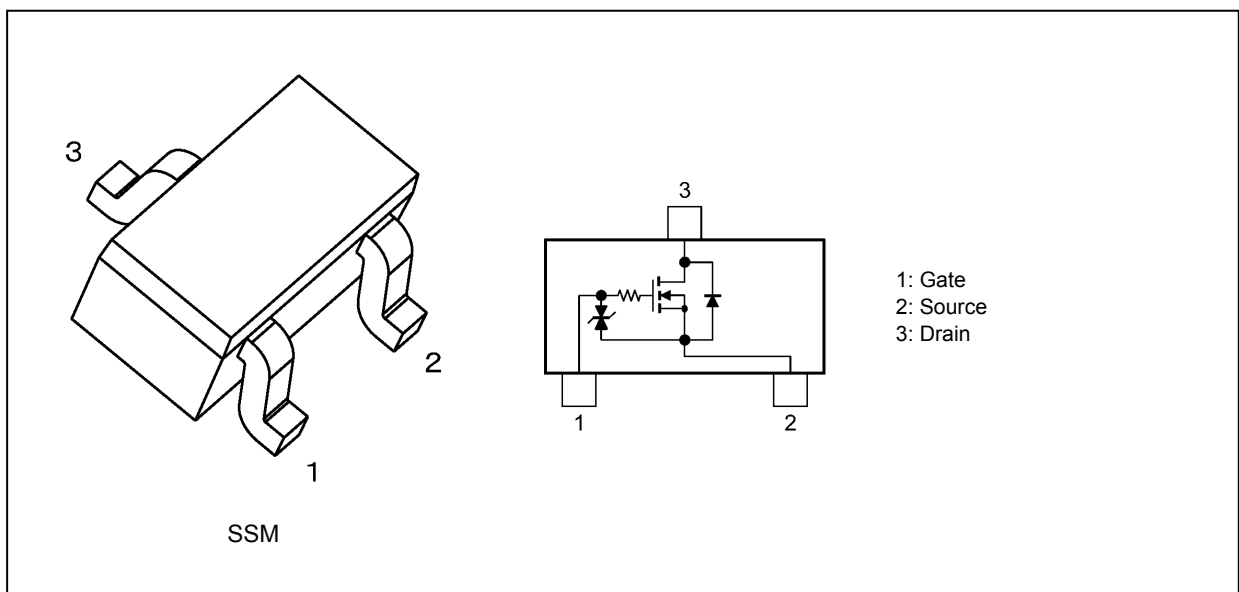
1. Applications

- High-Speed Switching

2. Features

- (1) ESD protected gate
- (2) Low drain-source on-resistance
 $R_{DS(ON)} = 2.8 \Omega$ (typ.) (@ $V_{GS} = 10 V$)
 $R_{DS(ON)} = 3.1 \Omega$ (typ.) (@ $V_{GS} = 5.0 V$)
 $R_{DS(ON)} = 3.2 \Omega$ (typ.) (@ $V_{GS} = 4.5 V$)

3. Packaging and Internal Circuit



Start of commercial production

2016-02

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GSS}	± 20	
Drain current (DC) (Note 1)	I_D	170	mA
Drain current (pulsed) (Note 1), (Note 2)	I_{DP}	680	
Power dissipation (Note 3)	P_D	150	mW
Power dissipation (Note 4)		500	
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed $150\text{ }^\circ\text{C}$.

Note 2: Pulse width $\leq 10\text{ }\mu\text{s}$, Duty $\leq 1\%$

Note 3: Device mounted on a $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$ FR4 glass epoxy board (Cu pad: $0.36\text{ mm}^2 \times 3$)

Note 4: Device mounted on a $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$ FR4 glass epoxy board (Cu pad: 645 mm^2)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	—	—	± 2	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$	—	—	± 0.5	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$	—	—	± 0.1	
Drain cut-off current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_j = 150\text{ }^\circ\text{C}$	—	—	200	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	60	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1	—	2.1	
Drain-source on-resistance (Note 1)	$R_{DS(ON)}$	$I_D = 100\text{ mA}, V_{GS} = 4.5\text{ V}$	—	3.2	4.7	Ω
		$I_D = 100\text{ mA}, V_{GS} = 5.0\text{ V}$	—	3.1	4.4	
		$I_D = 100\text{ mA}, V_{GS} = 10\text{ V}$	—	2.8	3.9	
		$I_D = 100\text{ mA}, V_{GS} = 10\text{ V}, T_j = 150\text{ }^\circ\text{C}$	—	5.4	8.1	
Forward transfer admittance (Note 1)	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	—	450	—	mS

Note 1: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	11	17	pF
Reverse transfer capacitance	C_{rss}		—	0.7	—	
Output capacitance	C_{oss}		—	3	—	
Switching time (rise time)	t_r	$V_{DD} = 40\text{ V}, I_D = 160\text{ mA}, V_{GS} = 0\text{ to }10\text{ V}, R_G = 50\text{ }\Omega$ Duty $\leq 1\%$, V_{IN} : $t_r, t_f < 5\text{ ns}$, Common source, See Chapter 5.3.	—	3	—	ns
Switching time (turn-on delay time)	$t_{d(on)}$		—	2	4	
Switching time (fall time)	t_f		—	24	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	7	14	

5.3. Switching Time Test Circuit

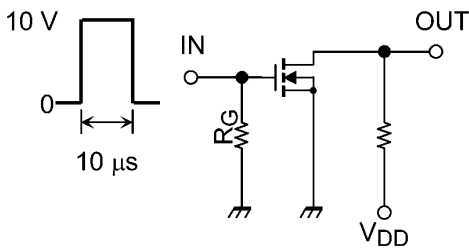


Fig. 5.3.1 Switching Time Test Circuit

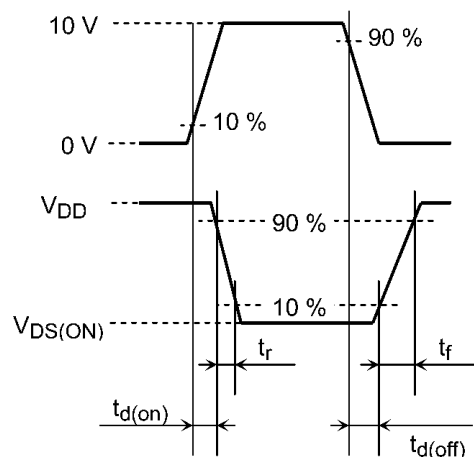


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

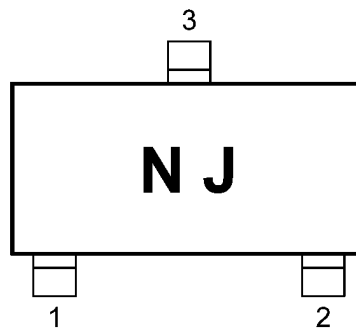
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} = 30\text{ V}$, $I_D = 200\text{ mA}$, $V_{GS} = 4.5\text{ V}$	—	0.27	0.35	nC
Gate-source charge	Q_{gs}		—	0.08	—	
Gate-drain charge	Q_{gd}		—	0.08	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V_{DSF}	$I_D = -115\text{ mA}$, $V_{GS} = 0\text{ V}$	—	-0.87	-1.2	V

Note 1: Pulse measurement.

6. Marking



7. Characteristics Curves (Note)

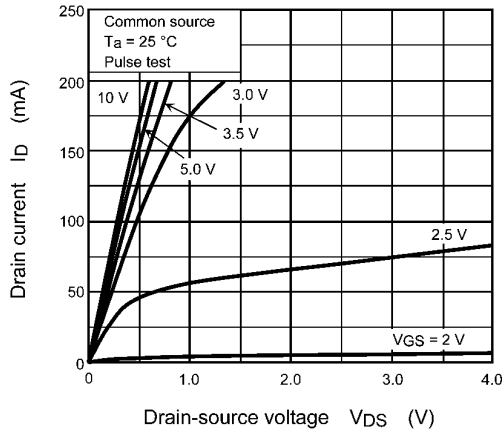


Fig. 7.1 $I_D - V_{DS}$

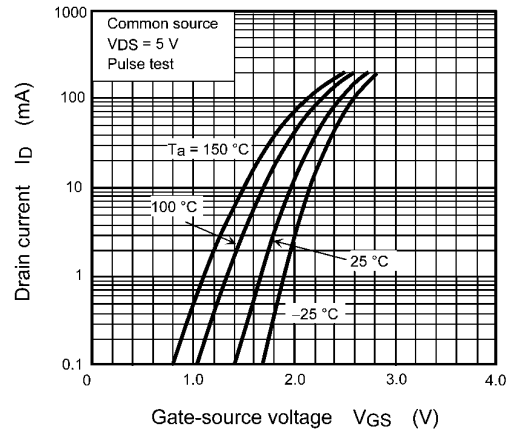


Fig. 7.2 $I_D - V_{GS}$

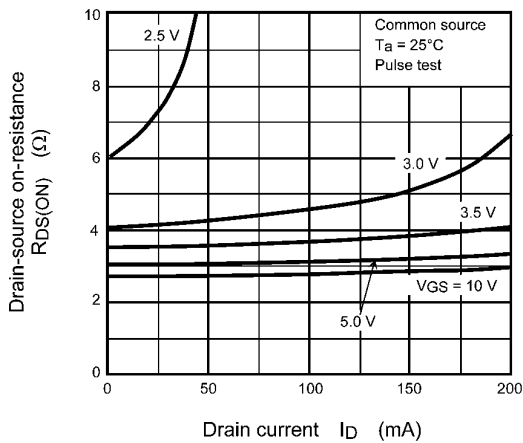


Fig. 7.3 $R_{DS(ON)} - I_D$

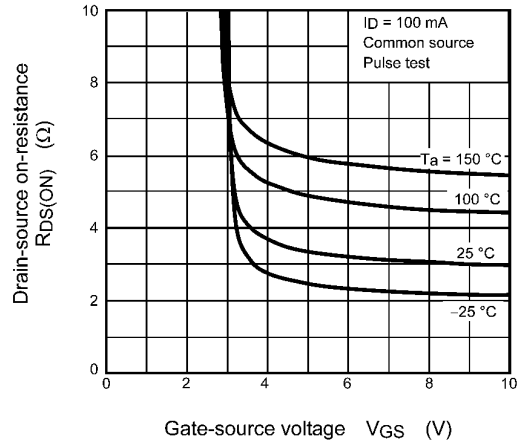


Fig. 7.4 $R_{DS(ON)} - V_{GS}$

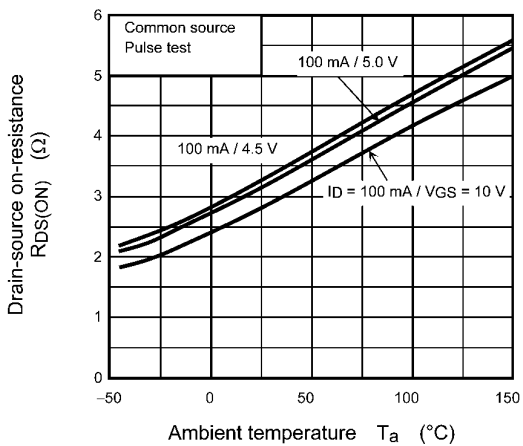


Fig. 7.5 $R_{DS(ON)} - T_a$

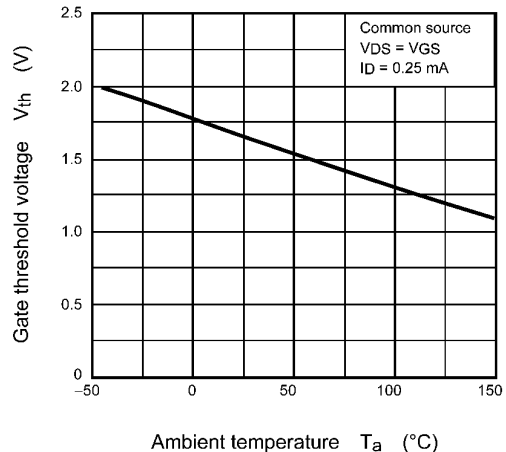


Fig. 7.6 $V_{th} - T_a$

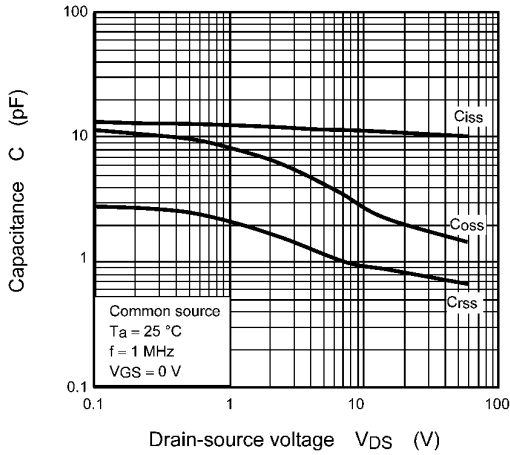


Fig. 7.7 C - V_{DS}

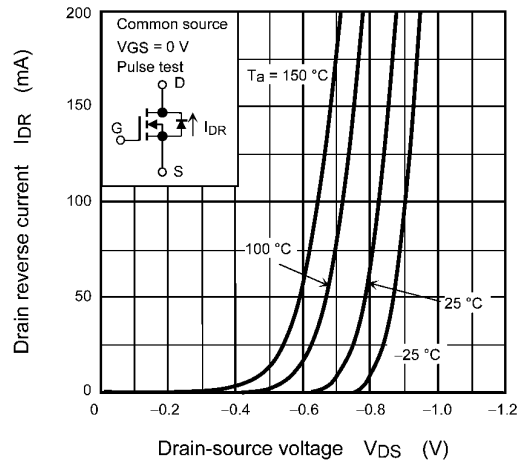


Fig. 7.8 I_{DR} - V_{DS}

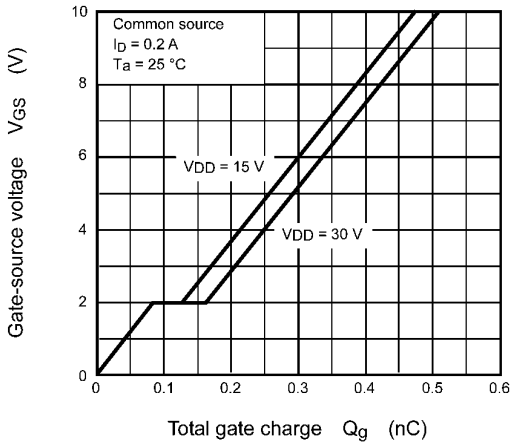


Fig. 7.9 Dynamic Input Characteristics

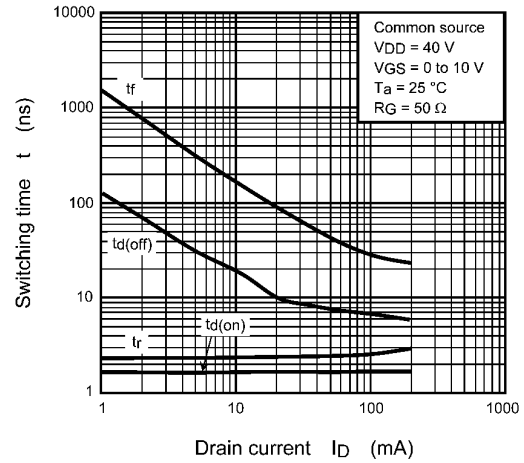


Fig. 7.10 t - I_D

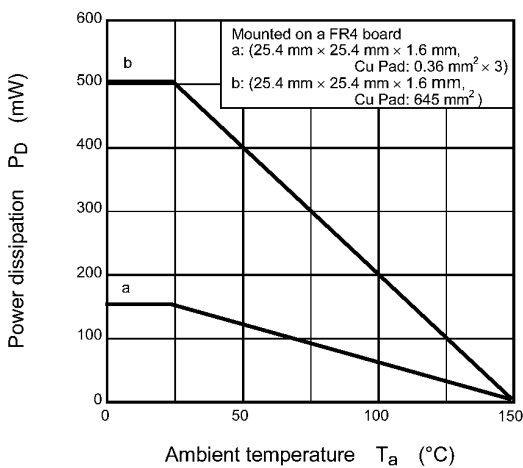


Fig. 7.11 P_D - T_a

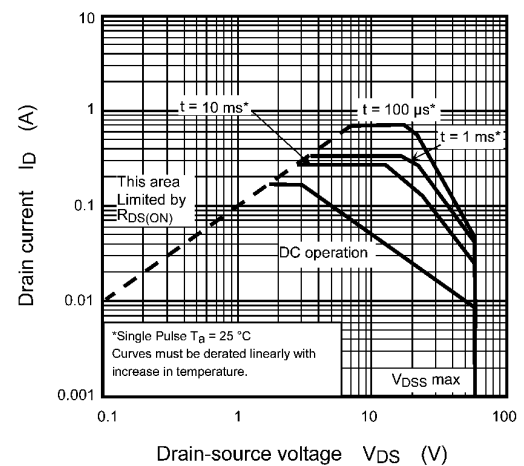
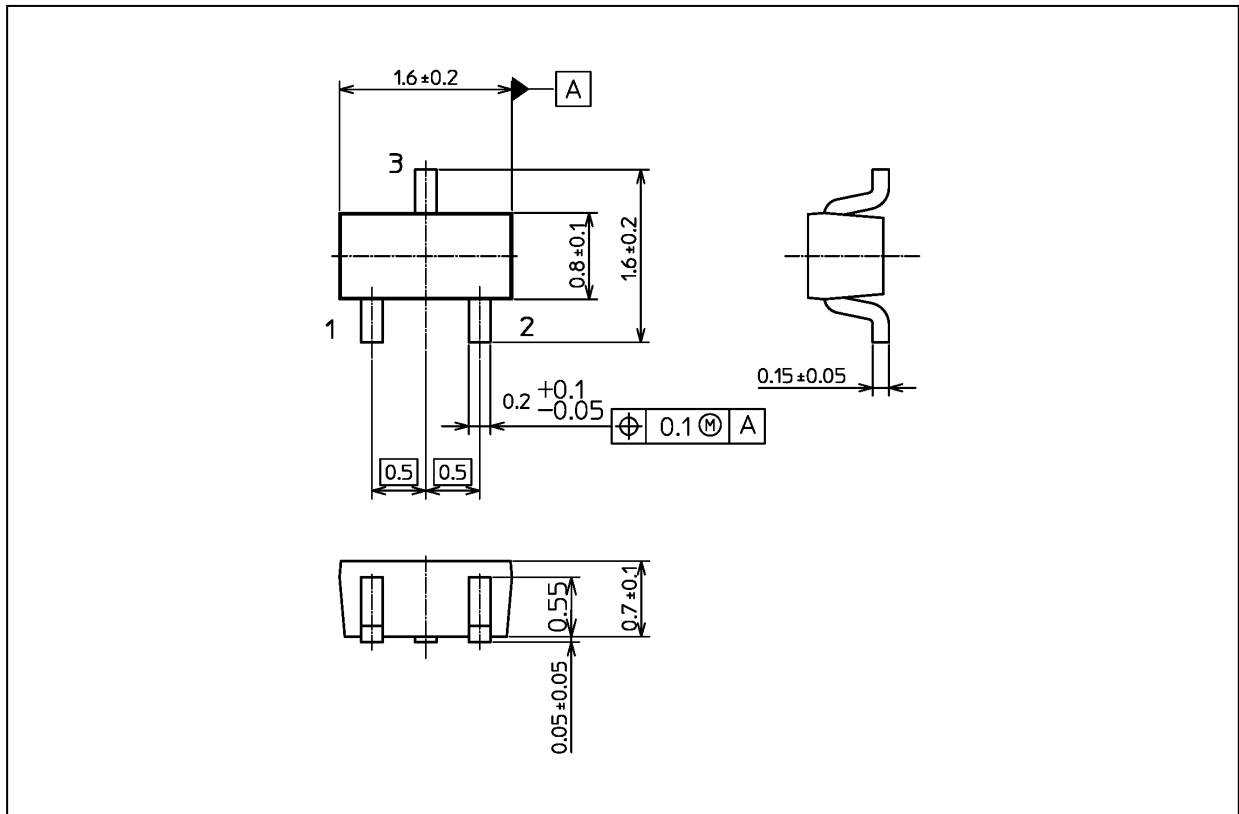


Fig. 7.12 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 2.4 mg (typ.)

Package Name(s)
JEDEC: SOT-416
Nickname: SSM

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