TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

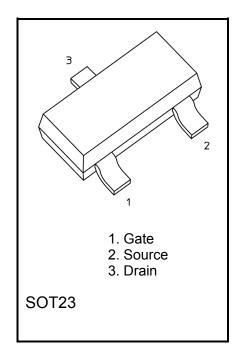
# T2N7002AK

○ High Speed Switching Applications

- ESD protected gate
- Low ON-resistance

#### Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage	V <sub>DSS</sub>	60	V		
Gate-source voltage		V <sub>GSS</sub>	$\pm 20$	V	
Drain current (Note1)	DC	Ι <sub>D</sub>	200	mA	
Drain current (Note1)	Pulse	I <sub>DP</sub> (Note 2)	760		
Dewer dissinction	P <sub>D</sub> (Note 3)	320	mW		
Power dissipation		P <sub>D</sub> (Note 4)	1000		
Channel temperature	T <sub>ch</sub>	150	°C		
Storage temperature		T <sub>stg</sub>	-55 to 150	°C	



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

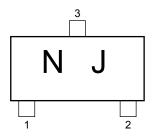
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

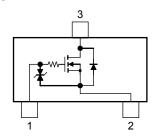
Note 2: Pulse width  $\leq$  10 µs, Duty  $\leq$  1%

- Note 3: Mounted on an FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu Pad: 0.42 mm<sup>2</sup> x 3)
- Note 4: Mounted on an FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu Pad: 645 mm² )

#### Marking



#### Equivalent Circuit (top view)



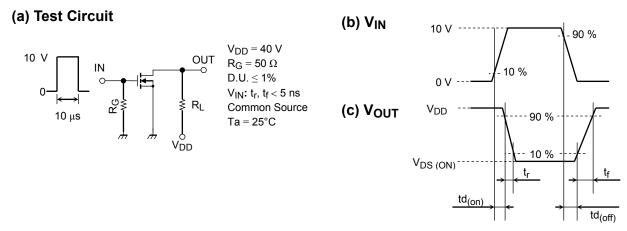
Start of commercial production 2015-01

### Electrical Characteristics (Ta = 25°C, Otherwise specified)

Characteristic		Symbol	Test Condition	Min	Тур.	Max	Unit	
Drain-source breakdown voltage		V (BR) DSS	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$	60	—	—	V	
Drain cutoff current		IDSS	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	—	—	1	- μΑ	
			$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ Tj}=150 ^{\circ}\text{C}$	_	—	200		
Gate leakage current		IGSS	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	—	±2		
			$V_{GS} = \pm 10 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	—	—	±0.5	μA	
			$V_{GS} = \pm 5 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	—	—	±0.1		
Gate threshold	d voltage	V <sub>th</sub>	$I_D = 250 \ \mu A, \ V_{DS} = V_{GS}$	1.1	—	2.1	V	
Forward trans	fer admittance	Y <sub>fs</sub>	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 200 \text{ mA}$ (Note 5)	—	450	_	mS	
Drain-source ON-resistance		R <sub>DS (ON)</sub> (Note 5)	$I_D = 100 \text{ mA}, V_{GS} = 10 \text{ V}$	—	2.8	3.9	Ω	
			$I_D = 100 \text{ mA}, V_{GS} = 10 \text{ V}, \text{ Tj}=150 ^{\circ}\text{C}$	—	5.4	8.1		
			$I_D = 100 \text{ mA}, V_{GS} = 5 \text{ V}$	—	3.1	4.4		
			$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$	—	3.2	4.7		
Total Gate Charge Gate-Source Charge		Q <sub>G(tot)</sub>	V = 20 V   = 200 mA	—	0.27	0.35	nC	
		Q <sub>GS</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 200 mA V <sub>GS</sub> = 4.5 V	_	0.08	_		
Gate-Drain Charge		Q <sub>GD</sub>	VGS - 4.5 V	—	0.08	_		
Input capacitance		C <sub>iss</sub>		—	11	17	pF	
Output capacitance		C <sub>oss</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz	—	3	_		
Reverse transfer capacitance		C <sub>rss</sub>		_	0.7	_		
Switching time	Turn-on delay time	t <sub>d(on)</sub>		—	2	4		
	Rise time	tr	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 160 mA	_	3	_	- ns	
	Turn-off delay time	t <sub>d(off)</sub>	$V_{GS}$ = 0 V to 10 V, $R_{G}$ = 50 $\Omega$	_	7	14		
	Fall time	t <sub>f</sub>	]	_	24	—		
Drain-source forward voltage		V <sub>DSF</sub>	$I_D = -115 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 5)	_	-0.87	-1.2	V	

Note 5: Pulse test

### **Switching Time Test Circuit**



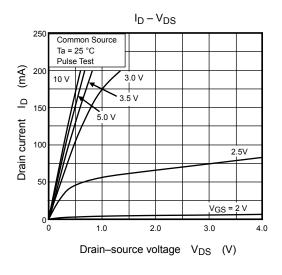
#### Notice of Usage

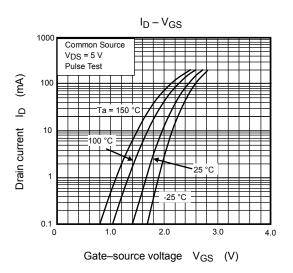
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current (ID) to below (0.25 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ . Take this into consideration when using the device.

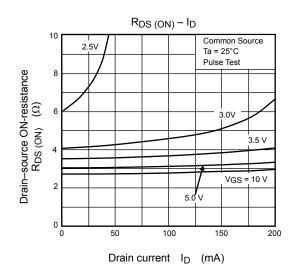
### **Handling Precaution**

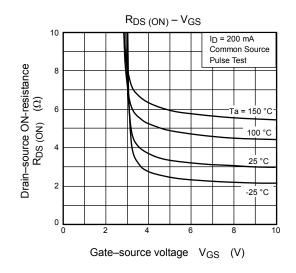
The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

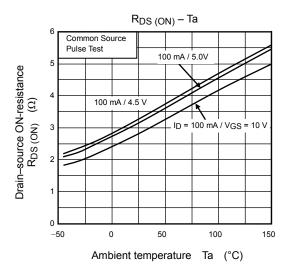
# **TOSHIBA**

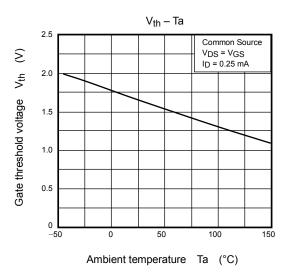












# **TOSHIBA**

S

 $V_{GS}$ 

Gate-source voltage

2

0 **k** 0

0.1

0.2

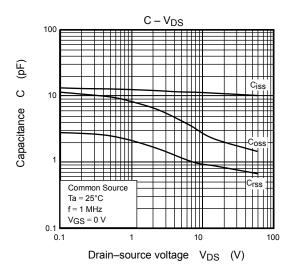
0.3

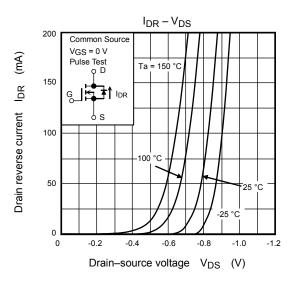
Total Gate Charge Qg (nC)

0.4

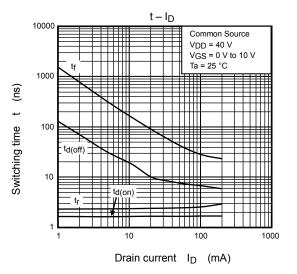
0.5

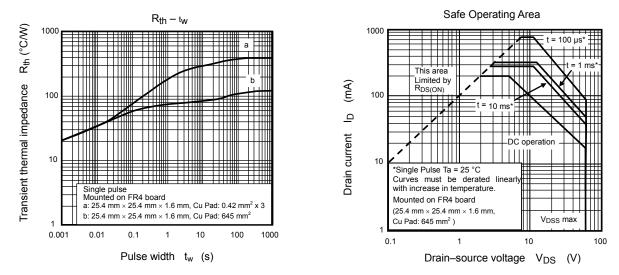
0.6





Dynamic Input Characteristic





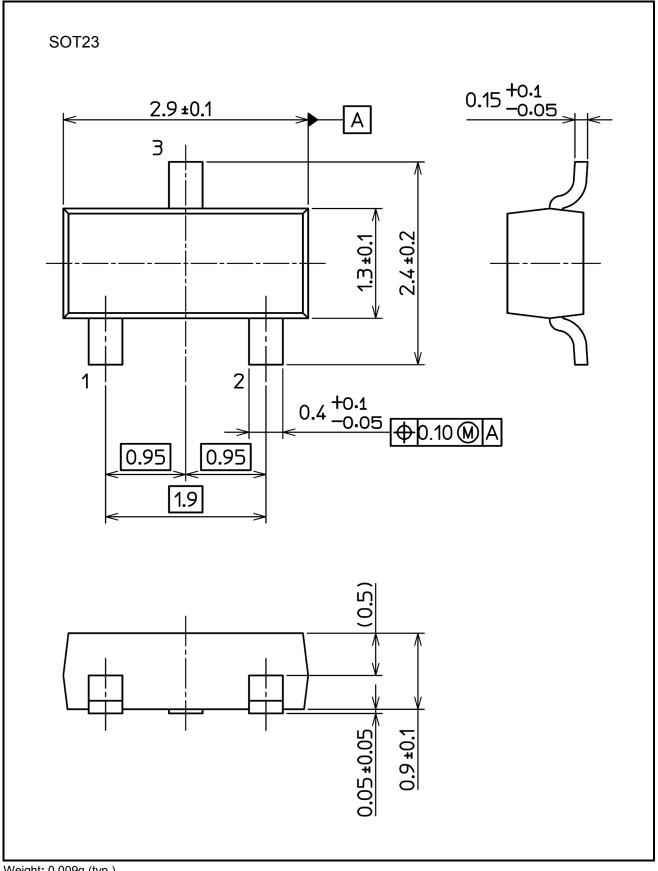
Note: The above characteristics curves are presented for reference only and not guaranteed by production test.

# **TOSHIBA**

#### **Package Dimensions**

T2N7002AK

Unit: mm



Weight: 0.009g (typ.)

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