

TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB62208FG

BiCD Constant-Current Two-Phase Bipolar Stepping Motor Driver IC

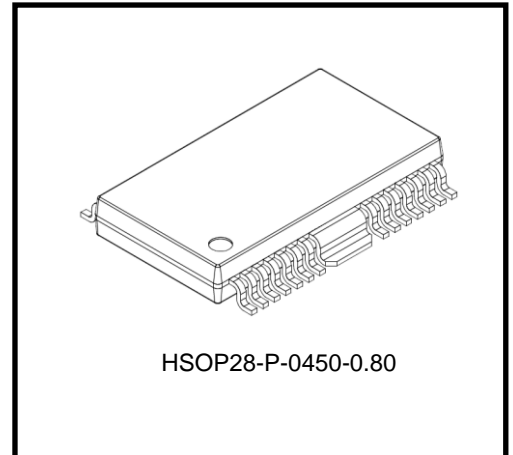
The TB62208FG is a two-phase bipolar stepping motor driver using a PWM chopper.

Fabricated with the BiCD process, the TB62208FG is rated at 40 V/1.8 A.

The on-chip voltage regulator allows control of a stepping motor with a single VM power supply.

Features

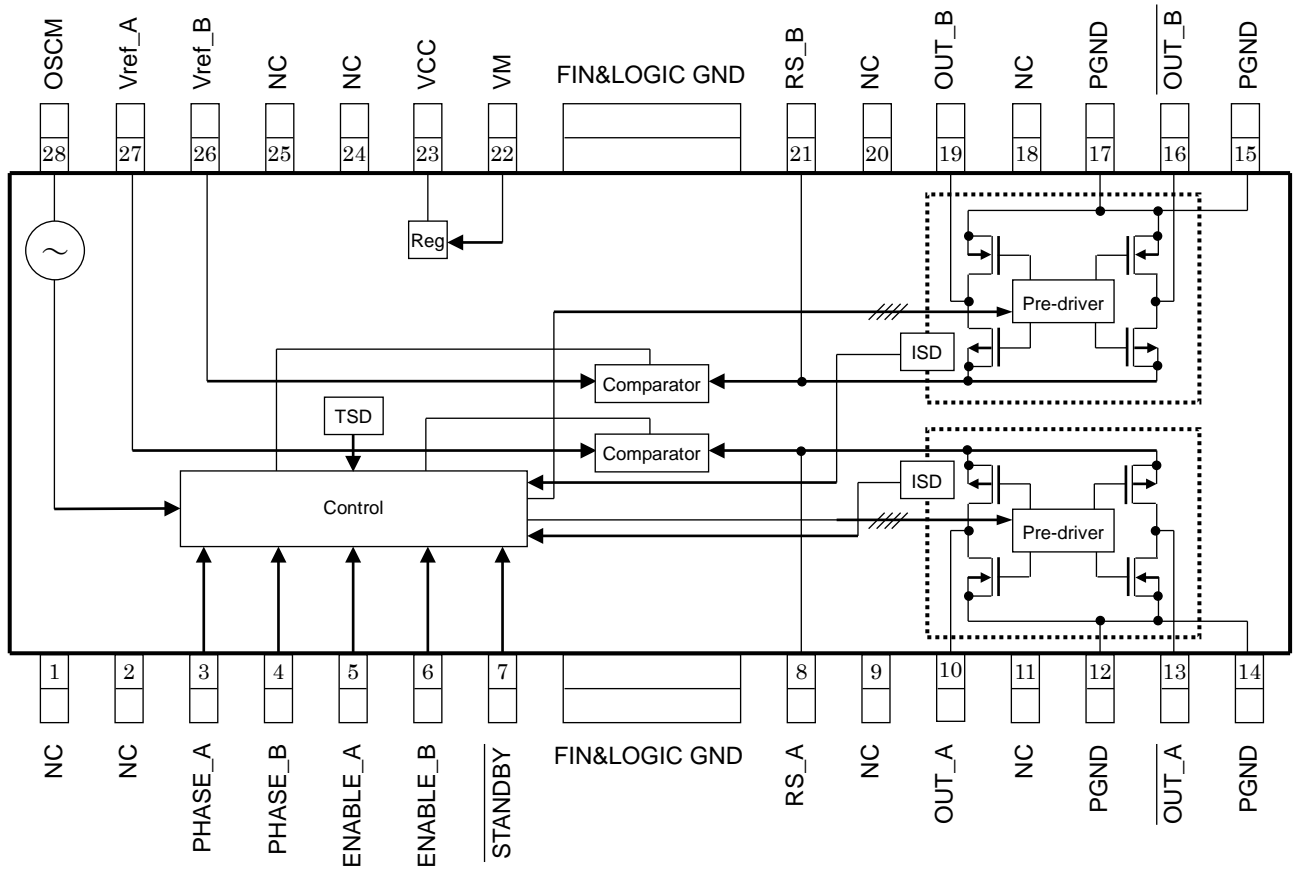
- Bipolar stepping motor driver
- PWM constant-current drive
- Provides phase-A and phase-B enable inputs to allow 2-phase and 1-2-phase excitation.
- BiCD process: Uses DMOS FETs as output power transistors.
- High voltage and current: 40 V/1.8 A
- Thermal shutdown (TSD), over-current shutdown (ISD), and power-on-resets (PORs) for VMR and VCCR
- Package: Heat-sink Small Outline Package (HSOP28-P-0450-0.80)



HSOP28-P-0450-0.80

Weight: 0.79 g (typ.)

Block Diagram

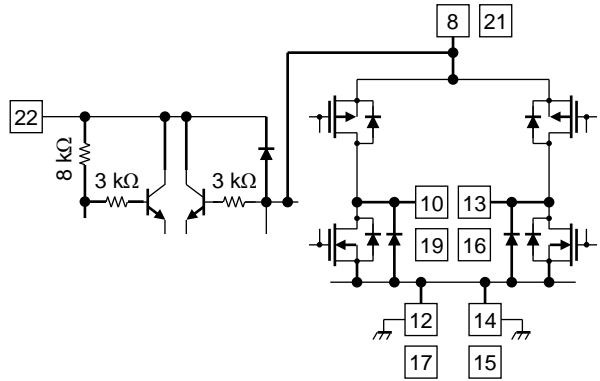
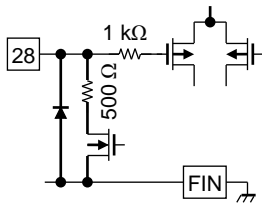
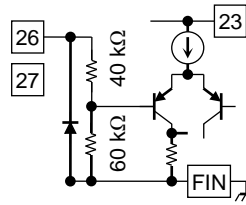
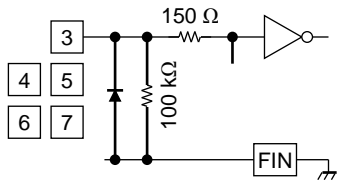


In the block diagram, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.

Pin Function

| Pin # | Pin Name | Function |
|-------|-----------------------------|---|
| 1 | NC | No-connect |
| 2 | NC | No-connect |
| 3 | PHASE_A | Phase-A motor output current direction selector |
| 4 | PHASE_B | Phase-B motor output current direction selector |
| 5 | ENABLE_A | Phase-A motor output enable SW 5V:OUTPUT ON / GND:OUTPUT OFF |
| 6 | ENABLE_B | Phase-B motor output enable SW 5V:OUTPUT ON / GND:OUTPUT OFF |
| 7 | $\overline{\text{STANDBY}}$ | Power-saving waiting mode SW pin with stopping OSCM and motor outputs |
| FIN | FIN&Logic GND | This fin is a heat sink which functions as logic GND. This must be connected to GND line of board. |
| 8 | RS_A | Power supply for the Phase-A motor output and sensing of the current |
| 9 | NC | No-connect |
| 10 | OUT_A | Positive phase-A motor output |
| 11 | NC | No-connect |
| 12 | PGND | Motor power ground |
| 13 | $\overline{\text{OUT_A}}$ | Negative phase-A motor output |
| 14 | PGND | Motor power ground |
| 15 | PGND | Motor power ground |
| 16 | $\overline{\text{OUT_B}}$ | Negative phase-B motor output |
| 17 | PGND | Motor power ground |
| 18 | NC | No-connect |
| 19 | OUT_B | Positive phase-B motor output |
| 20 | NC | No-connect |
| 21 | RS_B | Power supply for the Phase-B motor output and sensing of the current |
| FIN | FIN&Logic GND | This fin is a heat sink which functions as logic GND. This must be connected to GND line of board. |
| 22 | VM | Power supply |
| 23 | Vcc | Smoothing filter for internal 5V power supply |
| 24 | NC | No-connect |
| 25 | NC | No-connect |
| 26 | Vref_B | Tunes the current level for phase-B motor output |
| 27 | Vref_A | Tunes the current level for phase-A motor output |
| 28 | OSCM | Tunes frequency of oscillator for chopping |

Pin Interfaces



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Output Function Table

| | Pin name | | | OUT(+) | OUT(-) | OSC_M |
|----------|--|--|---|--------|--------|-------------|
| | $\overline{\text{STAND BY}}$ | PHASE | ENABLE | | | |
| Function | Power-saving waiting SW "L" : disable the OSCM and Outputs. The motor can not be operated | The determination pin of the direction of motor current "H" : Current flows into OUT(-) from OUT(+) | The ON/FFF switch of the output transistors "L" : Output pins will be in a high impedance state. | | | |
| State | L | X | X | OFF | OFF | a halt |
| | H | X | L | OFF | OFF | oscillation |
| | H | H | H | H | L | oscillation |
| | H | L | H | L | H | oscillation |

X : Don't-care

Protection Features

- (1) Thermal shutdown (TSD)
The thermal shutdown circuit turns off all the outputs when the junction temperature (Tj) exceeds 150°C (typical). The outputs retain the current states.
The TB62208FG exits TSD mode and resumes normal operation when the TB62208FG is rebooted or the $\overline{\text{STANDBY}}$ pin is changed from High to Low and then to High.
- (2) Power-on-resets (PORs) for VMR and VCCR (VM and VCC voltage monitor)
The outputs are forced off until VM and VCC reach the rated voltages.
- (3) Overcurrent shutdown (ISD)
Each phase has an overcurrent shutdown circuit, which turns off the corresponding outputs when the output current exceeds the shutdown trip threshold (above the maximum current rating: 2.0 A minimum).
The TB62208FG exits ISD mode and resumes normal operation when the $\overline{\text{STANDBY}}$ pin is changed from High to Low and then to High.
This circuit provides protection against a short-circuit by temporarily disabling the device. Important notes on this feature will be provided later.

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|----------------------------|---------------------|-------------|------|
| Motor power supply | V _M | 40 | V |
| Motor output voltage | V _{out} | 40 | V |
| Output current (Note 1) | I _{OUT} | 1.8 | A |
| Logic input voltage | V _{IN} | -0.5 to 6.0 | V |
| Power dissipation (Note 2) | P _D | 1.3 | W |
| Operating temperature | T _{opr} | -20 to 85 | °C |
| Storage temperature | T _{stg} | -55 to 150 | °C |
| Junction temperature | T _{j(max)} | 150 | °C |

Note 1: As a guide, the maximum output current should be kept below 1.0 A per phase. The maximum output current may be further limited by thermal considerations, depending on ambient temperature and board conditions.

Note 2: Stand-alone

T_a: Ambient temperature

T_{opr}: Ambient temperature while the TB62208FG is active

T_j: Junction temperature while the TB62208FG is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry.

It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, T_{j(max)}, will not exceed 120°C.

Cautions on absolute maximum ratings:

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TB62208FG does not have overvoltage protection. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.

All voltage ratings including supply voltages must always be followed. The section on the protection features on page 8 should also be referred to.

Operating Ranges (Ta = 0 to 85°C)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--|--------------------|------------------------------------|-----|------|------|------|
| Supply voltage for internal circuitry | V _{CC} | Internally generated | 4.5 | 5.0 | 5.5 | V |
| Motor supply voltage | V _M | — | 10 | 24 | 38 | V |
| Output current | I _{OUT} | Ta = 25°C; Per phase | — | 1.2 | 1.8 | A |
| Digital input voltage | V _{IN(H)} | Logic High level | 2.0 | 3.3 | 5 | V |
| | V _{IN(L)} | Logic Low level | GND | — | 1.0 | V |
| Phase input frequency | f _{PHASE} | — | — | 1.0 | 150 | kHz |
| Chopper frequency | f _{chop} | — | 80 | 100 | 120 | kHz |
| V _{ref} reference voltage | V _{ref} | — | GND | 3.0 | 3.6 | V |
| Voltage across the current-sensing resistor pins (Voltage across VM and RS) | V _{RS} | Referenced to the VM pin (Note) | 0 | ±1.0 | ±1.5 | V |

Note: The maximum VRS voltage should not exceed the maximum rated voltage.

Electrical Characteristics 1 (Ta = 25°C, VM = 24 V, unless otherwise specified)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | |
|---|-----------------------|---------------------|--|--|------|-----|------|----|
| Input hysteresis voltage | V _{IN (HIS)} | DC | Logic input pins (Note) | 100 | 200 | 300 | mV | |
| Logic input current | High | I _{IN (H)} | DC | Logic input pins; V _{IN} = 5 V | 35 | 50 | 75 | μA |
| | Low | I _{IN (L)} | | Logic input pins; V _{IN} = 0 V | — | — | 1.0 | |
| Supply current (V _M pin) | | I _{M1} | DC | Outputs open Logic inputs: All Lows Logic and outputs disabled | — | 2 | 3 | mA |
| | | I _{M2} | | Outputs open; f _{PHASE} = 1 kHz Logic enabled; All outputs disabled | — | 3.5 | 5 | |
| | | I _{M3} | | Outputs open; f _{PHASE} = 4 kHz Logic enabled (2-phase excitation; 100-kHz chopping) | — | 5 | 7 | |
| Output leakage current | High-side | I _{OH} | DC | V _{RS} = V _M = 40 V; V _{OUT} = 0 V; Digital inputs: All Lows | — | — | 1 | μA |
| | Low-side | I _{OL} | DC | V _{RS} = V _M = V _{OUT} = 40 V; Digital inputs: all Lows | 1 | — | — | μA |
| Channel-to-channel current differential | ΔI _{OUT1} | DC | Channel-to-channel error | −5 | 0 | 5 | % | |
| Output current error relative to the predetermined value | ΔI _{OUT2} | DC | I _{OUT} = 1.0A | −5 | 0 | 5 | % | |
| RS pin current | I _{RS} | DC | V _{RS} = V _M = 24 V STANDBY = L | 0 | — | 10 | μA | |
| Drain-source ON-resistance of the output transistors (upper and lower sum) | R _{ON (D-S)} | DC | I _{OUT} = 1.0 A, T _j = 25°C | — | 1.2 | 1.5 | Ω | |

Note : V_{IN(L→H)} is defined as the V_{IN} voltage that causes the outputs (pins 10 and 11) to change when a pin under test is gradually raised from 0 V. V_{IN(H→L)} is defined as the V_{IN} voltage that causes the outputs (pins 10 and 11) to change when the pin is then gradually lowered.

The difference between V_{IN(L→H)} and V_{IN(H→L)} is defined as the input hysteresis.

Electrical Characteristics 2 (Ta = 25°C, VM = 24 V, unless otherwise specified)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------------------------|-------------|--------------|--|-------|-------|-------|------|
| Vref input voltage range | Vref | DC | VM = 24 V, $\overline{\text{STANDBY}} = \text{H}$, outputs enabled, PHASE = 1 kHz | GND | 3.0 | 5.0 | V |
| Vref input current | Iref | DC | $\overline{\text{STANDBY}} = \text{H}$ output enabled, Vref = 3.0 V | 20 | 35 | 50 | μA |
| Vref decay rate | Vref (GAIN) | DC | $\overline{\text{STANDBY}} = \text{H}$, output enabled, Vref = 2.0 V | 1/4.8 | 1/5.0 | 1/5.2 | - |
| TSD threshold (Note 1) | TjTSD | DC | VM = 24 V | 140 | 155 | 170 | °C |
| VM recovery voltage | VMR | DC | $\overline{\text{STANDBY}} = \text{H}$ | 7.0 | 8.0 | 9.0 | V |
| Overcurrent trip threshold (Note 2) | ISD | — | — | 2.0 | 3.0 | 4.0 | A |

Note 1: Thermal shutdown (TSD) circuitry

When the junction temperature of the device has reached the threshold, the TSD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.

The TSD circuitry is tripped at a temperature between 140°C (min) and 160°C (max). Once tripped, the TSD circuitry keeps the output transistors off until $\overline{\text{STANDBY}}$ is deasserted High.

Note 2: Overcurrent shutdown (ISD) circuitry

When the output current has reached the threshold, the ISD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.

To prevent the ISD circuitry from being tripped due to switching noise, it has a masking time of four CR oscillator cycles. Once tripped, it takes a maximum of four cycles to exit ISD mode and resume normal operation.

The ISD circuitry remains active until the $\overline{\text{STANDBY}}$ pin is changed from Low to High again.

The TB62208FG remains in Standby mode while in ISD mode.

Back-EMF

- While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF. If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB62208FG or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

- The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit.
- If the device is used beyond the specified operating ranges, these circuits may not operate properly; then the device may be damaged due to an output short-circuit.
- The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

IC Mounting

Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause the device breakdown, damage and/or deterioration.

AC Electrical Characteristics (Ta = 25°C, Vm = 24 V, 6.8 mH/5.7 Ω)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|--------------------------|--------------|---|------|------|------|------|
| Phase frequency | f _{PHASE} | AC | OSC = 1600 kHz | – | – | 400 | kHz |
| Minimum phase pulse width | t _{PHASE} | AC | – | 100 | – | – | ns |
| | t _{wp} | AC | | 50 | – | – | |
| | t _{wn} | AC | | 50 | – | – | |
| Output transistor switching characteristics | t _r | – | – | 150 | 200 | 250 | ns |
| | t _f | – | | 100 | 150 | 200 | |
| | t _{pLH(P)MAX} | – | PHASE to OUT | 500 | 850 | 1200 | |
| | t _{pHL(P)MAX} | – | | 500 | 850 | 1200 | |
| | t _{pLH(P)MIN} | – | | 250 | 600 | 950 | |
| | t _{pHL(P)MIN} | – | | 250 | 600 | 950 | |
| | t _{pLH(O)} | – | CR(OSC) to OUT | 300 | 600 | 900 | |
| t _{pHL(O)} | – | 350 | | 650 | 950 | | |
| Blanking time for current spike prevention | t _{BLANK} | – | I _{OUT} = 1.0 A | 200 | 300 | 500 | ns |
| CR oscillation reference frequency | f _{CR} | – | C _{osc} = 270 pF, R _{osc} = 3.6 kΩ | 1200 | 1600 | 2000 | kHz |
| Chopper frequency range | f _{chop(RANGE)} | – | V _M = 24 V, outputs enabled, (I _{OUT} = 1.0 A) | 40 | 100 | 150 | kHz |
| Predefined chopper frequency | f _{chop} | – | Outputs enabled (I _{OUT} = 1.0 A), CR = 1600 kHz | – | 100 | – | kHz |
| ISD masking time | t _{ISD(Mask)} | AC | The number of CR-CLK pulses after ISD threshold is exceeded due to an output short-circuit to powerline or ground | – | 4 | – | - |
| ISD on-time | t _{ISD} | AC | | 4 | – | 8 | |

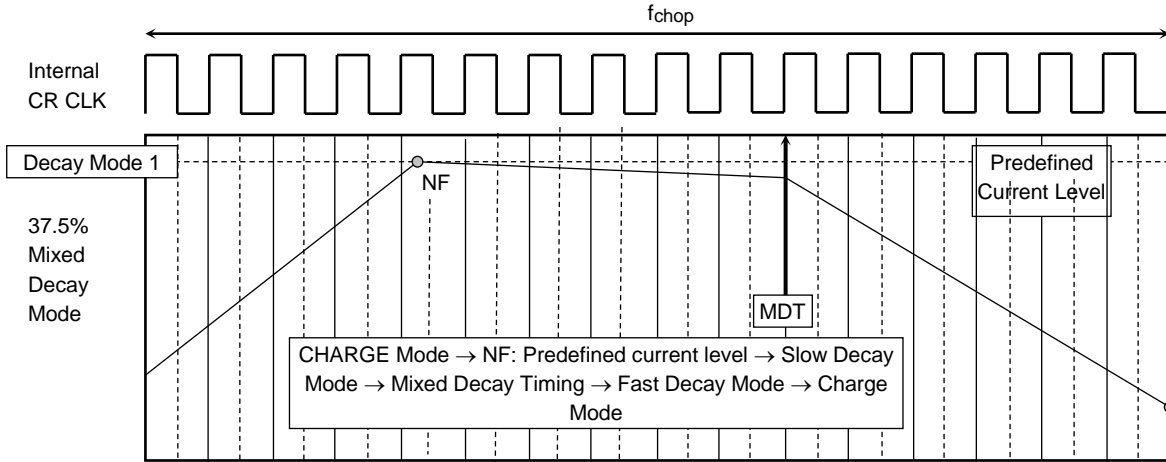
OSC_M frequency can be calculated by the following approximate formula.
Please give as a reference of frequency adjustment.

$$f_{OSCM} = \frac{1}{0.6 \times C \times (R_1 + 500)}$$

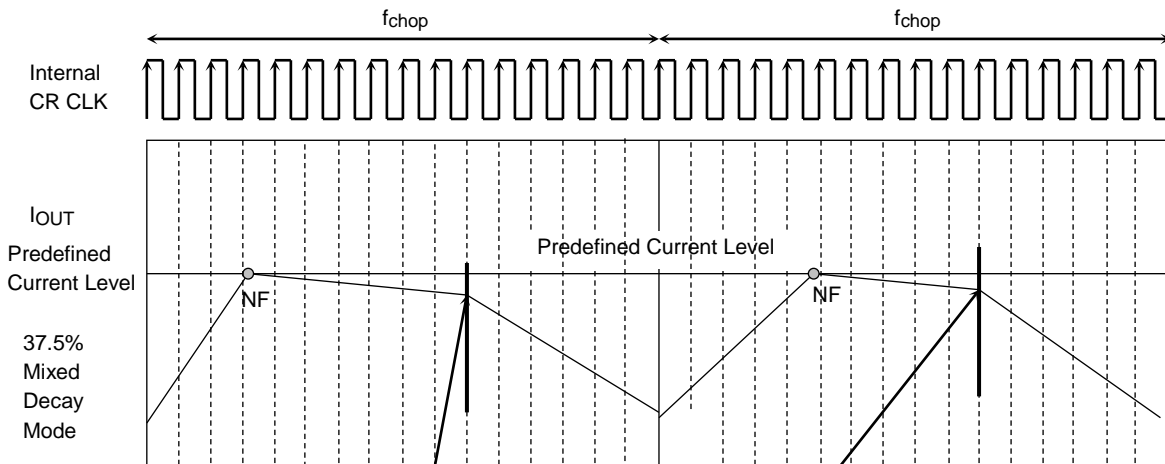
.....C, R₁: The external constant for OSCM
(C=270pF, R₁=3.6kΩ on an application circuit diagram)

Current Waveform in Mixed Decay Mode

For constant-current control, Mixed-Decay mode starts out in Fast-Decay mode for 37.5% of the whole period and then is followed by Slow-Decay mode for the remainder of the period.



Current Waveform in MIXED DECAY Mode

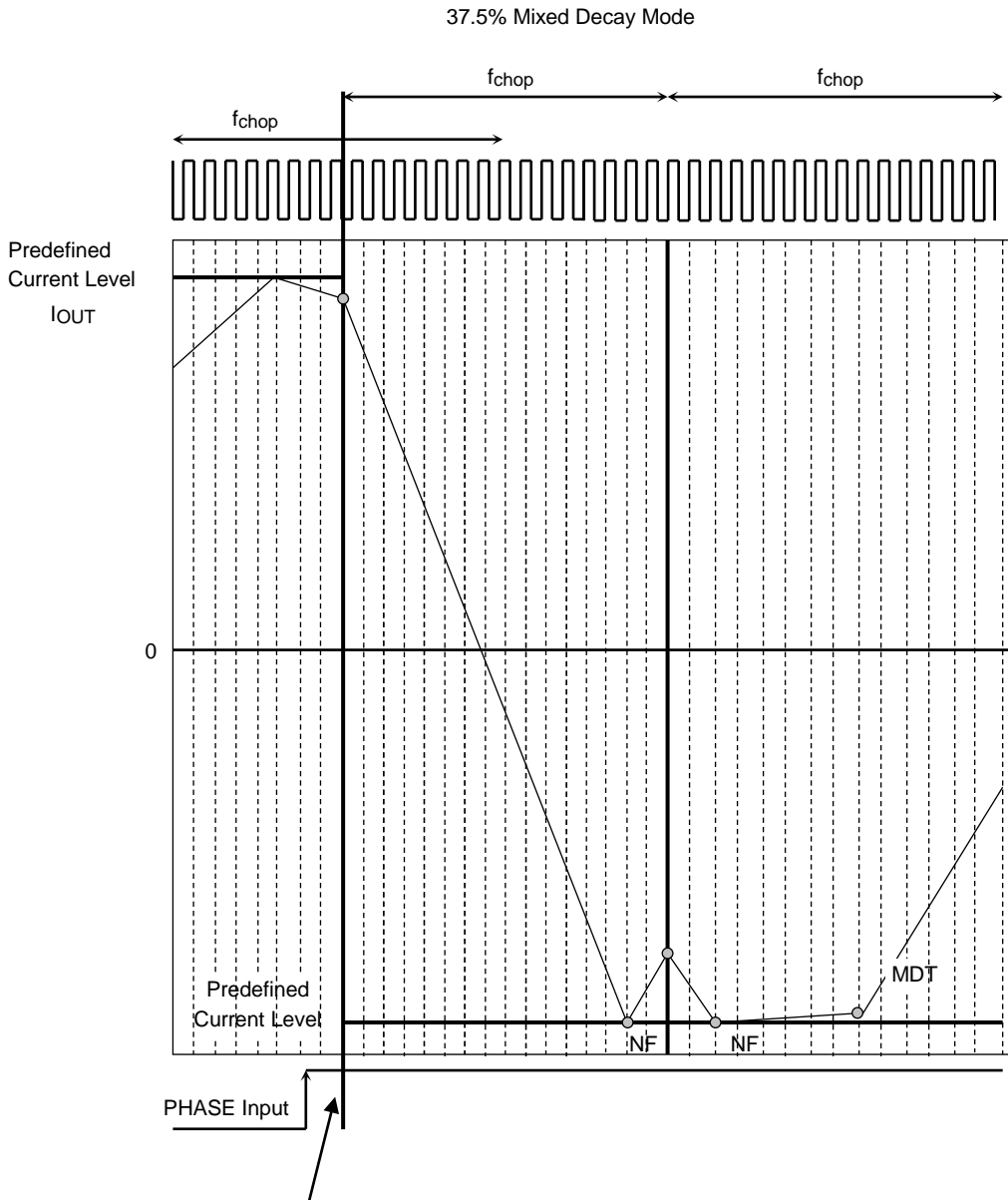


MDT (Mixed Decay Timing) Point: 37.5%

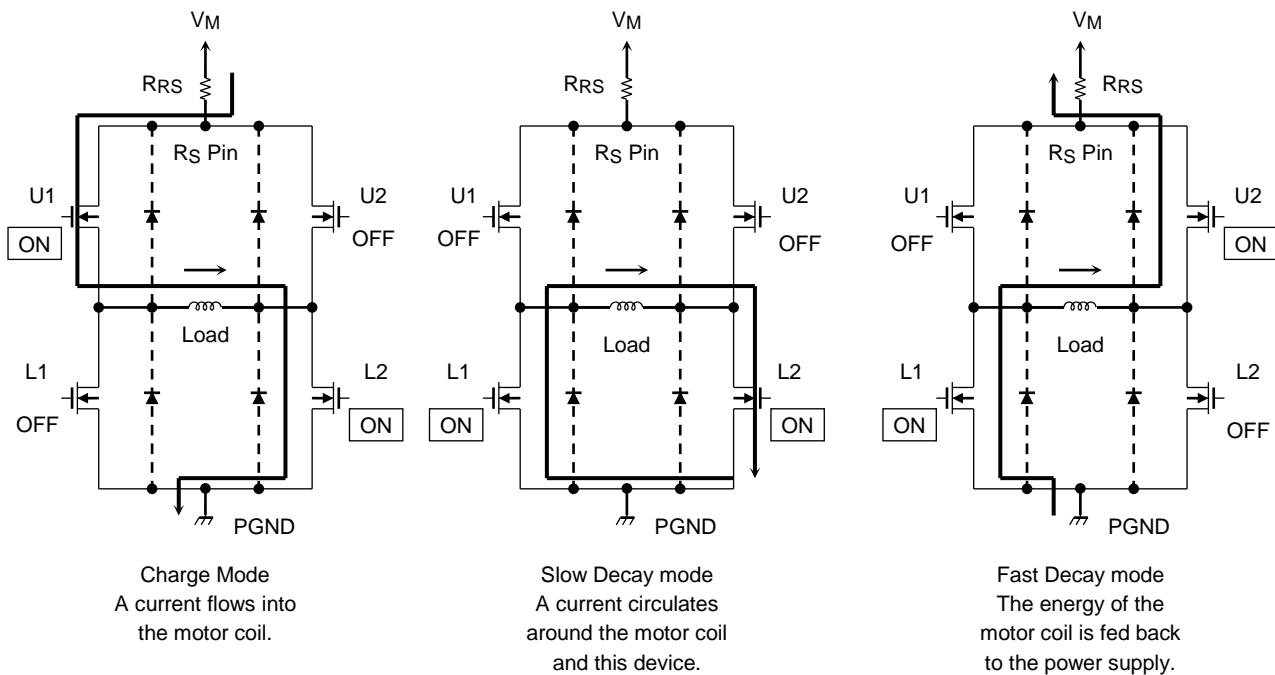
Timing charts may be simplified for explanatory purposes.

• Waveforms of Internal CR CLK and Output Signals (2-Phase Excitation Mode)

Timing charts may be simplified for explanatory purposes.



• Output Transistor Operating Modes



Output Transistor Operating Modes

| CLK | U1 | U2 | L1 | L2 |
|------------|-----|-----|-----|-----|
| Charge | ON | OFF | OFF | ON |
| Slow Decay | OFF | OFF | ON | ON |
| Fast Decay | OFF | ON | ON | OFF |

Note: This table shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following table.

| CLK | U1 | U2 | L1 | L2 |
|------------|-----|-----|-----|-----|
| Charge | OFF | ON | ON | OFF |
| Slow Decay | OFF | OFF | ON | ON |
| Fast Decay | ON | OFF | OFF | ON |

The TB62208FG switches among Charge, Slow Decay and Fast Decay modes automatically for constant-current control. The equivalent circuit diagrams are simplified or some parts of them may be omitted for explanatory purposes.

Calculation of the Predefined Output Current

For PWM constant-current control, the TB62208FG uses a clock generated by the CR oscillator. The peak output current can be set via the current-sensing resistor (R_{RS}) and the reference voltage (V_{ref}), as follows:

$$I_{out} = V_{ref} / 5 \div R_{RS} (\Omega)$$

where, $1/5$ is the V_{ref} decay rate, $V_{ref(GAIN)}$. For the value of $V_{ref(GAIN)}$, see the Electrical Characteristics table.

For example, when $V_{ref} = 3$ V, to generate an output current (I_{OUT}) of 0.8 A, R_{RS} is calculated as:

$$R_{RS} = (V_{ref} / 5) \div I_{out} = (3 / 5) \div 0.8 = 0.75 \Omega. (\geq 0.5 \text{ W})$$

IC Power Consumption

The power consumed by the TB62208FG is approximately the sum of the following two: 1) the power consumed by the output transistors, and 2) the power consumed by the digital logic and pre-drivers.

The power consumed by the output transistors is calculated, using the $R_{ON(D-S)}$ value of 1.5 Ω .

Whether in Charge, Fast Decay or Slow Decay mode, two of the four transistors comprising each H-bridge contribute to its power consumption at a given time.

Thus the power consumed by each H-bridge is given by:

$$P(\text{out}) = I_{\text{OUT}} (\text{A}) \times V_{\text{DS}} (\text{V}) = 2 \times I_{\text{OUT}}^2 \times R_{\text{ON}} \dots\dots\dots(1)$$

In two-phase excitation mode (in which two phases have a phase difference of 90°), the average power consumption in the output transistors is calculated as follows:

- $R_{\text{ON}} = 1.50 \Omega$ (@1.0 A)
- $I_{\text{OUT}} (\text{Peak: max}) = 1.0 \text{ A}$
- $V_{\text{M}} = 24 \text{ V}$

$$P(\text{out}) = 2 \times 1.0^2 (\text{A}) \times 1.50 (\Omega) = 3.0 (\text{W}) \dots\dots\dots(2)$$

The power consumption in the IM domain is calculated separately for normal operation and standby modes:

- Normal operation mode: $I(\text{IM3}) = 5.0 \text{ mA (typ.)}$
- Standby mode: $I(\text{IM1}) = 2.0 \text{ mA (typ.)}$

The current consumed in the digital logic portion of the TB62208FG is indicated as IMx. The digital logic operates off a voltage regulator that is internally connected to the VM power supply. It consists of the digital logic connected to V_{M} (24 V) and the network affected by the switching of the output transistors. The total power consumed by IMx can be estimated as:

$$P(\text{IM}) = 24 (\text{V}) \times 0.005 (\text{A}) = 0.12 (\text{W}) \dots\dots\dots(3)$$

Hence, the total power consumption of the TB62208FG is:

$$P = P(\text{out}) + P(\text{IM}) = 3.12 (\text{W})$$

The standby power consumption is given by:

$$P(\text{Standby}) = 24 (\text{V}) \times 0.002 (\text{A}) = 0.048 (\text{W})$$

Board design should be fully verified, taking thermal dissipation into consideration.

• Test Points for AC Specifications

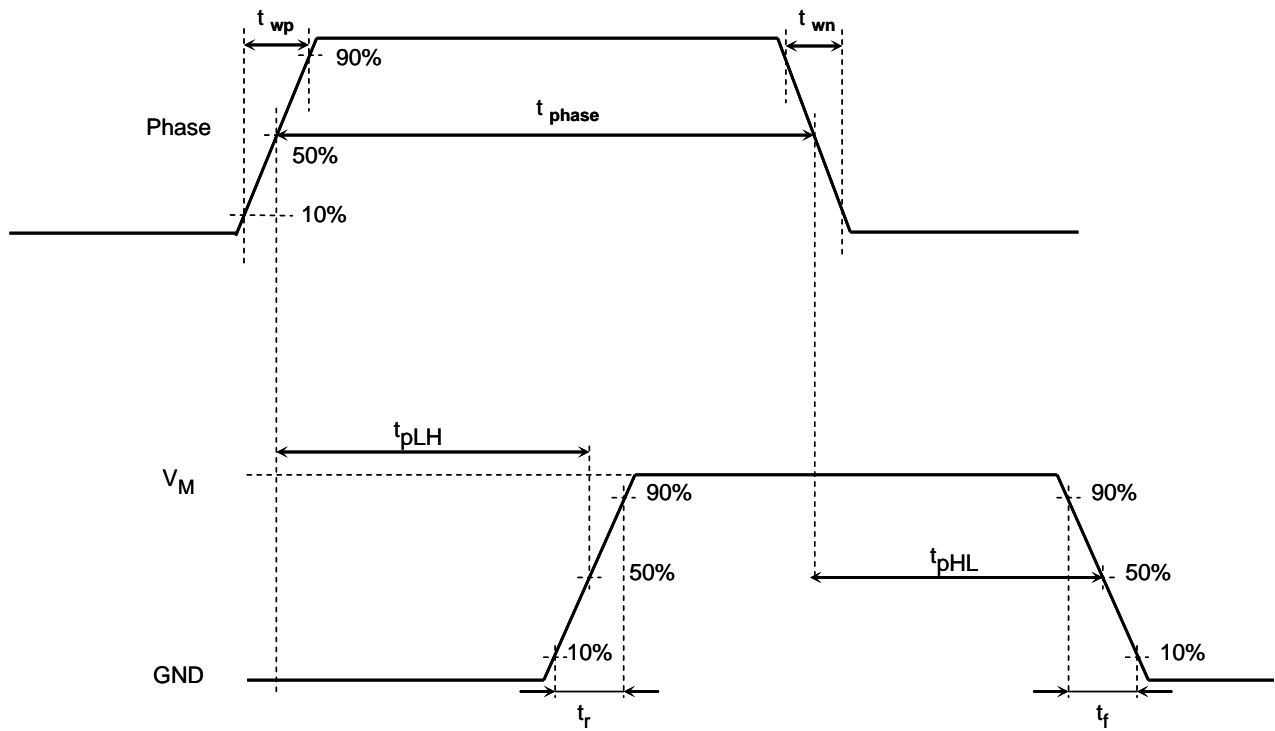


Figure 1 Timing Waveforms and Symbols

Timing charts may be simplified for explanatory purposes.

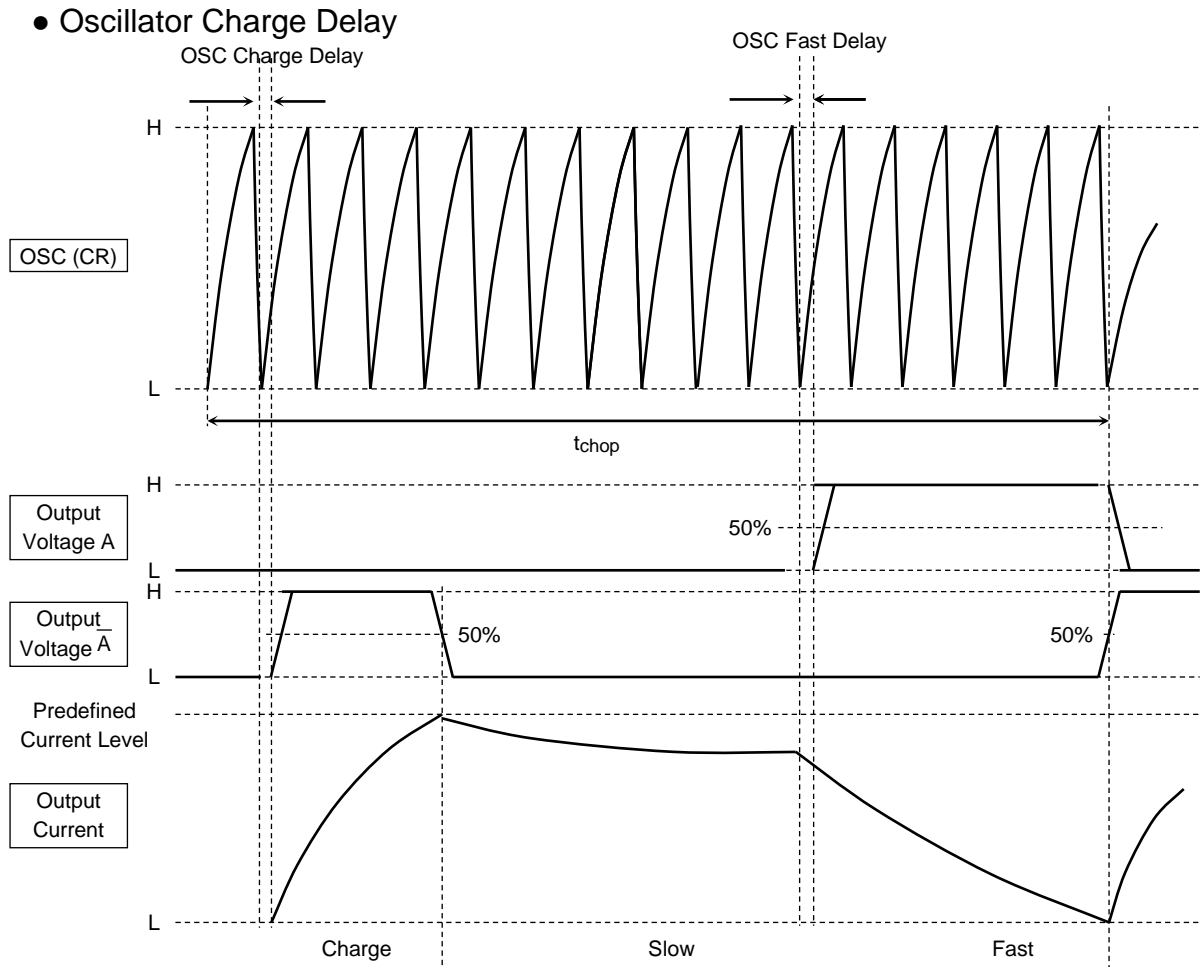
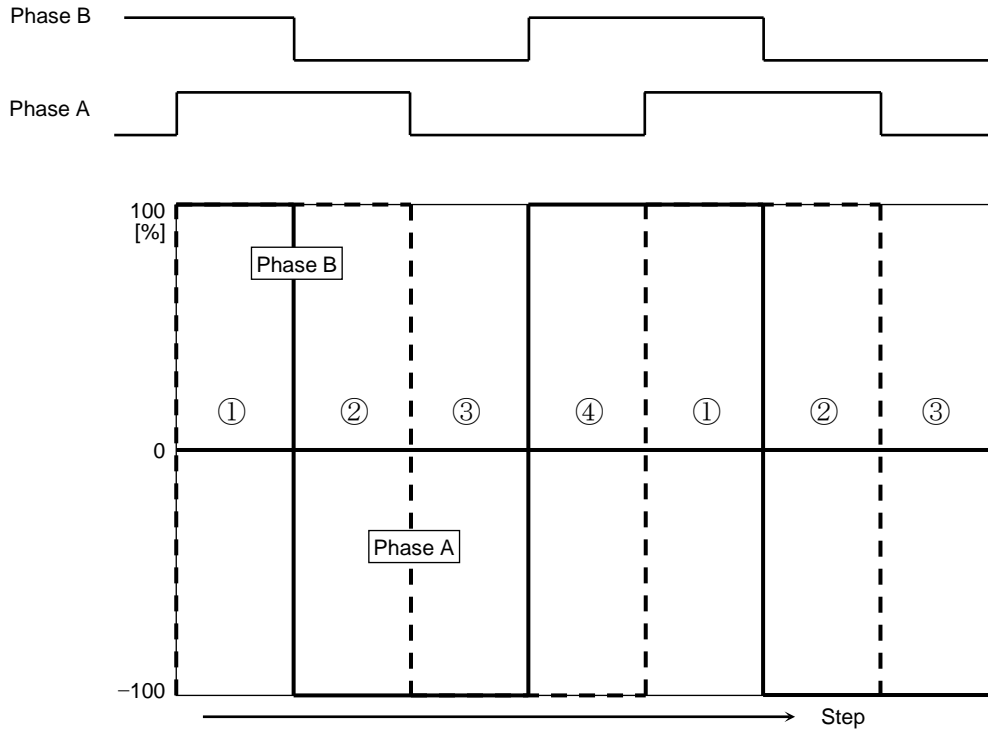


Figure 2 Mixed Decay Timing Waveforms

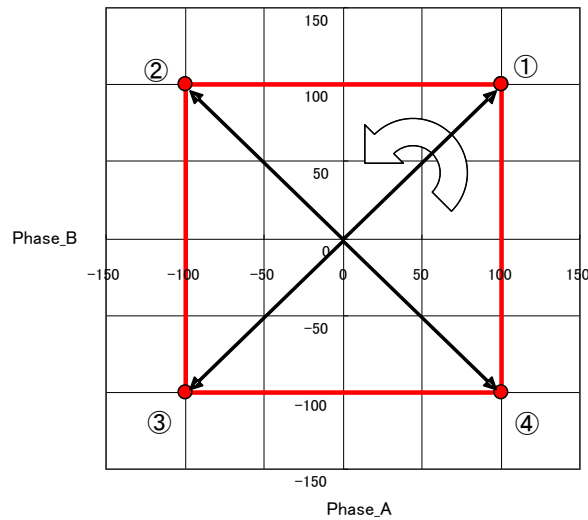
Phase Sequences

Two-Phase Excitation Mode

In two-phase excitation mode, the ENABLE input is held at logic High (except when the motor is off).

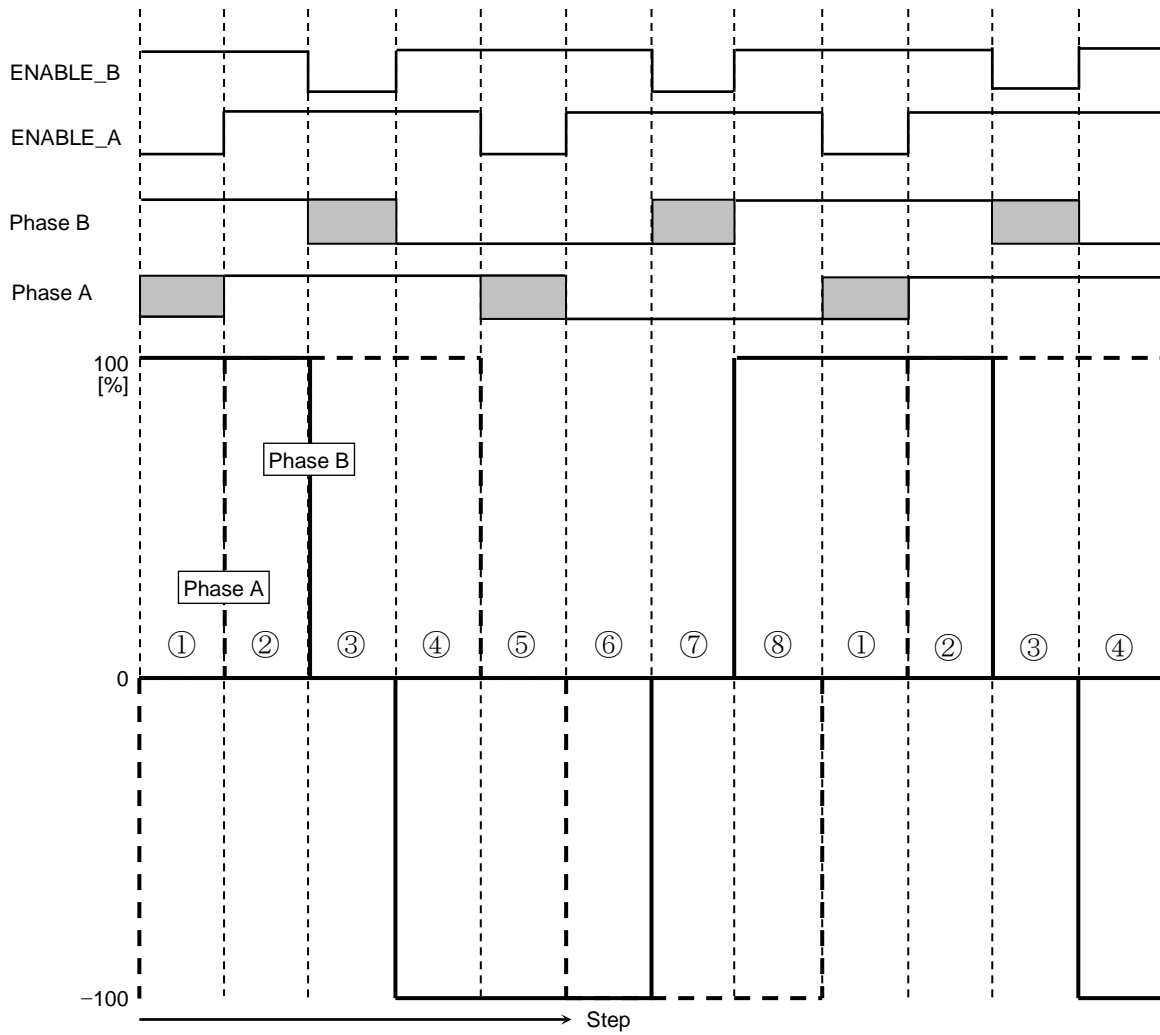


2-Phase Excitation Mode

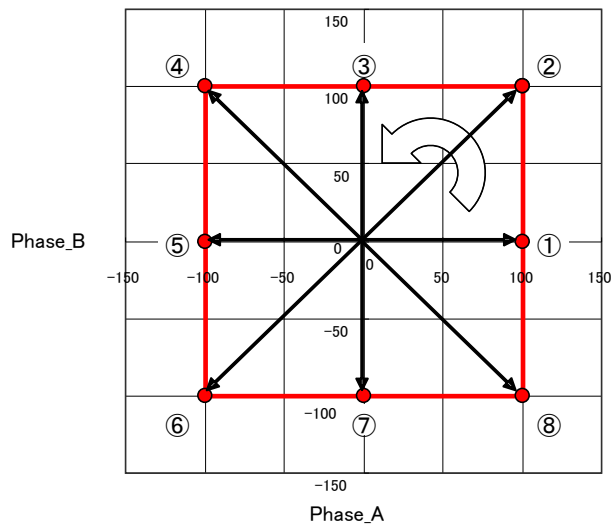


Note: The two-phase excitation mode is susceptible to significant load variations incurred by the motor back-EMF. In Slow Decay mode, a current swell caused by the motor back-EMF might not be cut down.

1-2-Phase Excitation Mode

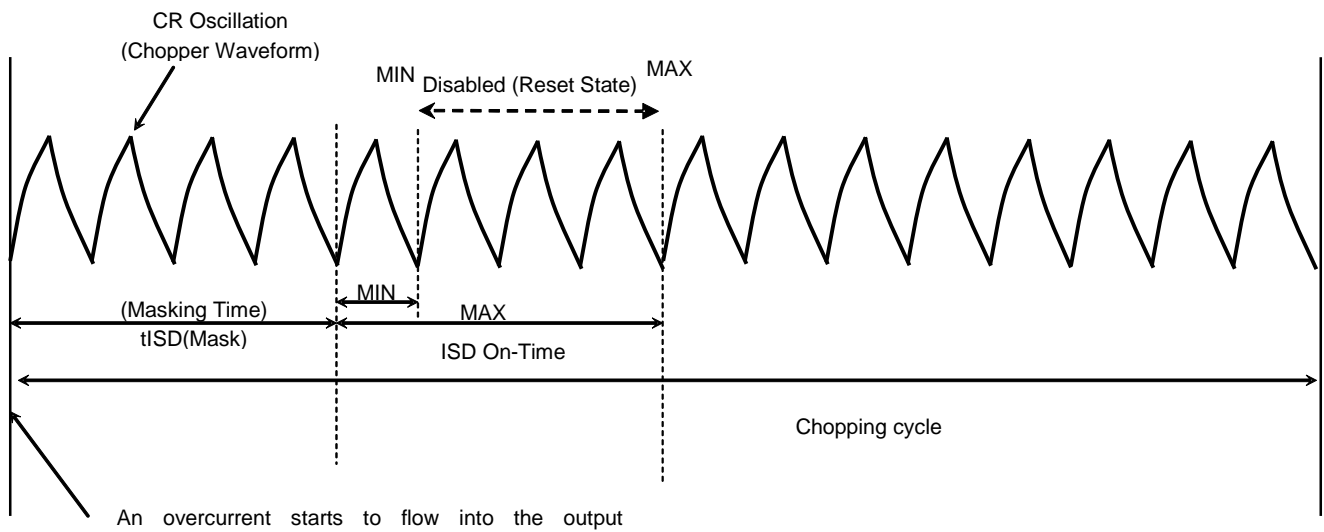


1-2-Phase Excitation Mode



Overcurrent Shutdown (ISD) Circuitry

ISD Masking Time and ISD On-Time



The overcurrent shutdown (ISD) circuitry has a masking time to prevent current spikes during I_{rr} and switching from erroneously tripping the ISD circuitry. The masking time is a function of the chopper frequency obtained by CR:

$$\text{masking time} = 4 \times \text{CR_frequency}$$

The minimum and maximum times taken to turn off the output transistors since an overcurrent flows into them are:

$$\text{Min: } 4 \times \text{CR_frequency}$$

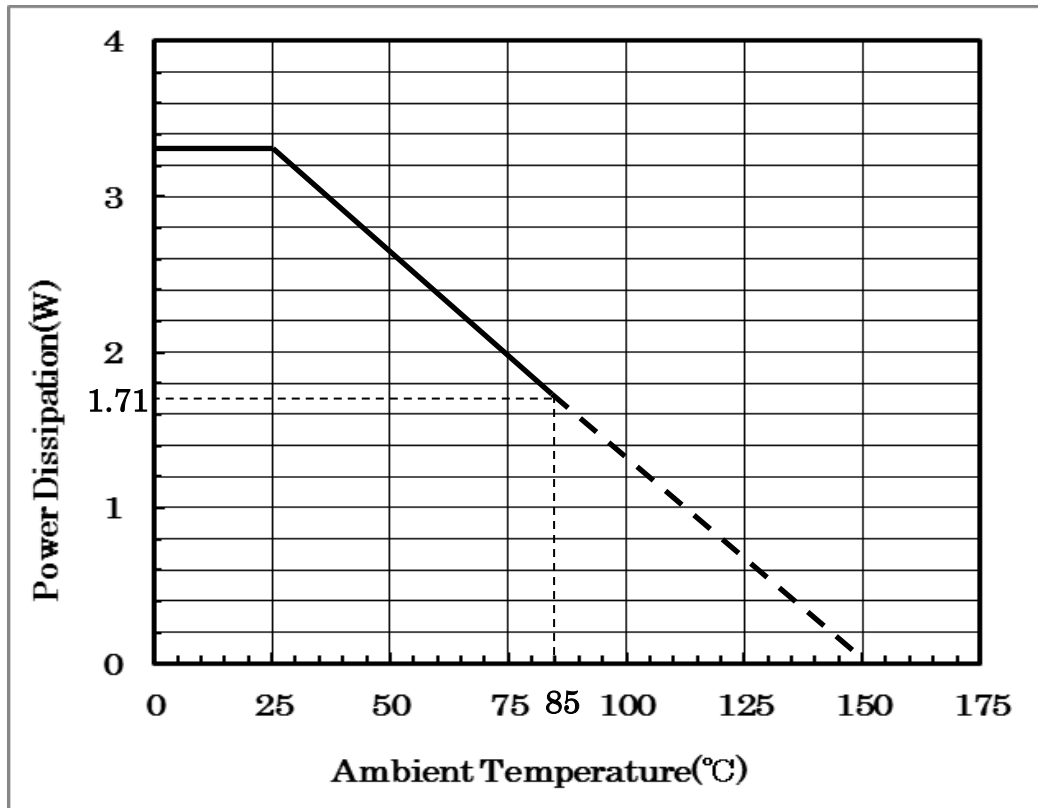
$$\text{Max: } 8 \times \text{CR_frequency}$$

It should be noted that these values assume a case in which an overcurrent condition is detected in an ideal manner. The ISD circuitry might not work, depending on the control timing of the output transistors.

Therefore, a protection fuse must always be added to the V_M power supply as a safety precaution. The optimal fuse capacitance varies with usage conditions, and one that does not adversely affect the motor operation or exceed the power dissipation rating of the TB62208FG should be selected.

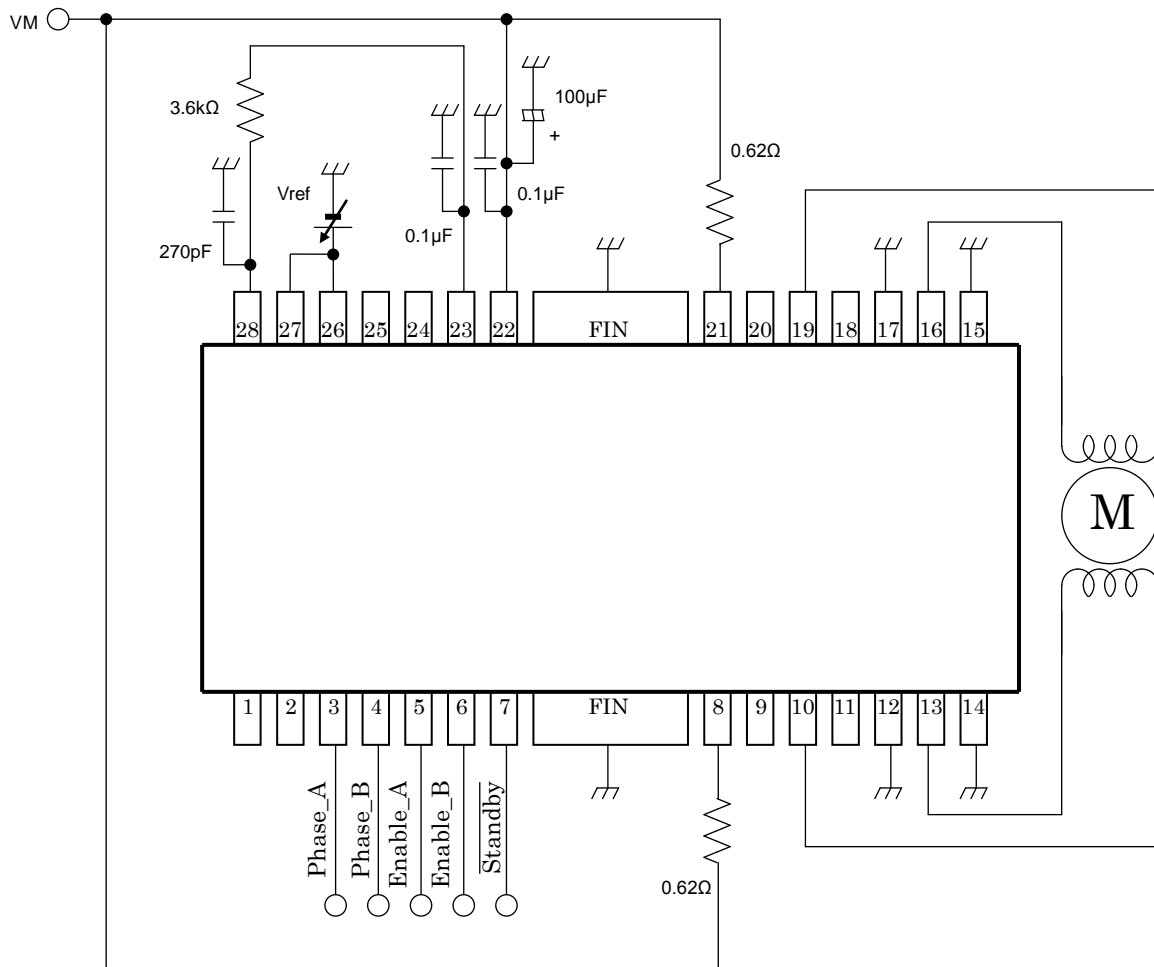
PD – Ta (Package Power Dissipation)

When mounted on a specialized board (140 mm × 70 mm × 1.6 mm: 38°C/W: typ.)



Application Circuit

The values shown in the following figure are typical values. For input conditions, see the "Operating Conditions" tables.



Note: Bypass capacitors should be added as necessary.

It is recommended to use a single ground plane for the entire board whenever possible, and an efficient grounding method should be considered for heat dissipation.

In cases where mode setting pins are controlled via switches, either pull-down or pull-up resistors should be added to them to avoid floating states.

For a description of the input values, see the "Output Function Table."

The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

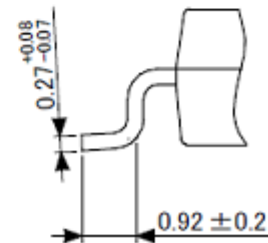
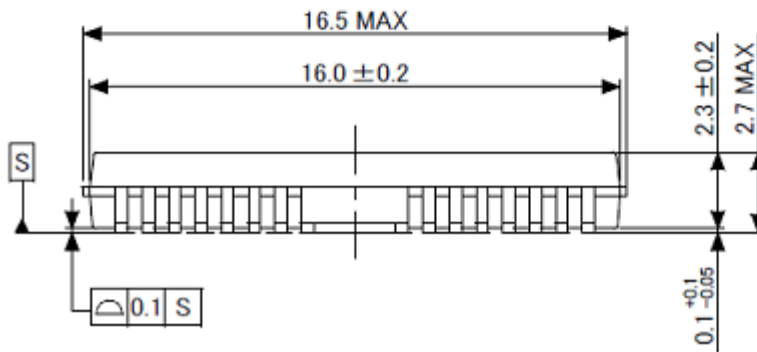
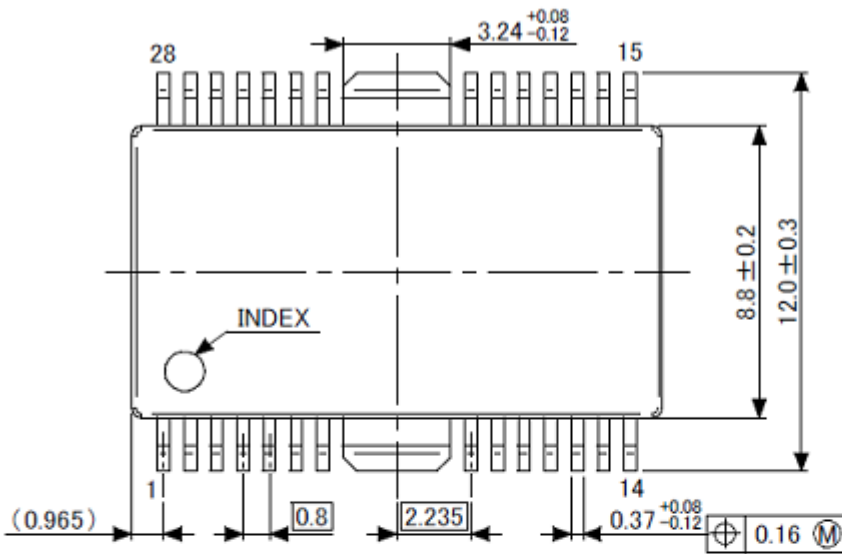
The external components in the above diagram are used to test the electrical characteristics of the device; it is not guaranteed that no system malfunction or failure will not occur.

Careful attention should be paid to the layout of the output, V_{DD} (V_M) and GND traces to avoid short-circuits across output pins or to the power supply or ground. If such a short-circuit occurs, the TB62208FG may be permanently damaged. Also, if the device is installed in a wrong orientation, a high voltage might be applied to components with lower voltage ratings, causing them to be damaged. The TB62208FG does not have an overvoltage protection circuit. Thus, if a voltage exceeding the rated maximum voltage is applied, the TB62208FG will be damaged; it should be ensured that it is used within the specified operating conditions.

Package Outline Dimensions

HSOP28-P-0450-0.80

Unit: mm



Weight: 0.79 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
- If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

- (1) Over current Protection Circuit
- Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
- Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.
- (2) Thermal Shutdown Circuit
- Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
- Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.
- (3) Heat Radiation Design
- In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- (4) Back-EMF
- When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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