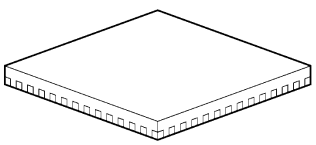
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB62216FTG

PWM Chopper-Type Motor Driver IC



QFN48-P-0707-0.50

Package weight: 0.14g (typ)

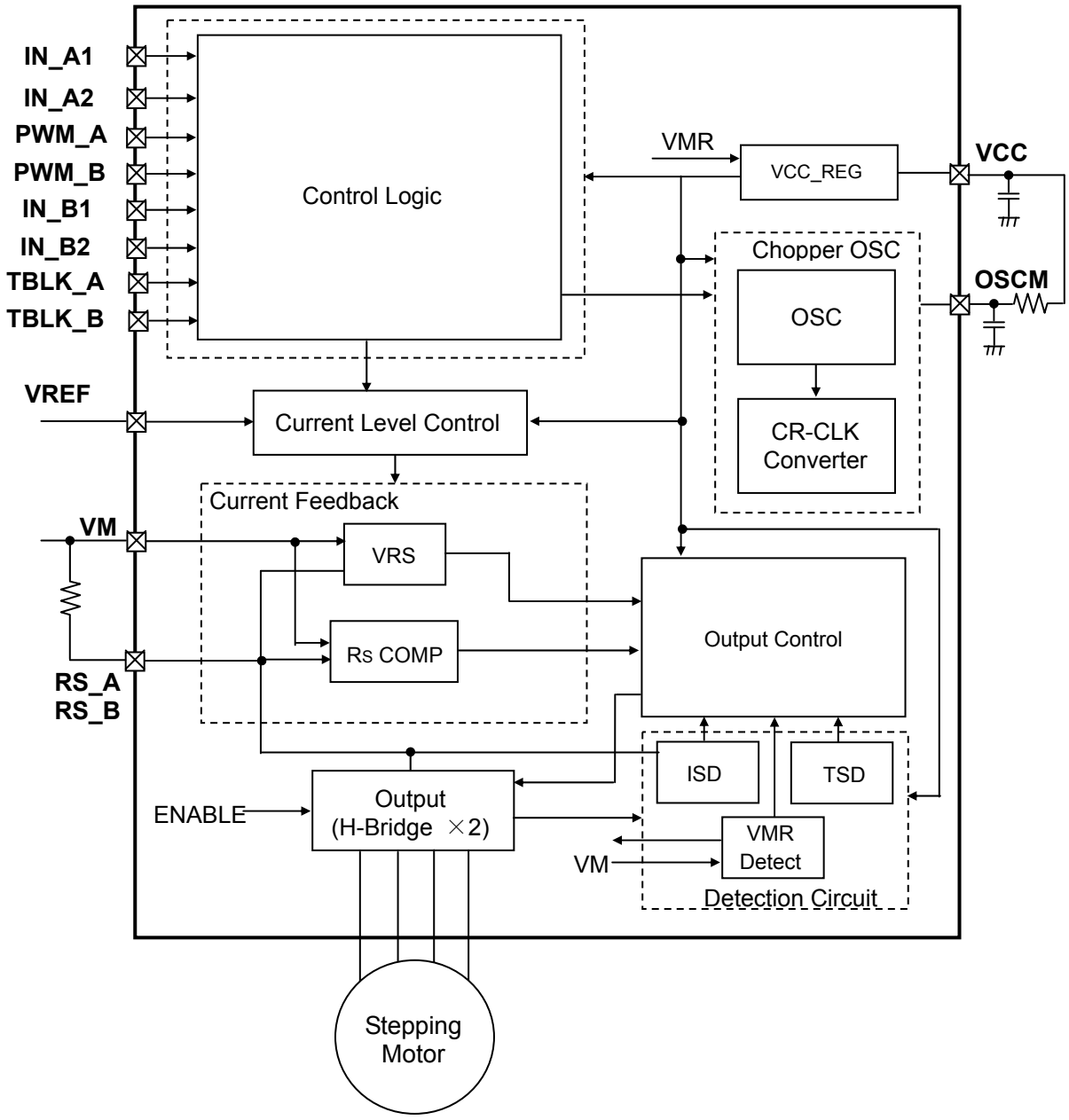
The TB62216FTG is a motor driver using internal PWM signals.
The TB62216FTG is capable of driving 2 DC brushed motors.
Fabricated with the BiCD process, the TB62216FTG is rated at 40V/2.5A.
The internal voltage regulator allows control of the motor with a single VM power supply.

Features

- Monolithic IC by using BiCD process
- PWM controlled constant-current drive
- Low on-resistance of output stage transistor is low by using BiCD process.
- High Voltage and current (For specification, please refer to absolute maximum ratings and operation ranges)
- Thermal shutdown (TSD)、over-current shutdown (ISD), abnormally current detection (VRS) and power-on reset (POR)
- Built-in regulator allows the TB62216FTG to function with only VM power supply.
- Able to customize PWM signal frequency by external condenser.
- Package: QFN48-P-0707-0.50

Note) Please be careful about thermal conditions during use.

Block Diagram



* Please note that in the block diagram, functional blocks or constants may be omitted or simplified for explanatory purposes.

Notes:
All the grounding wires of the TB62216FTG must run on the solder within the mask of the PCM. It must also be externally terminated at a single point. Also, the grounding method should be considered for efficient heat dissipation.

Logic input pins must be correctly wired. While using switches to control input levels, make sure to pull up to VCC or pull down to GND to avoid high impedance.

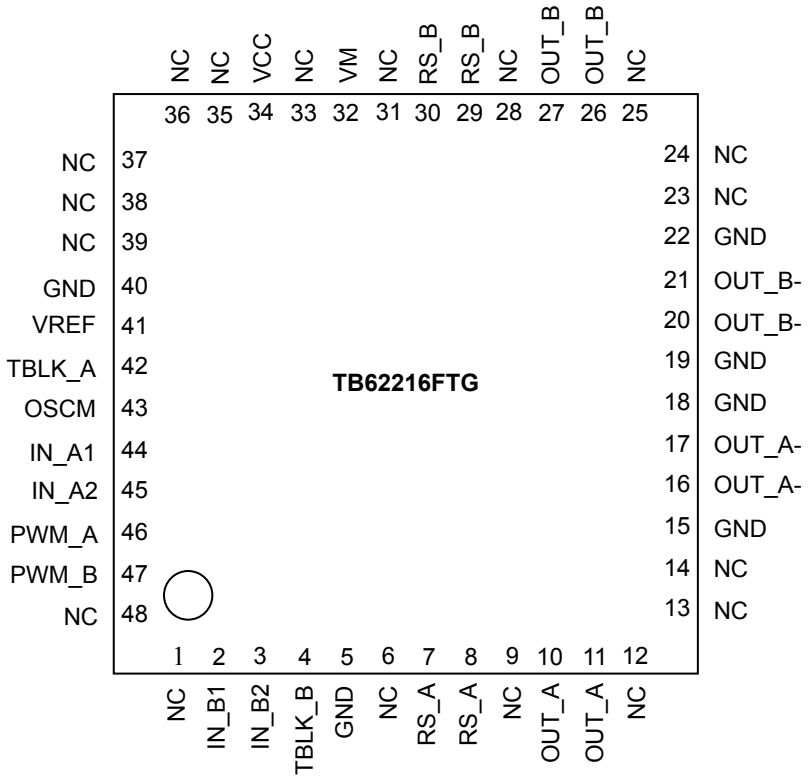
Please take extra care while tracing the layout of the VM, GND and output patterns to avoid shortage across output, GND or power supplies. If such shortage occurs, the TB62216FTG may be permanently damaged.

The utmost care should also be taken for pattern designing and implementation of the TB62216FTG. If power-relevant pins such as VM, RS, OUT, and GND (which is capable of running particularly large current) are wired incorrectly, an operation error may occur or the TB62216FTG may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the TB62216FTG may be damaged by a current larger than the specified current running through the IC.

Pin assignment (TB62216FTG)

(Top View)



Pin Function

TB62216FTG (QFN48)

Function explanation

Pin No.	Pin Name	Function		Pin No.	Pin Name	Function
1	NC	Not connected		25	NC	Not connected
2	IN_B1	Bridge B excitation control input		26	OUT_B	Bridge B + output
3	IN_B2	Bridge B excitation control input		27	OUT_B	Bridge B + output
4	TBLK_B	Bridge B Digital tBLK input		28	NC	Not connected
5	GND	Ground pin for Logic input		29	RS_B	Bridge B sense output
6	NC	Not connected		30	RS_B	Bridge B sense output
7	RS_A	Bridge A sense output		31	NC	Not connected
8	RS_A	Bridge A sense output		32	VM	Motor Voltage supply
9	NC	Not connected		33	NC	Not connected
10	OUT_A	Bridge A + output		34	VCC	Internal regulator voltage monitor
11	OUT_A	Bridge A + output		35	NC	Not connected
12	NC	Not connected		36	NC	Not connected
13	NC	Not connected		37	NC	Not connected
14	NC	Not connected		38	NC	Not connected
15	GND	Ground pin for Bridge A		39	NC	Not connected
16	OUT_A-	Bridge A – output		40	GND	Ground pin for Logic input
17	OUT_A-	Bridge A – output		41	VREF	Current customize for Bridge A and B
18	GND	Ground pin for Bridge A		42	TBLK_A	Bridge A Digital tBLK input
19	GND	Ground pin for Bridge B		43	OSCM	Oscillator pin for internal PWM signal
20	OUT_B-	Bridge B - output		44	IN_A1	Bridge A excitation control input
21	OUT_B-	Bridge B - output		45	IN_A2	Bridge A excitation control input
22	GND	Ground pin for Bridge B		46	PWM_A	Bridge A short brake input
23	NC	Not connected		47	PWM_B	Bridge B short brake input
24	NC	Not connected		48	NC	Not connected

・Please do not connect any pattern to the NC pin.

・Please connect the pins with the same names, at the nearest point of the device.

Logic Input Function Table

(1) IN_A1, IN_A2 (Bridge A Controller)
Setting the drive mode of Bridge A

	PWM_A	IN_A1	IN_A2	OUT_A	OUT_A-	Function
INPUT	L	L	L	OFF (High impedance)	OFF (High impedance)	STOP(OFF)
	H					
	L	L	H	L	L	Short brake
	H			L	H	CCW
	L	H	L	L	L	Short brake
	H			H	L	CW
	L	H	H	L	L	Short brake
	H					

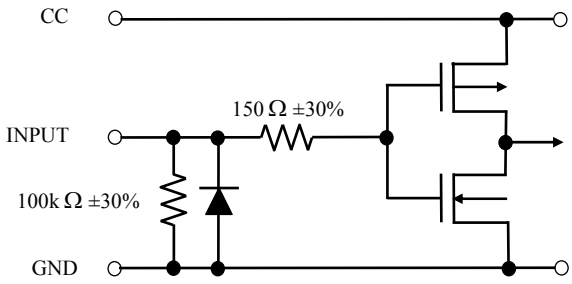
(2) IN_B1, IN_B2 (Bridge B Controller)
Setting the drive mode of Bridge B

	PWM_B	IN_B1	IN_B2	OUT_B	OUT_B-	Function
INPUT	L	L	L	OFF (High impedance)	OFF (High impedance)	Stop(OFF)
	H					
	L	L	H	L	L	Short brake
	H			L	H	CCW
	L	H	L	L	L	Short brake
	H			H	L	CW
	L	H	H	L	L	Short brake
	H					

(3) TBLK_A,B (Digital tBLK Controller)
Setting the noise reject timer

Name	Function	Input	Note
TBLK_A,B	Digital tBLK (Noise Reject timer)	Low	OSCM*4clk
		High	OSCM*6clk

Equivalent Input Circuit

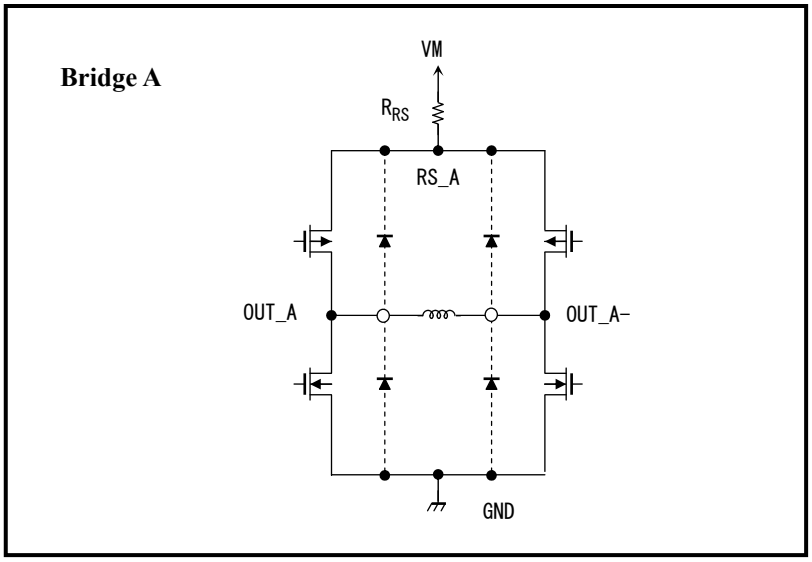


INPUT
IN_A1
IN_A2
IN_B1
IN_B2
PWM_A
PWM_B
TBLK_A
TBLK_B

Please note that in the equivalent input circuit, functional blocks or constants may be omitted or simplified for explanatory purposes.

■The example of combination of H-SW in each motor drive mode (the H-SW Connection)

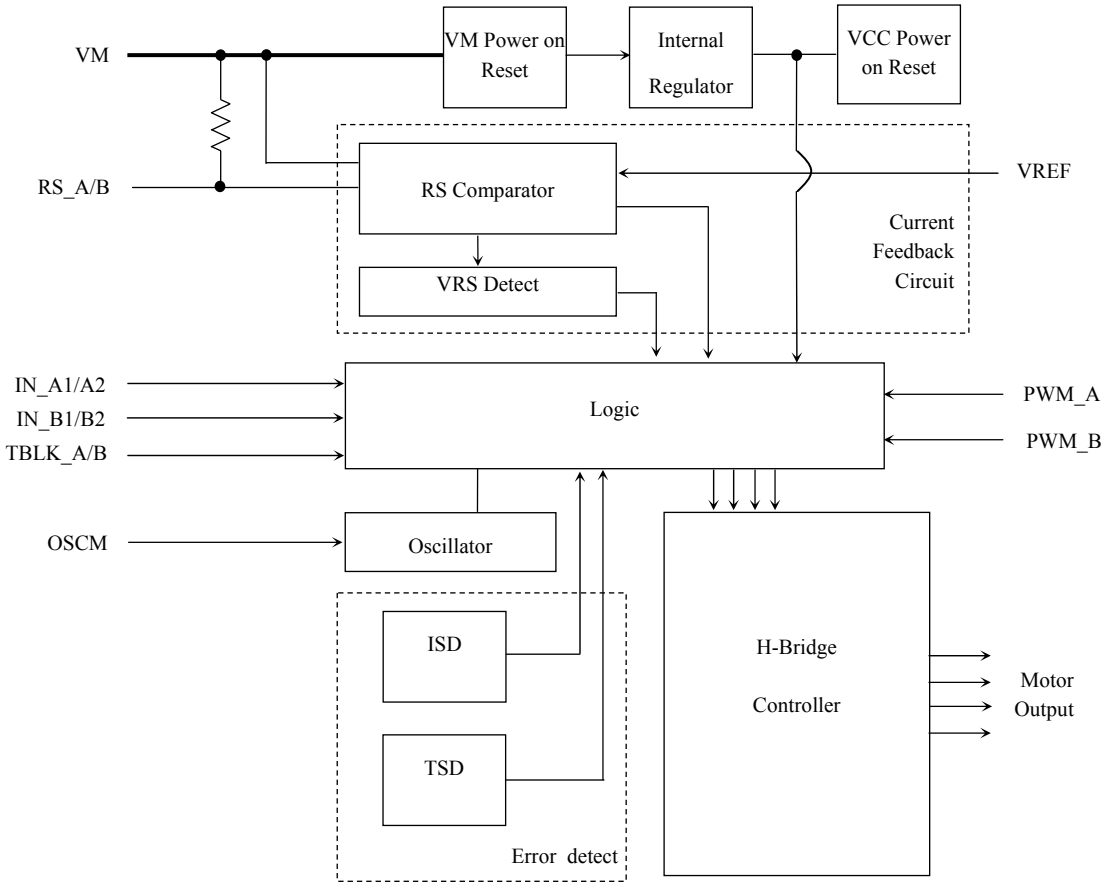
●Connection example for 1 DC Motor



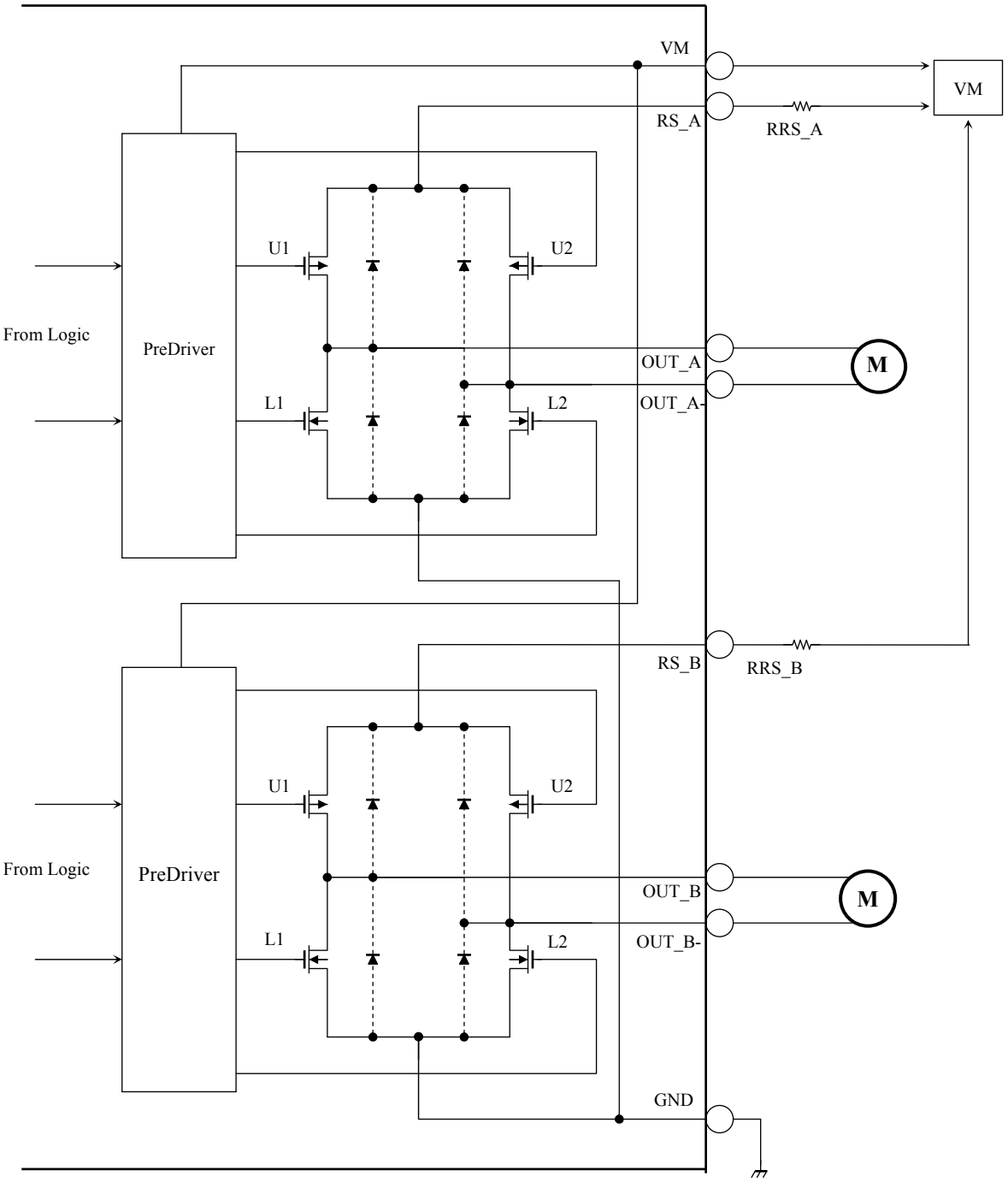
Please note that the functional blocks or constants may be omitted or simplified for explanatory purposes.

・Current feedback and current level set circuits

Note: Logic input pins are pulled down by 100kΩ internally; be sure to short unused logic pins to GND to avoid operation error.



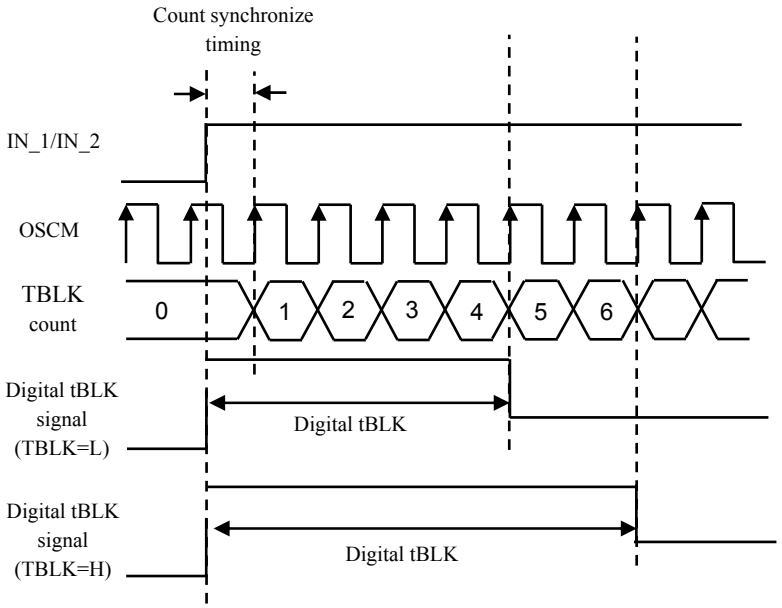
Equivalent Output Circuit (Bridge A, B)



Please note that the functional blocks or constants may be omitted or simplified for explanatory purposes.

1. Digital tBLK Function

TBLK	Blanking time
L	Digital tBLK = OSCM×4clk
H	Digital tBLK = OSCM×6clk

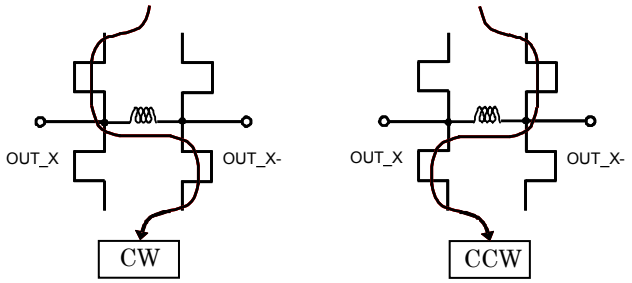


Please note that the timing charts or constants may be omitted or simplified for explanatory purposes.

The digital tBLK is used to avoid error judgment of varistor recovery current that occurs in charge drive mode when H-bridges are used with DC motors. The digital tBLK time can be controlled through TBLK_A and TBLK_B pins.
By setting digital tBLK, direct PWM control and constant-current control is possible, but the motor current will rise above the predefined current level (NF) while digital tBLK is active.
Besides digital tBLK, analog tBLK settled by an internal constant of IC is also attached.

2. DC Motor Control Signal Function

	PWM_A	IN_A1	IN_A2	OUT_A	OUT_A-	Function
INPUT	L	L	L	OFF (High impedance)	OFF (High impedance)	STOP(OFF)
	H					
	L	L	H	L	L	Short brake
	H			L	H	CCW
	L	H	L	L	L	Short brake
	H			H	L	CW
	L	H	H	L	L	Short brake
	H					



Please note that the functional blocks or constants may be omitted or simplified for explanatory purposes.

● Absolute Maximum Ratings (Ta=25°C)

Characteristics	Symbol	Rating	Unit	Note
Motor power supply	VM	40	V	
Motor output voltage	V_{OUT}	40	V	
Motor output current	I_{OUT}	2.5	A	* 1: per 1 H-SW
	I_{OUT}(peak)	5.0	A	*2: (tw≤500ns)
RS pin voltage	VRS	VM ± 4.5	V	
Logic power supply	VCC	6	V	
Logic input voltage	VIN	-0.4 to 6.0	V	*3
VREF reference voltage	VREF	GND to 4.2V	V	
Power dissipation	PD	1.3	W	*4
Operating temperature	Topr	−20 to 85	°C	
Storage temperature	Tstg	−55 to 150	°C	
Junction temperature	Tj	150	°C	

*1: Motor output current is per 1 H-SW. While in use, please make sure that the motor current is controlled to be under 80 % of the absolute maximum ratings. (In this case, about 2.0A (max) per 1 H-SW).
*2: Motor output current peak width must be less than 500ns
*3: Logic input voltage must be input less than 6.0V
*4: The value in the state where it is not mounted on the board
Ta: Ambient temperature.
Topr: Operating ambient temperature.
Tj: Operating junction temperature. The maximum junction temperature is limited by the thermal shutdown.

Note: The absolute maximum ratings

The absolute maximum ratings are a specification that must not be exceeded, even for a moment.
Exceeding the ratings may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Operating Ranges (Ta=0 to 85°C)

Characteristics	Symbol	Note	Min	Typ	Max	Unit
Motor power supply	VM		10	24	38	V
Motor output current	I_{OUT}	Ta=25°C, per 1 H-SW	−	1.2	2.0	A
	I_{OUT}(peak)	(tw≤500ns)	-	1.2	4.0	A
Logic input voltage	VIN(H)	Logic [High] level	2.0	3.3	5.5	V
	VIN(L)	Logic [Low] level	GND	-	0.8	V
PWM signal frequency	fchop	VM=24V	40	100	150	kHz
VREF reference voltage	VREF	VM=24V	GND	3.0	4.0	V

Note: Use the maximum junction temperature (Tj) at 120°C or less.
The maximum current cannot be used under certain thermal conditions.

Electrical Specifications 1 (Ta=25°C, VM=24V, unless specified otherwise)

Characteristics		Symbol	Test condition	Min	Typ	Max	Unit
Logic input voltage	High	VIN(H)	Logic input pins	2.0	—	5.4	V
	Low	VIN(L)		GND -0.4	GND	0.8	
Logic input hysteresis voltage		Hys	Logic input pins	0.1	0.2	0.3	V
Logic input current		IIN(H)	VIN(H)	—	50	70	μA
		IIN(L)	VIN(L)	—	—	1.0	
Power consumption		IM	Outputs: open IN_A1/A2/B1/B2:L fchop=100kHz Output off	—	5.0	7.0	mA
Output leakage current	High-side	IOH	VRS=VM=24V, Vout=0V, (IN_A1,IN_A2)=(L,L) (IN_B1,IN_B2)=(L,L)	−1	—	—	μA
	Low-side	IOL	VRS=VM=Vout=24V, (IN_A1,IN_A2)=(L,L) (IN_B1,IN_B2)=(L,L)	—	—	1	μA
Bridge-to-Bridge current differential		⊿Iout1	Bridge A,B current differential, Iout=2.0A	−5	—	5	%
Output current error relative to the predetermined value		⊿Iout2	Iout=2.0A	−5	—	5	%
RS pin voltage		⊿VRS	-	0	0.6	0.8	V
RS pin current		IRS	VM=VRS=24V IN_A1/A2/B1/B2:L	—	—	10	μA
Drain-source ON-resistance (The sum of high side & low side)		Ron(D-S)	Iout=2.0A, Tj=25°C	—	1.0	1.5	Ω

Electrical Specifications 2 (Ta=25°C, VM=24V, unless specified otherwise)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Internal regulator voltage	VCC	ICC=5.0mA	4.75	5.0	5.25	V
Internal regulator current	ICC	-	-	2.5	5.0	mA
VREF input voltage	VREF	VM=24V, Output: OFF	GND	3.0	4.0	V
VREF input current	IREF	VREF=3.0V, Output: ON	0	—	10	μA
VREF gain rate	VREF(gain)	VREF=3.0V, Output: ON	1/5.3	1/5.1	1/4.9	—
TSD threshold	Tj TSD	(Note 1)	140	150	160	°C
VCC power on reset voltage	VCCPOR	VM=24V	2.0	3.0	4.0	V
VM power on reset voltage	VMPOR		6.0	-	8.0	V
Over current threshold	ISD	Fchop=100kHz (Note 2)	2.6	3.6	4.6	A
Over voltage threshold	VRS det	VM-RS pin voltage	0.9	1.5	-	V

Note 1: Thermal shutdown (TSD) circuit
When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. The TSD circuit threshold is between 140 °C (min) and 160 °C (max). Once the TSD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted.

Note 2: Over-current/voltage shutdown (ISD/VRS) circuit
When the output current or the RS pin voltage reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted. For fail-safe, please insert a fuse to avoid secondary trouble.

AC Electrical Specifications (Ta=25°C, VM=24V, 6.8mH+5.7Ω)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Logic input frequency	f_{Logic}	f_{OSCM}=1600kHz	−	−	200	kHz
Minimum phase pulse width	tw(tLogic)	−	100	−	−	ns
	twp		50	−	−	
	twn		50	−	−	
Output transistor switching characteristics	tr	-	−	0.2	−	µs
	tf		−	0.2	−	
	tpLH(IN_X)	Phase to OUT	−	1	−	
	tpHL(IN_X)		−	1.5	−	
	tpLH(OSC)	OSC to OUT	−	0.5	−	
	tpHL(OSC)		−	1	−	
Analog blanking time for current spike elimination	AtBLK	Iout=0.6A,VM=24V Analog tBLK	250	400	550	ns
Digital blanking time for current spike elimination	DtBLK(L)	TBLK:L, f_{OSCM}=1600kHz Digital tBLK	-	2.5	-	µs
	DtBLK(H)	TBLK:H, f_{OSCM}=1600kHz Digital tBLK	-	3.75	-	µs
OSC oscillation reference frequency	fOSCM	C＝270pF, R=3.6kΩ	1.2	1.6	2.0	MHz
Chopping frequency	fchop	f_{OSCM}=1.6MHz	−	100	−	kHz

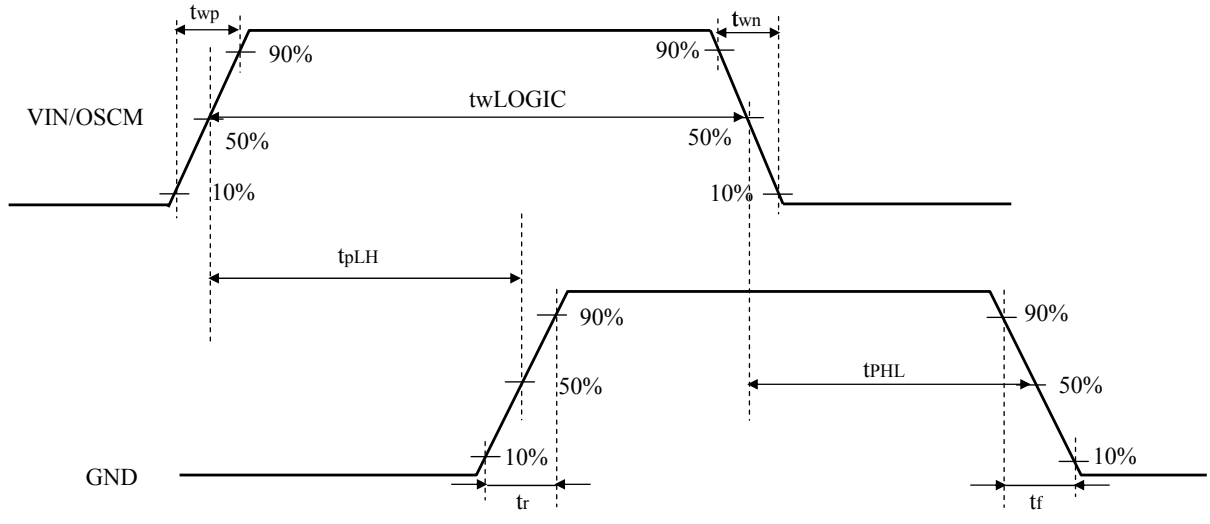


Fig.1 Timing Charts of Input Phase Signal and Output Transistor Switching

Timing charts may be simplified for explanatory purpose.

Calculation of the Predefined Output Current

The peak output current can be set via the current-sensing resistor (RRS) and the reference voltage (VREF), as follows:

$$I_{OUT} = \frac{VREF \times VREF(gain)}{RRS}$$

VREF (gain) is Vref reduction rate that is a fixed value of 1/5.1. For example, to calculate the motor output current threshold:

$$I_{OUT} = \frac{3.0(V) \times 1/5.1}{0.51(\Omega)} = 1.15(A)$$

1/5.1 is the VREF gain rate. For the value of VREF gain rate, see the Electrical Characteristics Table.

Calculation of the chopping frequency

The chopping frequency is 1/16 of f_{OSCM}. When f_{OSCM} is 1600 kHz, the chopping frequency is as follows:

fchop = f_{OSCM} / 16 = 1600/16 = 100 (kHz)

IC Power Consumption

The power consumed by the TB62216FTG is approximately the sum of the following:
(1) the power consumed by the output transistors
(2) the power consumed by the digital logic and pre-drivers.

(1) The power consumed by the output transistors is calculated, using the R_{ON} (D-S) value of 1.0 Ω .

Whether in Charge, Fast Decay or Slow Decay mode, two of the four transistors comprising each H-bridge contribute to its power consumption at a given time.

Thus the power consumed by each H-bridge is given by:

$$P\ OUT=H\text{-}Bridge(ch)\times I_{OUT}(A)\times VDS(V)= 1\times I_{OUT}{}^{2}\times RON \quad \ldots\ldots (1)$$

In two-phase excitation mode (in which two phases have a phase difference of 90°), the average power consumption in the output transistors is calculated as follows:

$RON=1.0\ \Omega$
I_{OUT}(peak:typ)=1.0A

$$P\ OUT=1(\ ch\ )\times 1.0^{2}(A)\times 1.0(\ \Omega\ )=1.0(W) \quad \ldots\ldots (2)$$

(2) The power consumption in the IM domain is calculated separately for normal operation and standby modes:

Normal operation mode: IM=5.0mA (typ.)

The current consumed in the digital logic portion of the TB62216FTG is indicated as IM. The digital logic operates off a voltage regulator internally connected to the VM power supply. It consists of the digital logic connected to VM(24V) and the network affected by the switching of the output transistors. The total power consumed by IM can be estimated as:

$$P\ IM=24(V)\times 0.005(A)=0.12(W) \quad \ldots\ldots (3)$$

3)The total power consumption of the TB62216FTG

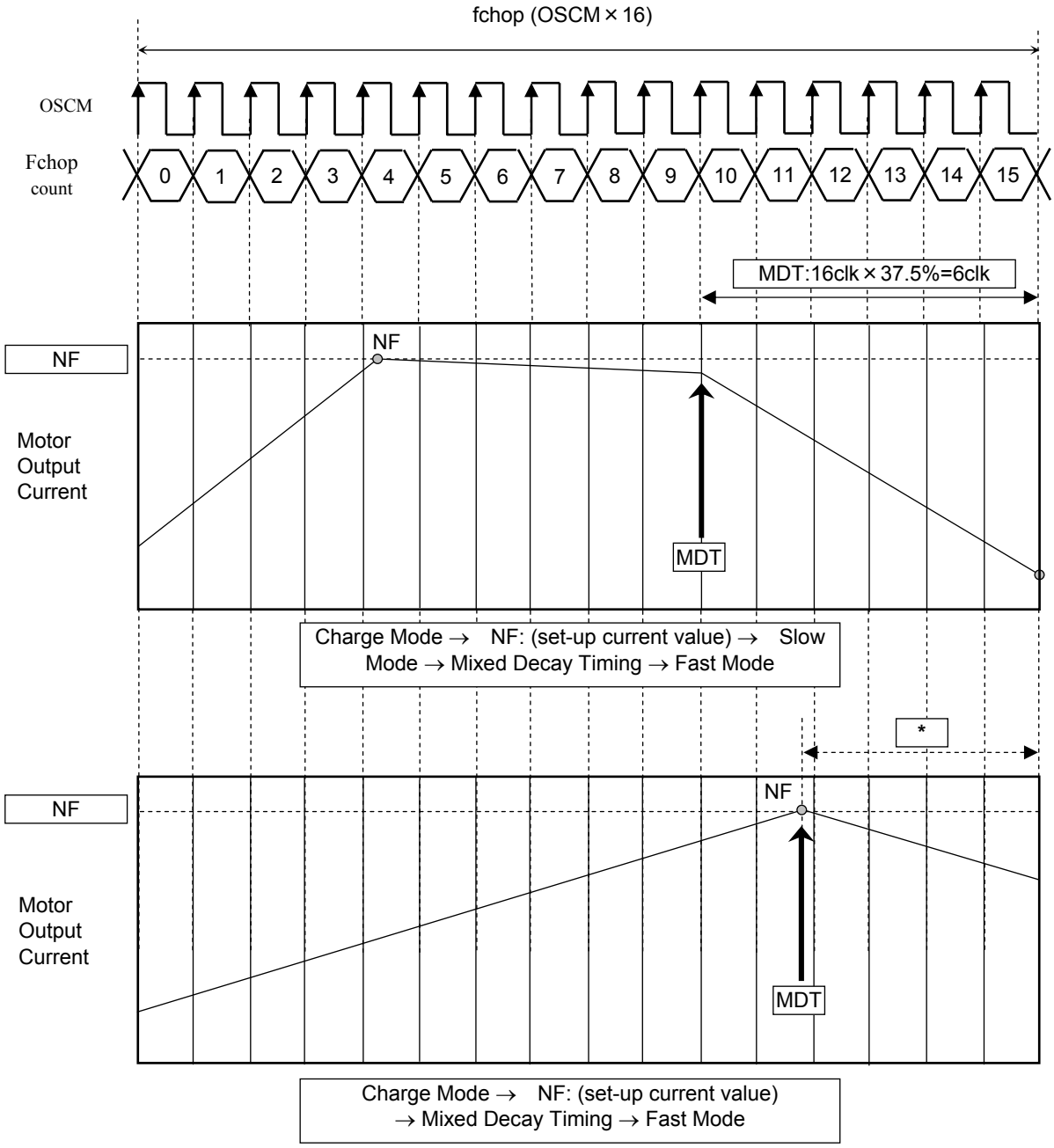
From the result of the two above-mentioned formulas

$$P=P\ OUT+P(IM)=1.12(W)$$

Board design should be fully verified, taking thermal dissipation into consideration.

Current figures of Mixed Decay Mode

The regeneration after reaching setup current is controlled in the order of Fast->Slow (fast decay → slow decay).
The timing from fast regeneration to slow regeneration is 37.5% fixation of fchop.

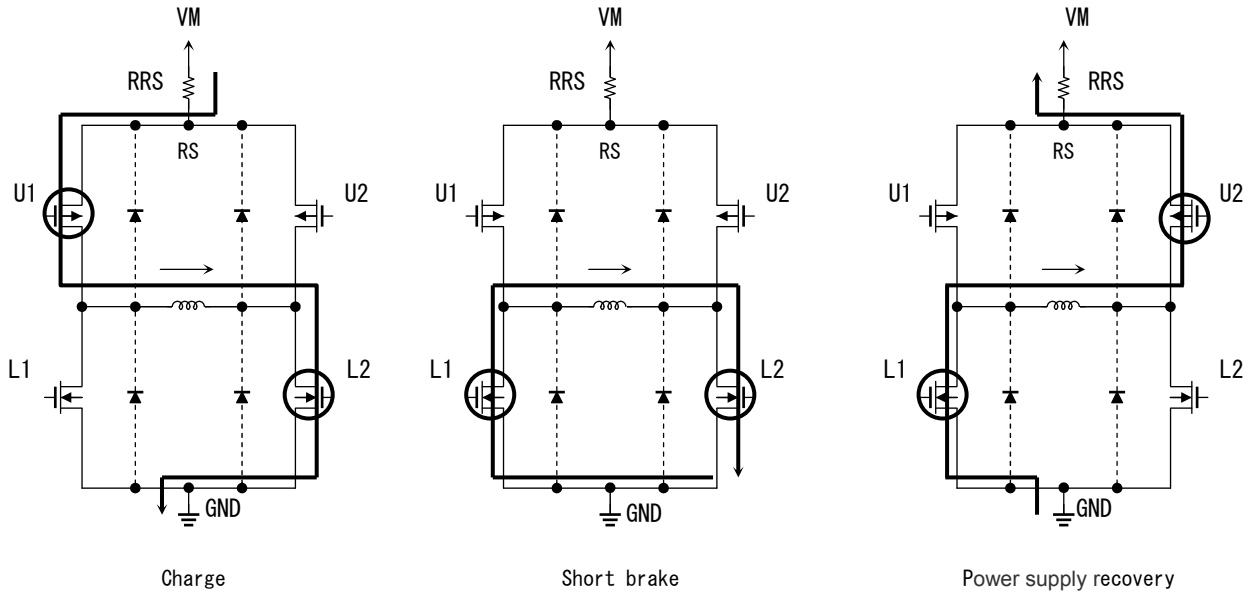


Note: About Mixed Decay Timing

Mixed Decay Timing (MDT) is a unique value of the TB62216FTG (fchop × 37.5%), but when the motor output current reaches NF (Itrip) threshold after MDT, the rest of fchop (*) becomes fast decay mode.

Timing charts may be simplified for explanatory purposes.

Output Transistor Operation Mode



Some of the functional blocks, circuits, or constants omitted or simplified for explanatory purpose.

Output Transistor Operational Function

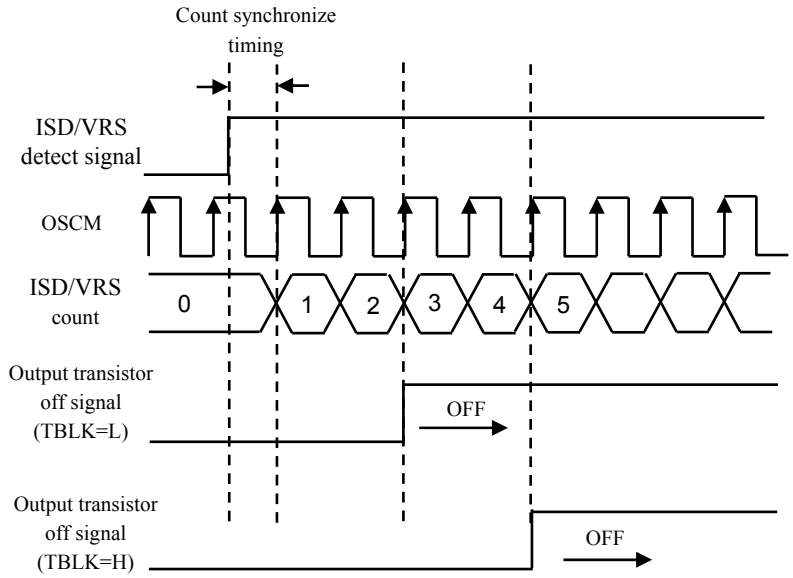
Mode	U1	L1	U2	L2
Charge	ON	OFF	OFF	ON
Slow/Short brake	OFF	ON	OFF	ON
Power supply recovery	OFF	ON	ON	OFF

Note: The parameters shown in the table above are examples when the current flows in the directions shown in the figures above. For the current flowing in the reverse direction, the parameters change as shown in the table below.

Mode	U1	L1	U2	L2
Charge	OFF	ON	ON	OFF
Slow/Short brake	OFF	ON	OFF	ON
Power supply recovery	ON	OFF	OFF	ON

Over Current Detection (ISD) and Over Voltage of RS detection of (VRS) features

・Detect timing



Timing charts may be simplified for explanatory purpose.

Over Current Eetection (ISD) and Over Voltage of RS detection (VRS) have blanking time to reject irr, switching noise and inrush current. This blanking time is based on the internal OSC (OSCM) frequency.

ISD, VRS blanking time = OSCM × 3CLK

After detecting ISD / VRS, the detect signal and the internal OSC (OSCM) synchronizes for count up; therefore, the output transistor is turned off after additional 1 CLK (max).

ISD, VRS detection time = OSCM × 4CLK

ISD and VRS do not necessarily guarantee complete IC safety. If the device is used beyond the specified operating ranges, these circuits may not operate properly; then the device may be owing to an output short circuit.
To avoid secondary trouble, please insert fuse to VM line for fail-safe.

●tBLK (blanking time for noise cancellation) features

Two types of dead time (blanking time) are incorporated according to the motor driver structures mainly to prevent error operation due to noise caused by switching.

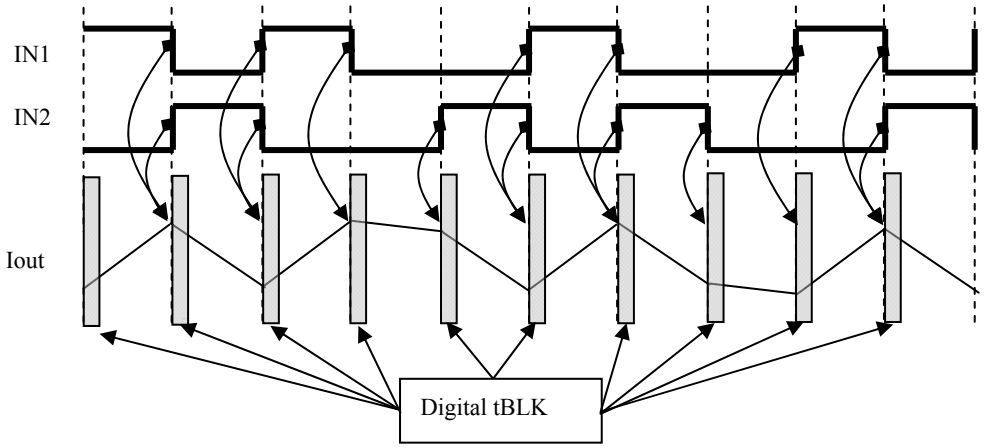
<Digital tBLK>
The digital tBLK is used to avoid error judgment of varistor recovery current that occurs in charge drive mode when H-bridges are used with DC motors. The digital tBLK time can be controlled through TBLK_A and TBLK_B pins.

- TBLK_A/B=Low level: OSCM×4clk
- TBLK_A/B=High level: OSCM×6clk

The digital tBLK is based on the internal oscillator (OSCM) frequency; therefore if the OSCM is changed by the constant(s), the digital tBLK time will also change.

<Analog tBLK>
"The dead time for noise cancellation (analog tBLK)" specified according to the motor block AC characteristics is a fixed time incorporated in the TB62216FTG. This is mainly used for avoiding error judgment of irr (diode recovery current). The analog tBLK time is a unique value of the TB62216FTG (internal timer of the TB62216FTG) controlled by an inserted low-pass filter with a fixed time of 400 ns (typ.).

● Digital tBLK timing for DC motor

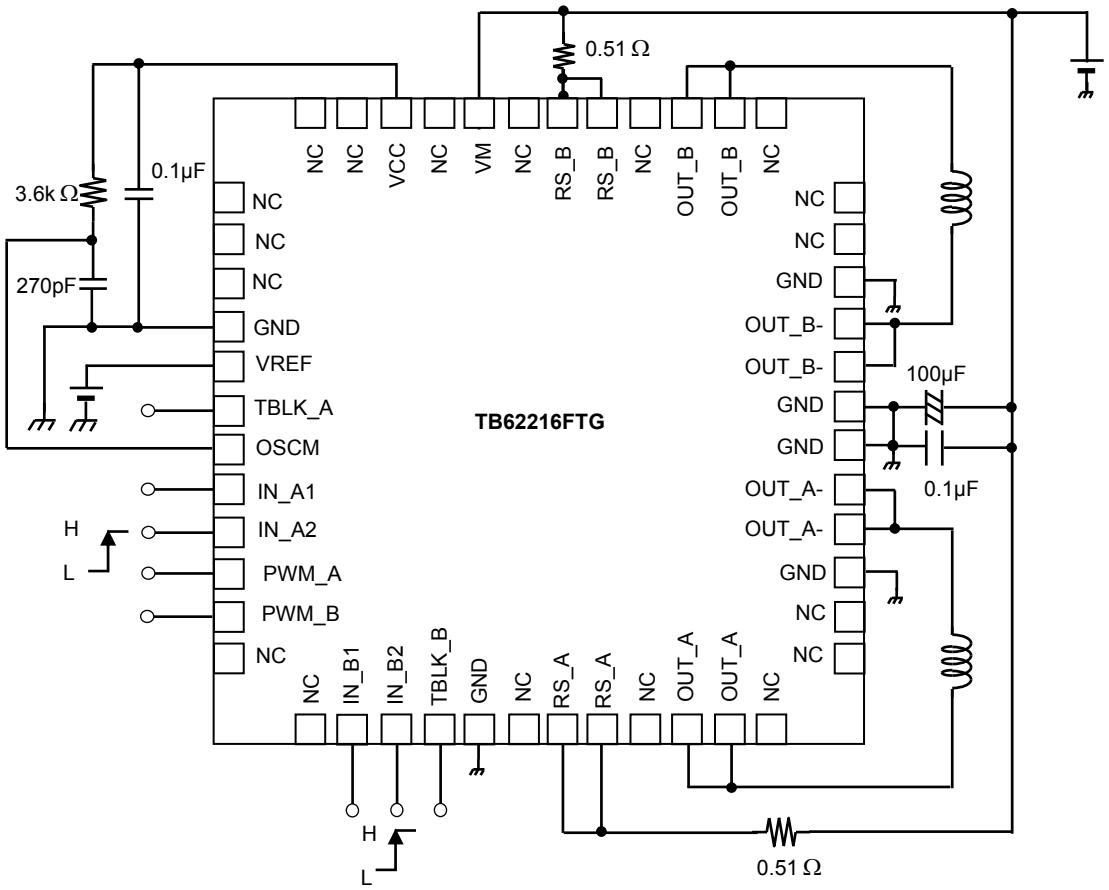


The digital tBLANK is inserted at the beginning of each charge period of the constant current chopping, and also when the IN_1 or IN_2 is switched.

Timing charts may be simplified for explanatory purpose.

Application Circuit Example

TB62216FTG (QFN48)

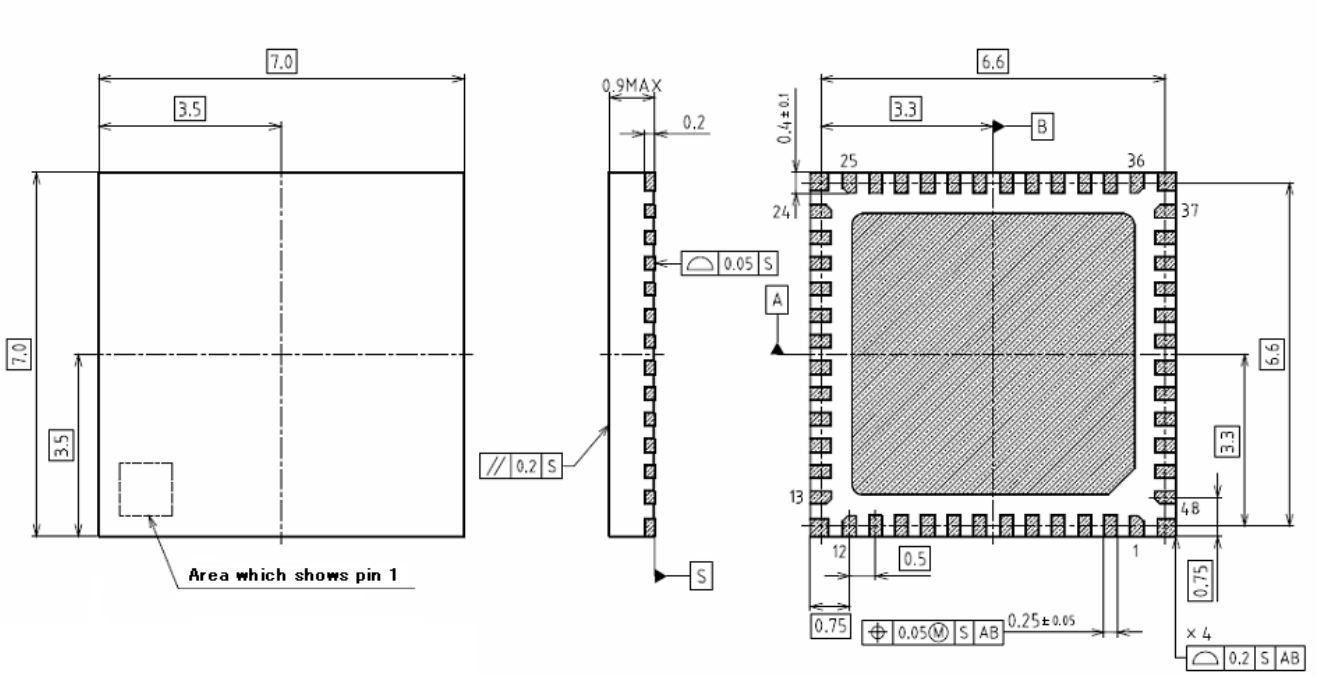


The application circuit above is an example; therefore, mass-production design is not guaranteed.

Package Dimensions

QFN48-P-0707-0.50

Unit :mm



Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.

Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occurs from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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