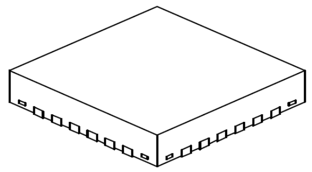
TOSHIBA BiCD Process Integrated Circuit Silicon Monolithic

TB62D786FTG

9-channel constant current LED driver with single wire

The TB62D786FTG is a constant current driver designed for LED illumination. This product incorporates 7-bit PWM dimming controllers and 9-channel constant current drivers. 9-channel constant current drivers are divided into three blocks corresponding to LED luminescence colors, and each output current can be adjusted by external resistors.
This product is controlled using the only DATA-IN input signal. It can be configured up to 64 recognition addresses with the ID setting pin.
This product includes a linear regulator (7.0 to 28 V) function, which shares with the power supply of LEDs.
Additionally, data can be transferred at high speed with BiCD process.

TB62D786FTG



P-VQFN24-0404-0.50-001
Weight: 0.037g (typ.)

Feature

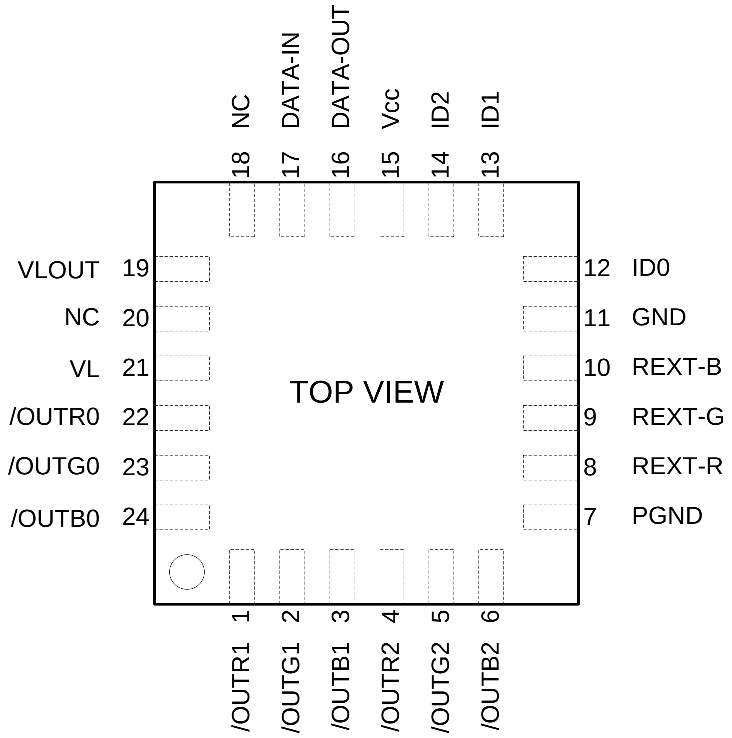
- Power supply voltage : VL = 7.0 to 28 V (The case used by sharing with a power supply of LED)
  Vcc = 5.0 V±10% (The case that the power supply of LED and that of this IC separately.)
- Maximum output current capability:80 mA (max) × 9 channels
- Constant current output range: 5 to 40 mA
- Output voltage at constant-current drive: 0.4 V(min) @I_{OUT}=5 to 40 mA
- Designed for common-anode LEDs.
- The input interface is controlled by DATA-IN (Single wire)
- Thermal shut down (TSD) included.
- Input and output of logic circuit: 5 V CMOS Interface
- Maximum output voltage: 28 V
- PWM control circuit included: 7-bit PWM
- Driver recognition: Up to 64 driver ICs can be controlled individually
- Operating temperature range: T_{opr} = -40 to 85°C
- Package: P-VQFN24-0404-0.50-001

- Constant current accuracy

Condition	Constant-current accuracy between channels	Constant-current accuracy between ICs
Output voltage: 0.5 V Output current: 15 mA	±3.0%	±6.0%

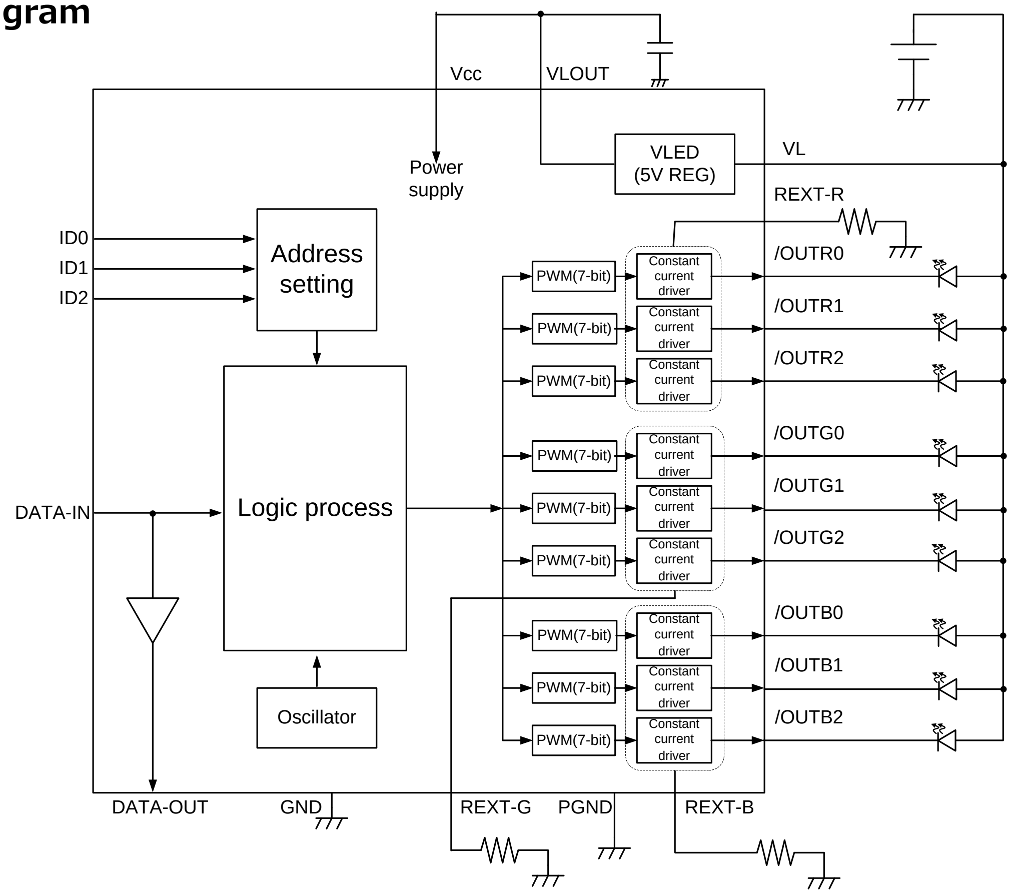
This product is very delicate because of elements of MOS structure. In handling, please take care of measures of static electricity, such as use of a ground band or an electric conduction mat, removal of static electricity by an ionizer, and management of temperature and humidity.

Pin Assignment (top view)



Please be sure to connect the back radiation PAD of a QFN package to GND of a substrate.

Block diagram



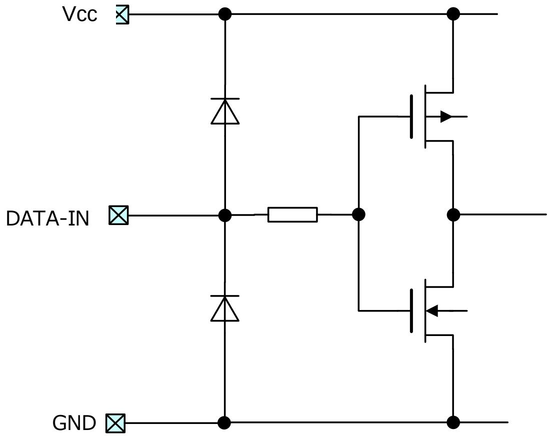
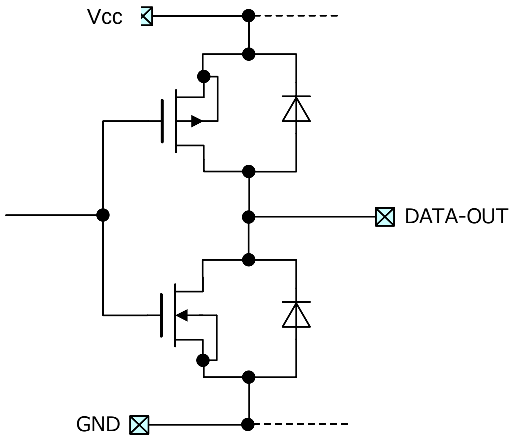
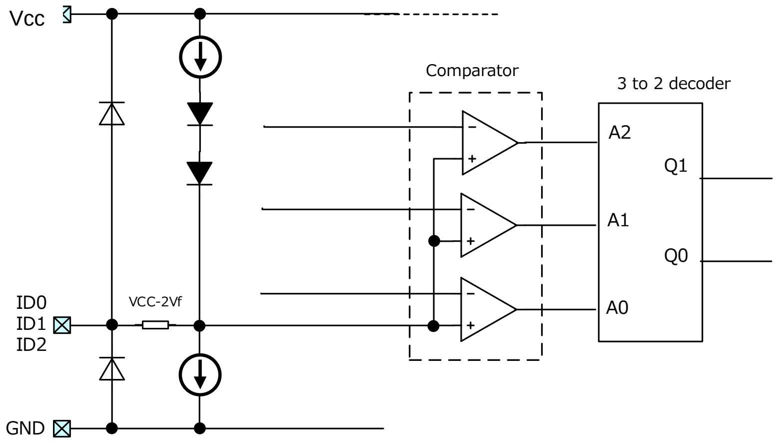
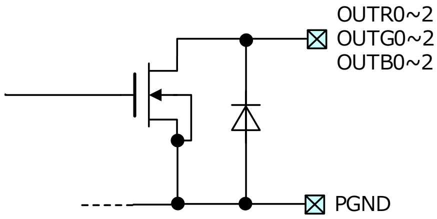
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Pin Description

Pin No.	Symbol	Function description
1	/OUTR1	Constant current output pin. (Open-drain type)
2	/OUTG1	Constant current output pin. (Open-drain type)
3	/OUTB1	Constant current output pin. (Open-drain type)
4	/OUTR2	Constant current output pin. (Open-drain type)
5	/OUTG2	Constant current output pin. (Open-drain type)
6	/OUTB2	Constant current output pin. (Open-drain type)
7	PGND	Power ground pin
8	REXT-R	External resistor pin for output current configuration (/OUTR0, /OUTR1, /OUTR2)
9	REXT-G	External resistor pin for output current configuration (/OUTG0, /OUTG1, /OUTG2)
10	REXT-B	External resistor pin for output current configuration (/OUTB0, /OUTB1, /OUTB2)
11	GND	Ground pin
12	ID0	ID configuration pin
13	ID1	ID configuration pin
14	ID2	ID configuration pin
15	Vcc	5V of supply voltage input pin
16	DATA-OUT	Serial data output pin (DATA-in input signal is output to the buffer.)
17	DATA-IN	Serial data input pin
18	NC	Non-connection pin. Please connect to GND or Vcc.
19	VLOUT	5V Regulator output pin. Please connect VLOUT and Vcc when it use included regulator. In case it inputs 5V direct to Vcc pin please VLOUT connect to GND pin.
20	NC	Non-connection pin. Please connect to GND or open. (Note 1)
21	VL	Power supply input pin in the case of sharing a power supply of LED and the power supply of this product.
22	/OUTR0	Constant current output pin. (Open-drain type)
23	/OUTG0	Constant current output pin. (Open-drain type)
24	/OUTB0	Constant current output pin. (Open-drain type)

Note 1: Please pay attention to short circuiting between adjacent pins when pin 20 is connected to GND.

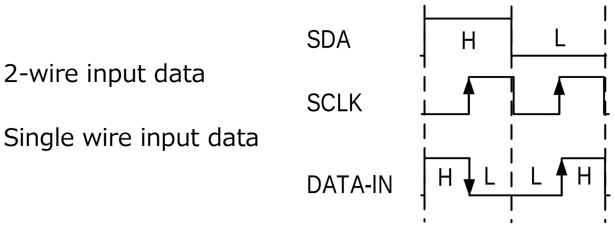
Equivalent circuit for inputs and outputs

Pin No.	Equivalent circuit
DATA-IN	
DATA-OUT	
ID0 to 2	
/OUTR0 to 2 /OUTG0 to 2 /OUTB0 to 2	

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Programming the TB62D786FTG

This product is controlled with single wire data signal shown in the following. As compared with 2-wire data signal synchronous with the clock signal in conventional products, this product assigns each data to the transition of potential (H to L or L to H).



(1) Data setting format

Each command setting input to DATA-IN is set with the following format.

This product recognizes the communication frequency (rising interval of input data) by taking in the start command (the start condition of data input).

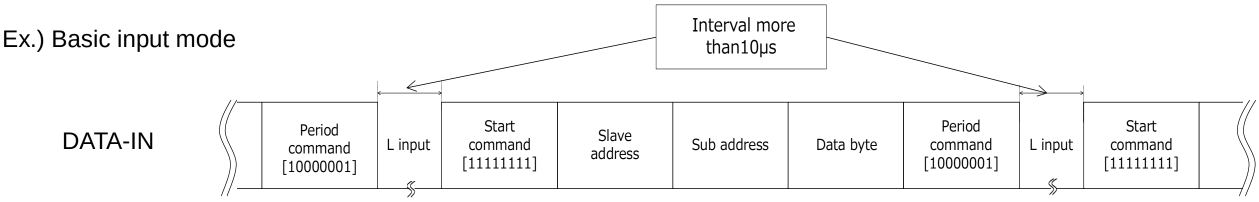
Start command : 1010101010101010=0xAA, 0xAA (original binary: 11111111)

Since this product continues to recognize the signal interval which recognizes at the start command until the period command, input the pulse width so that the period is not collapsed until completion of the period command.

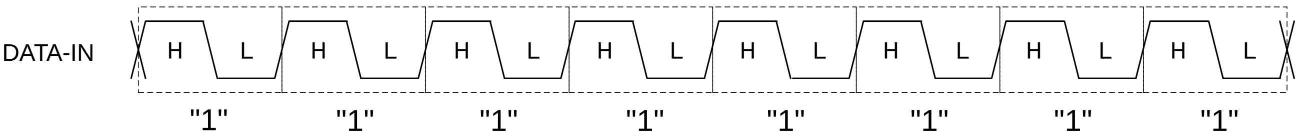
Period command : 1001010101010110=0x95,0x56 (original binary: 10000001)

After the completion of the period command input, make sure to set the interval ("L") more than 10 μs just before next start command input.

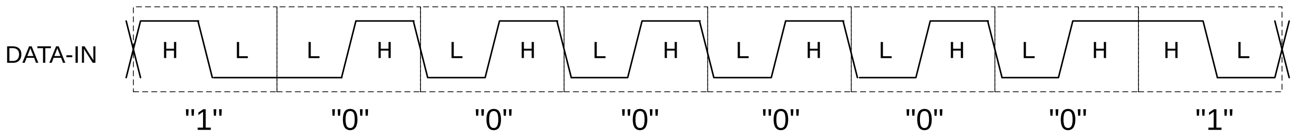
<Input format>



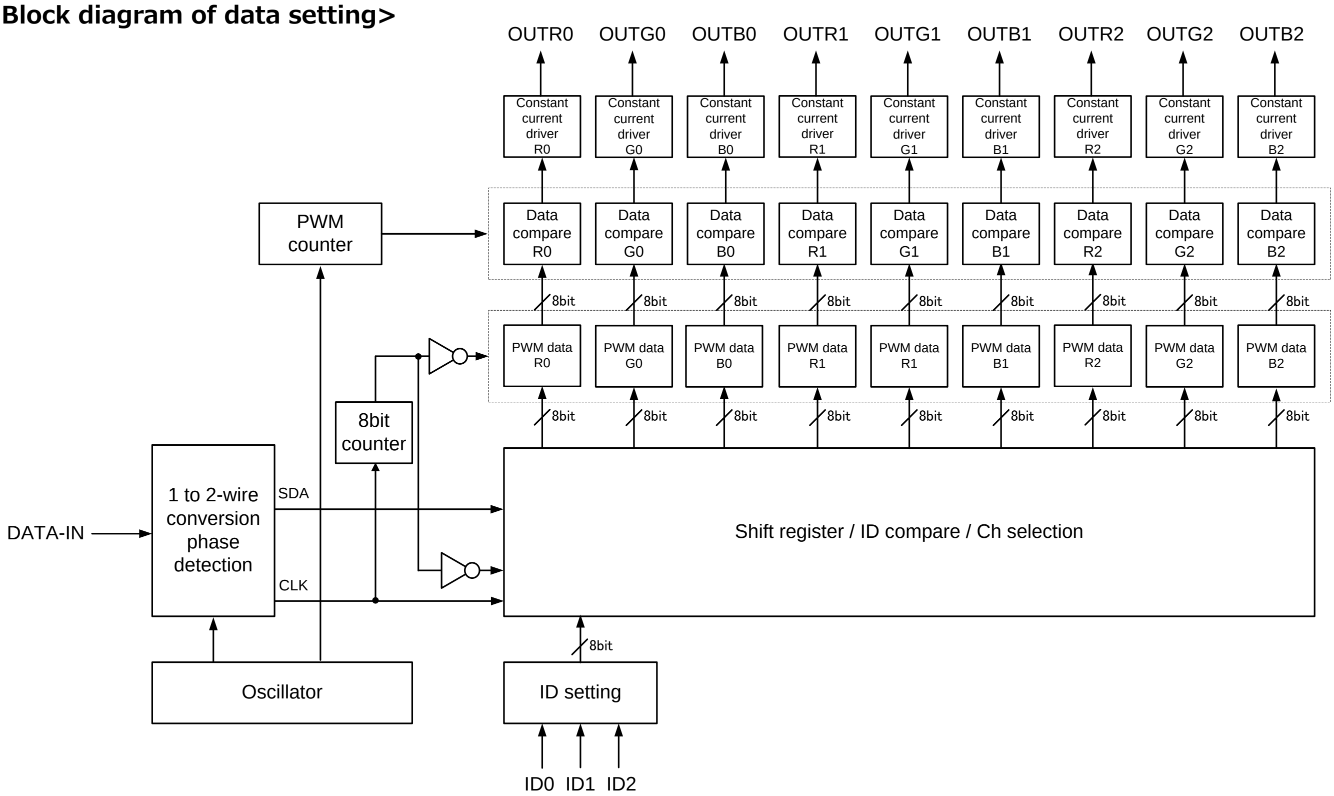
Example 1) Start command setting 0xAA, 0xAA (original binary 11111111)



Example 2) Period command setting [original binary 10000001]



<Block diagram of data setting>



(2) Normal programming mode

Normal input mode should be set as the following flow.

Start command -> Slave address -> Sub-address -> Data byte -> Period Command

Slave address: ID of IC, Sub-address: set to Output channel, Data byte: setting PWM

Interval (“L” more than 10μs)	Start Command	Slave Address	Sub-address (channel select)	Data byte (PWM configuration)	Period Command	Interval (“L” more than 10μs)

(3) Special programming mode

This is how to set when all channels are set individually.

-Special mode setting (In the case that all channels are set individually)

If the Special mode is set to sub-address, the illuminating data of all channels can be set.

Special mode: 0110100101010101=0x69, 0x55 (original binary: 01100000)

Interval (“L” more than 10μs)	Start Command	Slave Address	Sub-address (Special mode)	Data OUTR0	Data OUTG0	Data OUTB0

Data OUTR1	Data OUTG1	Data OUTB1	Data OUTR2	Data OUTG2	Data OUTB2	Period Command

Please set 9 channels of data surely. (When the data more than 9 channels are input, the 10th and subsequent data are invalid.).

-Channel setting to be output

Start Command	Slave Address	Sub-address (channel setting)	Data setting (Output which is set at sub-address)	Period Command

(4)Data settings

a) Slave address

Input voltages and logic states of the ID0, ID1, ID2 pins are determined as follows.
(MSB=”0”, LSB =0 (Except of all selections))
Vcc=”1010”=0xA, open="1001”=0x9, REXT-R/B/G(*)=”0110”=0x6, GND=”0101”=0x5

Slave setting

Slave address		Original binary	ID2	ID1	ID0
Input with one wire	Hexadecimal				
0101010101010101	0x5555	00000000	GND	GND	GND
0101010101011001	0x5559	00000010	GND	GND	REXT-R/G/B*
0101010101100101	0x5565	00000100	GND	GND	Open
0101010101101001	0x5569	00000110	GND	GND	Vcc
0101010110010101	0x5595	00001000	GND	REXT-R/G/B*	GND
0101010110011001	0x5599	00001010	GND	REXT-R/G/B*	REXT-R,G,B*
0101010110100101	0x55A5	00001100	GND	REXT-R/G/B*	Open
0101010110101001	0x55A9	00001110	GND	REXT-R/G/B*	Vcc
0101011001010101	0x5655	00010000	GND	Open	GND
0101011001011001	0x5659	00010010	GND	Open	REXT-R/G/B*
0101011001100101	0x5665	00010100	GND	Open	Open
0101011001101001	0x5669	00010110	GND	Open	Vcc
0101011010010101	0x5695	00011000	GND	Vcc	GND
0101011010011001	0x5699	00011010	GND	Vcc	REXT-R/G/B*
0101011010100101	0x56A5	00011100	GND	Vcc	Open
0101011010101001	0x56A9	00011110	GND	Vcc	Vcc
0101100101010101	0x5955	00100000	REXT-R/G/B*	GND	GND
0101100101011001	0x5959	00100010	REXT-R/G/B*	GND	REXT-R/G/B*
0101100101100101	0x5965	00100100	REXT-R/G/B*	GND	Open
0101100101101001	0x5969	00100110	REXT-R/G/B*	GND	Vcc
0101100110010101	0x5995	00101000	REXT-R/G/B*	REXT-R/G/B*	GND
0101100110011001	0x5999	00101010	REXT-R/G/B*	REXT-R/G/B*	REXT-R/G/B*
0101100110100101	0x59A5	00101100	REXT-R/G/B*	REXT-R/G/B*	Open
0101100110101001	0x59A9	00101110	REXT-R/G/B*	REXT-R/G/B*	Vcc
0101101001010101	0x5A55	00110000	REXT-R/G/B*	Open	GND
0101101001011001	0x5A59	00110010	REXT-R/G/B*	Open	REXT-R/G/B*
0101101001100101	0x5A65	00110100	REXT-R/G/B*	Open	Open
0101101001101001	0x5A69	00110110	REXT-R/G/B*	Open	Vcc
0101101010010101	0x5A95	00111000	REXT-R/G/B*	Vcc	GND
0101101010011001	0x5A99	00111010	REXT-R/G/B*	Vcc	REXT-R/G/B*
0101101010100101	0x5AA5	00111100	REXT-R/G/B*	Vcc	Open
0101101010101001	0x5AA9	00111110	REXT-R/G/B*	Vcc	Vcc
0110010101010101	0x6555	01000000	Open	GND	GND
0110010101011001	0x6559	01000010	Open	GND	REXT-R/G/B*
0110010101100101	0x6565	01000100	Open	GND	Open
0110010101101001	0x6569	01000110	Open	GND	Vcc
0110010110010101	0x6595	01001000	Open	REXT-R/G/B*	GND
0110010110011001	0x6599	01001010	Open	REXT-R/G/B*	REXT-R/G/B*
0110010110100101	0x65A5	01001100	Open	REXT-R/G/B*	Open
0110010110101001	0x65A9	01001110	Open	REXT-R/G/B*	Vcc
0110011001010101	0x6655	01010000	Open	Open	GND
0110011001011001	0x6659	01010010	Open	Open	REXT-R/G/B*
0110011001100101	0x6665	01010100	Open	Open	Open
0110011001101001	0x6669	01010110	Open	Open	Vcc
0110011010010101	0x6695	01011000	Open	Vcc	GND
0110011010011001	0x6699	01011010	Open	Vcc	REXT-R/G/B*
0110011010100101	0x66A5	01011100	Open	Vcc	Open
0110011010101001	0x66A9	01011110	Open	Vcc	Vcc

0110100101010101	0x6955	01100000	Vcc	GND	GND
0110100101011001	0x6959	01100010	Vcc	GND	REXT-R/G/B*
0110100101100101	0x6965	01100100	Vcc	GND	Open
0110100101101001	0x6969	01100110	Vcc	GND	Vcc
0110100110010101	0x6995	01101000	Vcc	REXT-R/G/B*	GND
0110100110011001	0x6999	01101010	Vcc	REXT-R/G/B*	REXT-R/G/B*
0110100110100101	0x69A5	01101100	Vcc	REXT-R/G/B*	Open
0110100110101001	0x69A9	01101110	Vcc	REXT-R/G/B*	Vcc
0110101001010101	0x6A55	01110000	Vcc	Open	GND
0110101001011001	0x6A59	01110010	Vcc	Open	REXT-R/G/B*
0110101001100101	0x6A65	01110100	Vcc	Open	Open
0110101001101001	0x6A69	01110110	Vcc	Open	Vcc
0110101010010101	0x6A95	01111000	Vcc	Vcc	GND
0110101010011001	0x6A99	01111010	Vcc	Vcc	REXT-R/G/B*
0110101010100101	0x6AA5	01111100	Vcc	Vcc	Open
0110101010101001	0x6AA9	01111110	Vcc	Vcc	Vcc
01XXXXXXXXXXXX10	0x4002**	0XXXXXX1	All selections		

* Please set it as a pin for one of REXT-R,G,B.

** The hexadecimal number display of all selections is a case which is defined as x=0.

b) Sub-address

Output channel setting/ All channels setting/ Special mode setting

In output channel setting, a channel which defines PWM configuration is selected. In all channels setting, PWM is configured for all channels. The special mode is the mode which sets all channels individually.

Channel setting command		Original binary	Channel setting
Input with one wire	Hexadecimal		
0101010101011001	0x5559	00000010	/OUTR0
0101010101100101	0x5565	00000100	/OUTG0
0101010101101001	0x5569	00000110	/OUTB0
0101010110010101	0x5595	00001000	/OUTR1
0101010110011001	0x5599	00001010	/OUTG1
0101010110100101	0x55A5	00001100	/OUTB1
0101010110101001	0x55A9	00001110	/OUTR2
0101011001010101	0x5655	00010000	/OUTG2
0101011001011001	0x5659	00010010	/OUTB2
0101100101010101	0x5955	00100000	All channels setting
0110100101010101	0x6955	01100000	Special mode setting

c) Data byte (PWM setting)

Data bytes set PWM dimming.

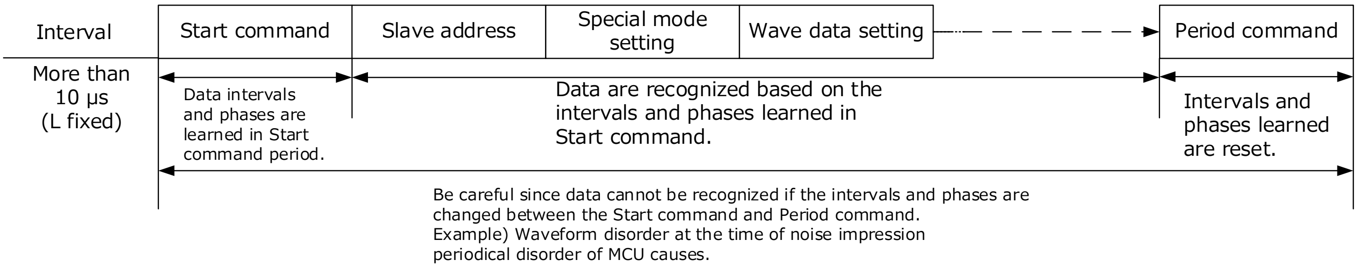
PWM setting command		Original binary	PWM dimming
Input with one wire	Hexadecimal		
0101010101010101	0x5555	00000000	0/127
0101010101011001	0x5559	00000010	1/127
0101010101100101	0x5565	00000100	2/127
…		…	…
1010101010100101	0xAAA5	11111100	126/127
1010101010101001	0xAAA9	11111110	127/127

Note: Any data other than those specified above must not be programed.
Default setting is 0/127.

(5) Notes of data setting

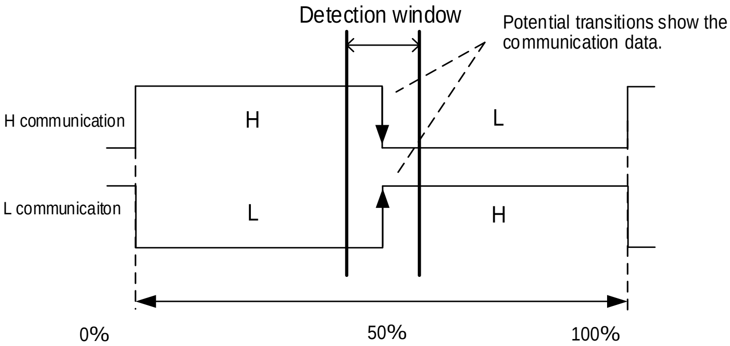
This product has the specification of data recognition or processing with only a data signal (asynchronous input signal). The data period (communication speed) is read (learned) with the start command (data input start condition). Data are recognized according to this learning period, and reset the learning period with the period command (data input completion condition). Therefore, if the data period from the start command to the period command is collapsed, data are not recognized (see the following (a)). Then the period learned during an interval period is reset and it waits for next communication.

(a) Learning data period



(b) Data recognition

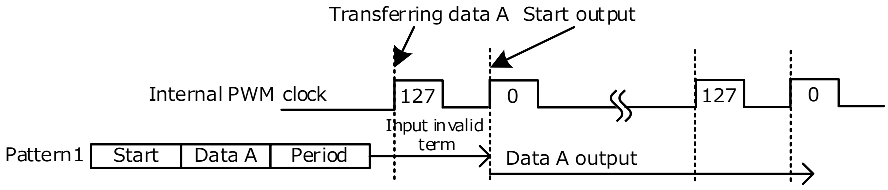
The data input of this product makes data 2 bits (H, and L, or L and H) on the basis of a Manchester code, and transitions of the potential in a detection window show logic. Including jitter, communication delay and others, data are received by potential transitions in the detection window.



Reference: Example of control data input

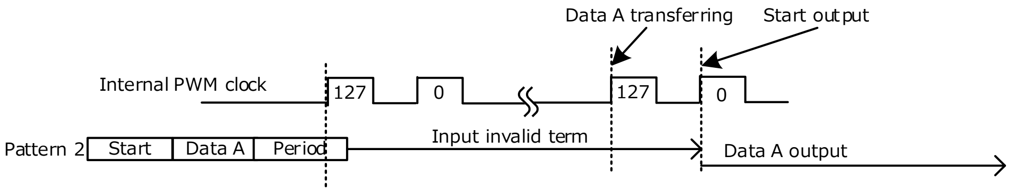
(6) Example of data input to the same ID

a) In case data A is input up to the rising edge of 127 internal PWM clocks.



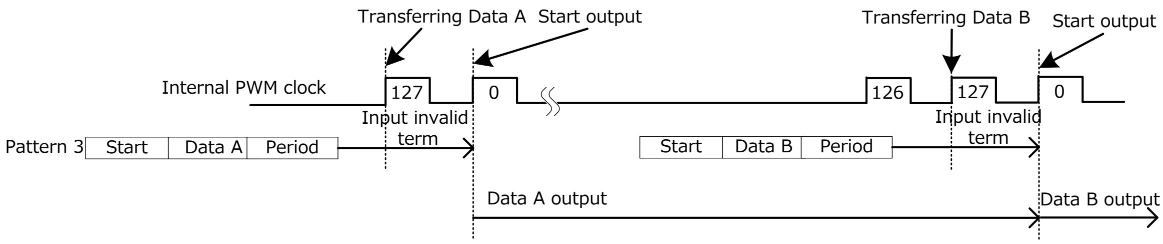
Output data A starts at the rising edge of zero internal PWM clock.
Inputting is invalid from the rising edge of 127 internal PWM clocks to the rising edge of zero internal PWM clock which is just after these 127 PWM clocks.

b) In case data A is input after the rising edge of 127 internal PWM clocks.



Outputting data A does not start at the rising edge of zero internal PWM clock just after the data A is input. It starts at the next rising edge of zero internal PWM clock.
Inputting is invalid from the data A (period) input to the rising edge of after the next zero internal PWM clock.

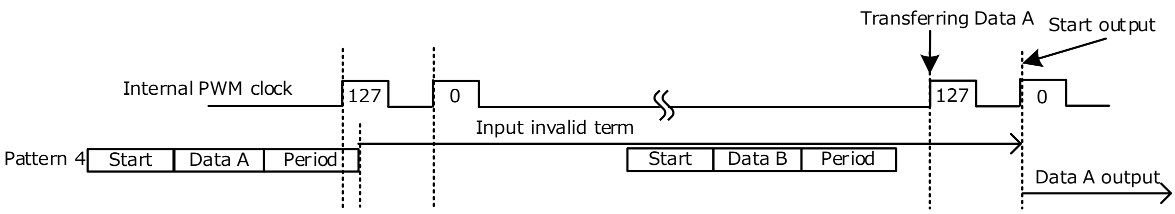
c) In case data B is input after data of pattern 1 starts outputting.



Outputting data A starts at the rising edge of zero internal PWM clock just after the data A is input. Outputting data B starts at the rising edge of zero internal PWM clock which is just after the data B input.
Inputting is invalid in the following term.
From the rising edge of 127 internal PWM clocks which are just after the data A is input to the rising edge of zero internal PWM clock which is just after these 127 clocks.
From the rising edge of 127 internal PWM clocks which is just after the data B input to the rising edge of zero internal PWM clock which is just after these 127 clocks.

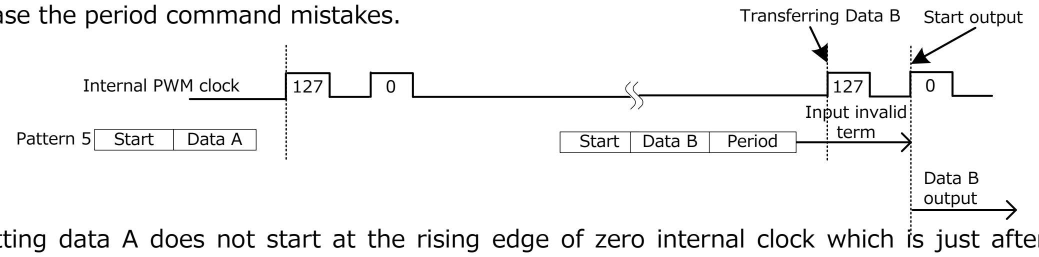
Pay attention that the IC does not operate according to the configuration while the following patterns (patterns 4 and 5) are input.

d) In case data B is input before starting the output of pattern 2.



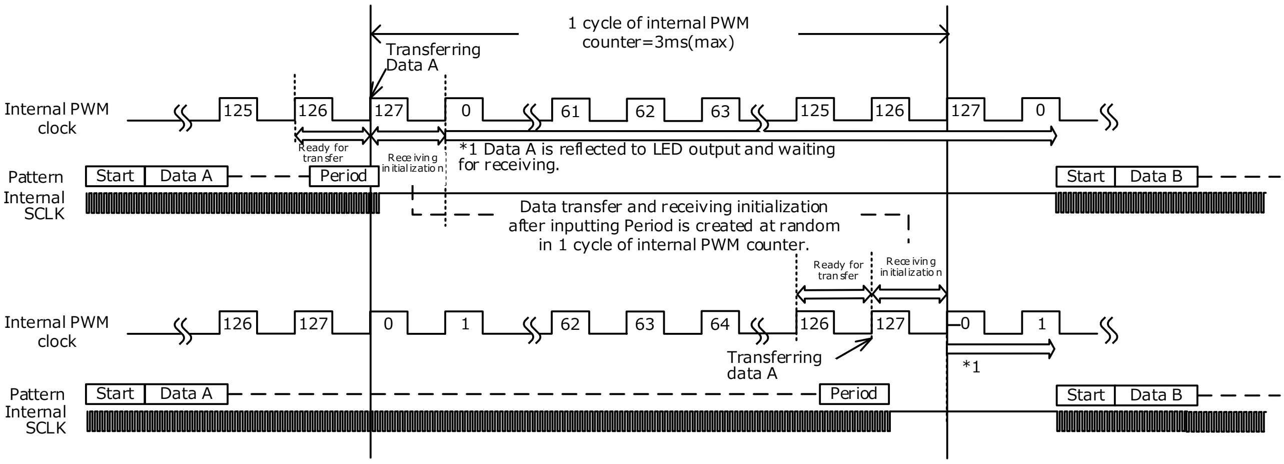
Inputting is invalid from the data A (period) input to the rising edge of the second internal clock. So, data B is invalid and data A is output.

e) In case the period command mistakes.



Outputting data A does not start at the rising edge of zero internal clock which is just after the data A input. Outputting data B starts at the rising edge of zero internal PWM clock which is just after the data B input.

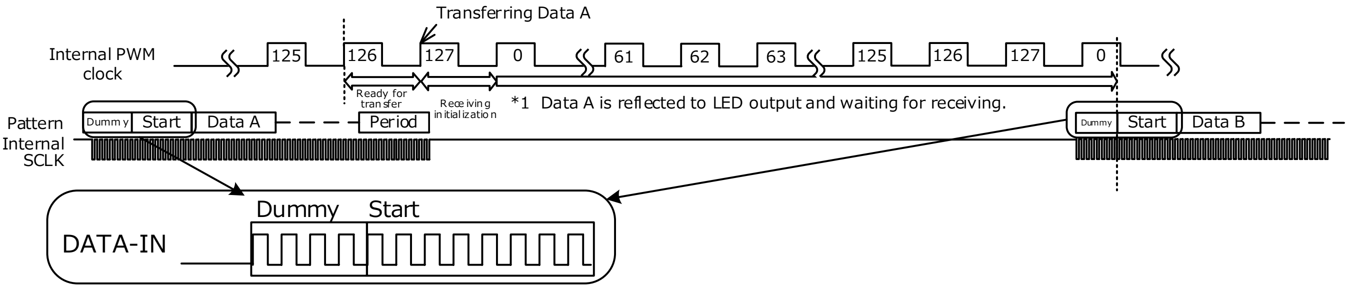
f) In case of matching asynchronously the timing between pattern end and internal data update



In case of matching asynchronously the timing between SCLK end and internal data update, the start command at the beginning of next pattern may not be received. That may occur in the pattern of first IC if there are patterns for two or more ICs. That does not occur if the pattern length is as follows.

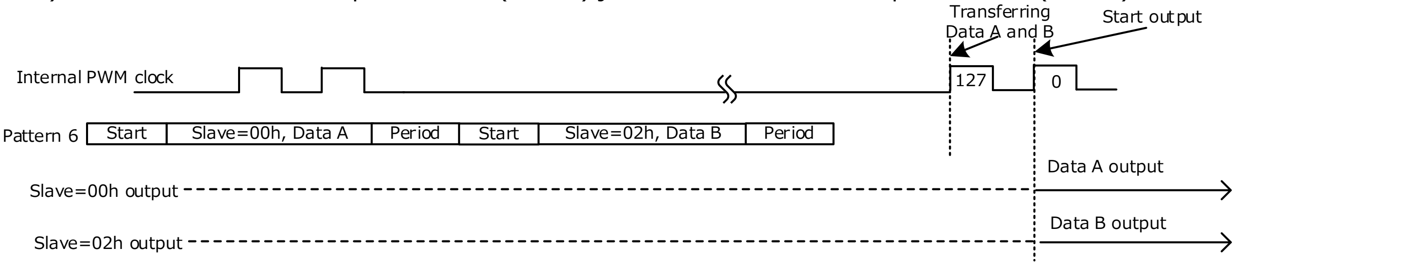
1. Less than minimum 10.6 μs after inputting period command
2. Exceeding maximum 3 ms from point of 1.

This time management is difficult. We recommend that the following measures are applied from initial state to avoid the occurrence of the event.
Dummy data are added to the beginning of the pattern, and 1 time or more SCLKs should be added.
The following figure shows the dummy data = L. However, the dummy data =H is also possible.



(7) Example of data input to the different ID.

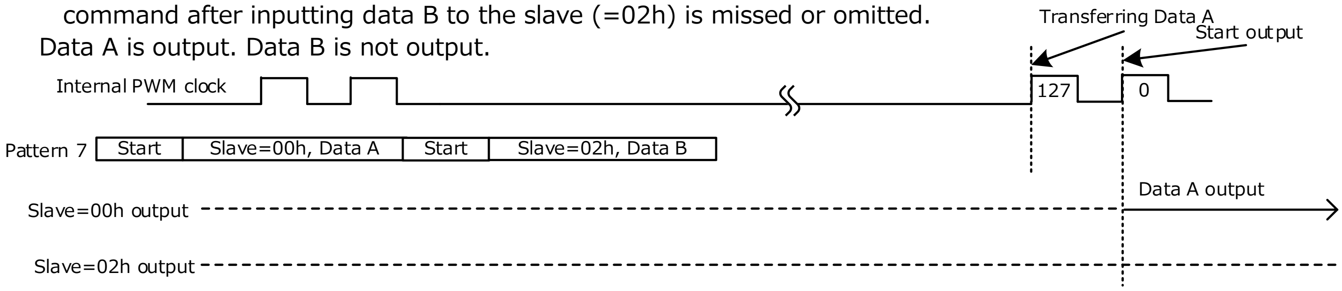
a) In case the data B is input to slave (= 02h) just after the data A is input to slave (= 00h).



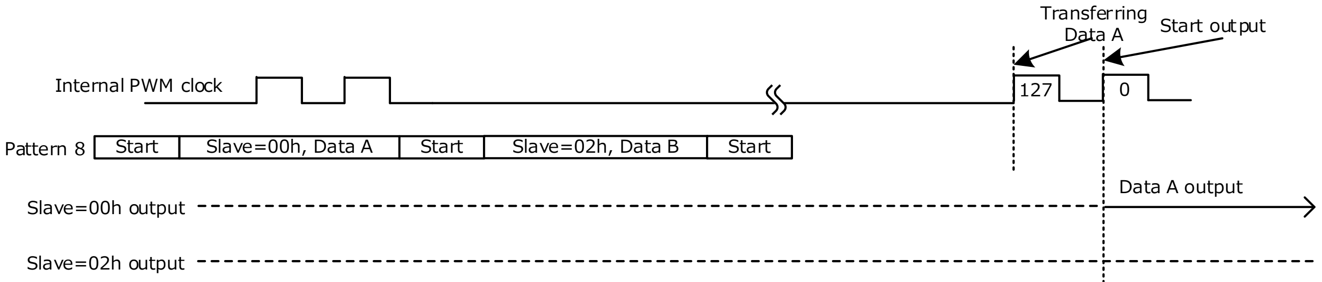
Both data A and data B are output at the rising edge of zero internal PWM clock which is just after the data A and the data B inputs.

(Reference)
Pay attention that the IC does not operate according to the configuration while following patterns (patterns 7 and 8) are input.

b) In case period command after inputting data A to the slave (=00h) is missed or omitted, or in case period command after inputting data B to the slave (=02h) is missed or omitted.
Data A is output. Data B is not output.



c) In case start command is input after data B of pattern 7 is input.



Data A is output. Data B is not output.

Power Supply Block

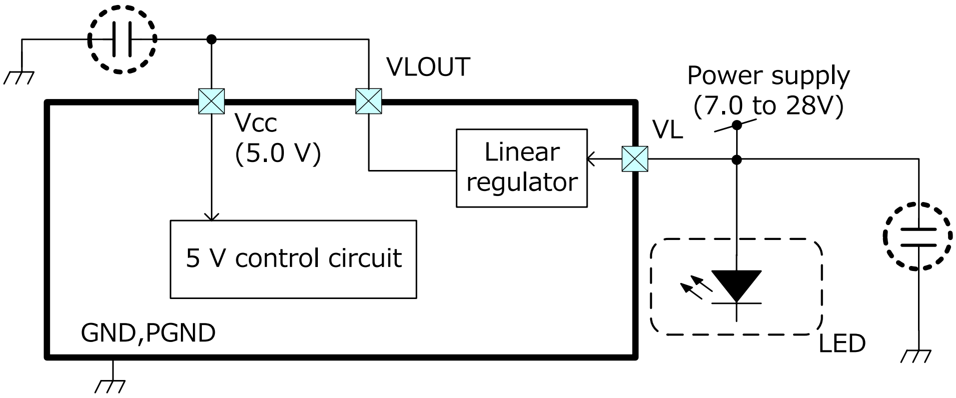
The power supply of this product can be set with the following 2 ways shown in (1) and (2).

(1) When the power supply of LEDs and those of this product are shared (The power supply function of this product is used.)

(2) When this product is operated with 5V power supply input, not sharing the power supply of LEDs (The power supply function of this product is not used.)

Each setting is shown below.

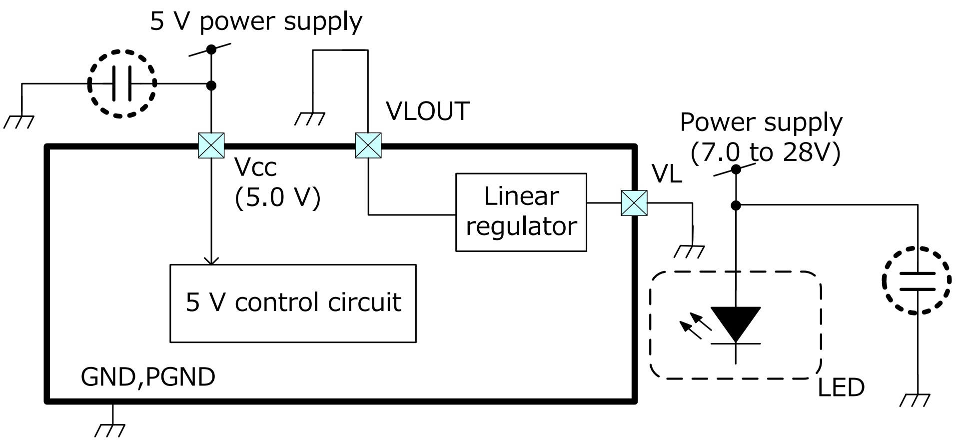
(1) When the power supply of LEDs and those of this product are shared



As shown in the above, the power supply (7.0 to 28V) is applied to the VL pin, and VLOUT and Vcc pins are connected directly.

Connect VLOUT pin output (5V) to Vcc of this product, and also connect at within 15 mA.

(2) When 5V power supply is input to Vcc directly



When 5V power supply is applied to this product without using the built-in power supply, ground VL pin and VLOUT pin to GND.

Note:

Add decoupling capacitors to VL pin and Vcc pin. The recommended values are as follows.

Recommended value of decoupling capacitors between VL (LED power supply) and GND: 1 μF of electrolytic capacitor

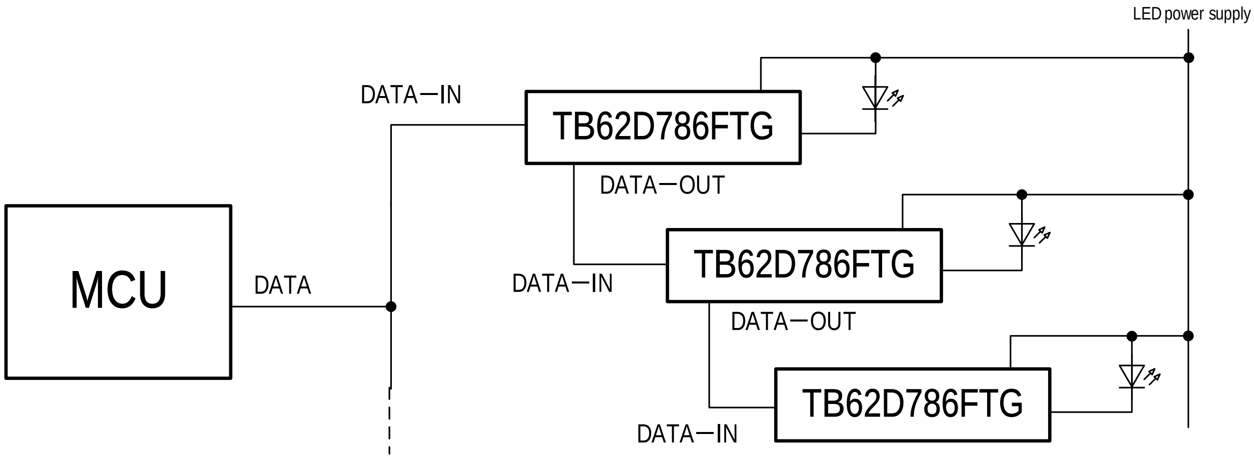
* Evaluate appropriately since it is dependent on the main power supply performance.

Recommended value of decoupling capacitors between Vcc (5V power supply) and GND: 1μF of electrolytic capacitor and 0.1μF of ceramic capacitor

* Evaluate appropriately since it is dependent on the LED current to be set and current supply amount of VLOUT.

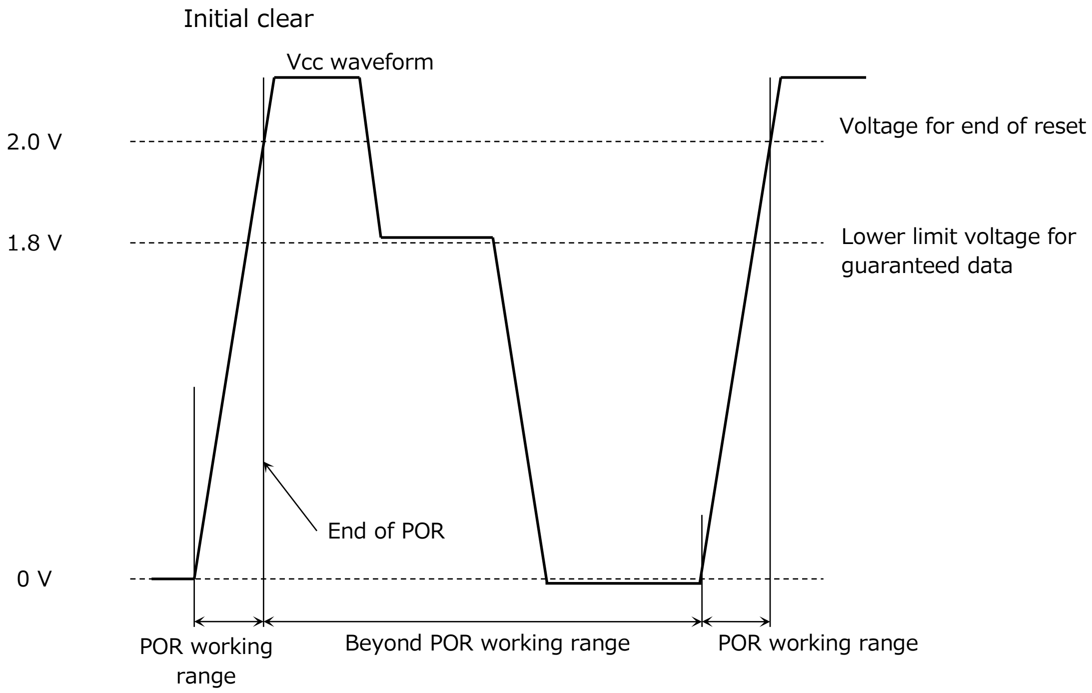
Data buffer

Data buffer is built in between DATA-IN and DATA-OUT, and it can be used for the cascade connection of two or more these products.
In the case of cascade connection with this buffer, connect up to 5 pieces (@ 2 MHz communication) on the same board.



Power on reset (POR)

It avoids the malfunction by the reset all internal data of IC and setting default in startup.
POR circuit operates only when VDD rises from 0 V. To restart POR, Vcc should be 0 V.
As for the voltage for holding internal data, it is guaranteed after Vcc reaches 4.5 V or more once.



Thermal shutdown function (TSD)

When the temperature of internal IC exceeds 150°C, all constant current outputs are turned off by this function. The constant current is output again when the temperature decreases to the rating.

TSD operation temperature 150°C to 180°C
TSD reset temperature 20°C below TSD operation temperature

* TSD function aims at detecting abnormal heating of ICs. Please avoid positively using the TSD function.

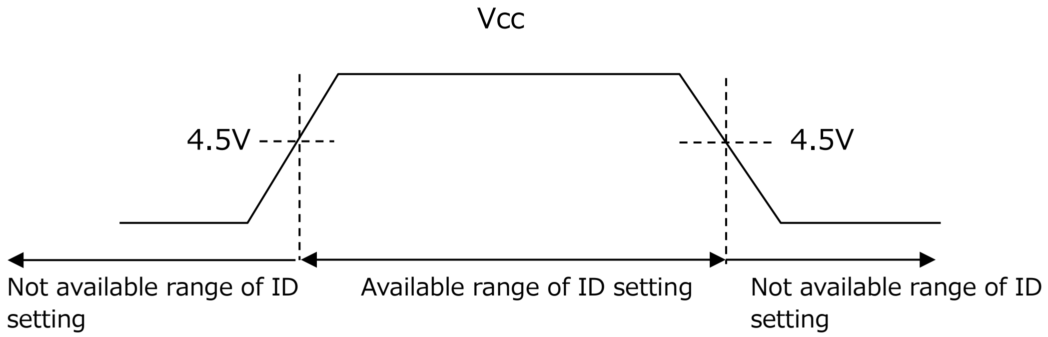
Notes of setting

1. Output load
   This product is the driver in which loads are LEDs. Do not connect loads except LEDs to the output.

2. External resistor for LED drive current setting (REXT-R, REXT-G, REXT-B)
   The external resistances to be connected to REXT-R, REXT-G, and REXTt-B pins should be connected separately. Three resistors must not be collected as one resister. If they are collected, current error is generated in each RGB.

3. Operation sequence of ID setting
   The ID setting can be available when Vcc exceeds 4.5 V after turning on.

   However, in order to prevent malfunction of the ID setting, the transitional input signals of less than 2-clock period of external input data (DATA-IN) are not received.



4. Data setting
   The gradation signals should be input data for 9 channels in the special mode certainly.
   When the data are input to over 9 channels, the data after 10th channel are invalid.
   When the data are input to less than 9 channels, the data of channels to be input are held, and the data of channels not to be input are held data before the input.
   Moreover, do not input data which are not indicated in this document.
   Confirm “Programming the TB62D786FTG” and “(5) Notes of data setting.”

5. Data setting timing
   When data are input to same slave address, next data should be input with spacing the interval 3 ms or more (128 internal PWM clocks) because data may not be received.
   When data are input to different slave address, the interval 3 ms (128 internal PWM clocks) or more is not required.

6. Decoupling capacitor
   For the stabilization of power supply system, it is recommended that decoupling capacitor between power supply and GND should place as near IC as possible. For details, refer to "power supply block."

State Transition Diagram

<With VL pin>

VLOUT pin and Vcc pin are wire-connected beforehand, and set each IC's ID (from ID0 to ID2 pin).

Turning on main power supply (VL pin)

VLOUT pin supplies IC operation voltage (4.5 V or more).

Vcc pin voltage is 4.5V or more.

ID recognition

Data should be input after Vcc voltage reaches 4.5V or more, and minimum 15ms passes.

Normal mode
The data of each output is updated for every ID set by the DATA signals, and LED illuminating is controlled.

More than TSD detecting temperature

Less than TSD detecting temperature

TSD (Thermal Shut Down) mode
All LED outputs are forced to OFF if the TSD detection temperature has reached.
The internal data are held.

<Without VL pin>

VLOUT pin and VL pin are wire-connected to GND beforehand, and set each IC's ID (from ID0 to ID2 pin).

Turning on IC power supply (Vcc pin)

Vcc pin voltage reaches 4.5V or more.

ID recognition

Data should be input after Vcc voltage reaches 4.5V or more, and minimum 15ms passes.

Normal mode
The data of each output is updated for every ID set by the DATA signals, and LED illuminating is controlled.

More than TSD detecting temperature

Less than TSD detecting temperature

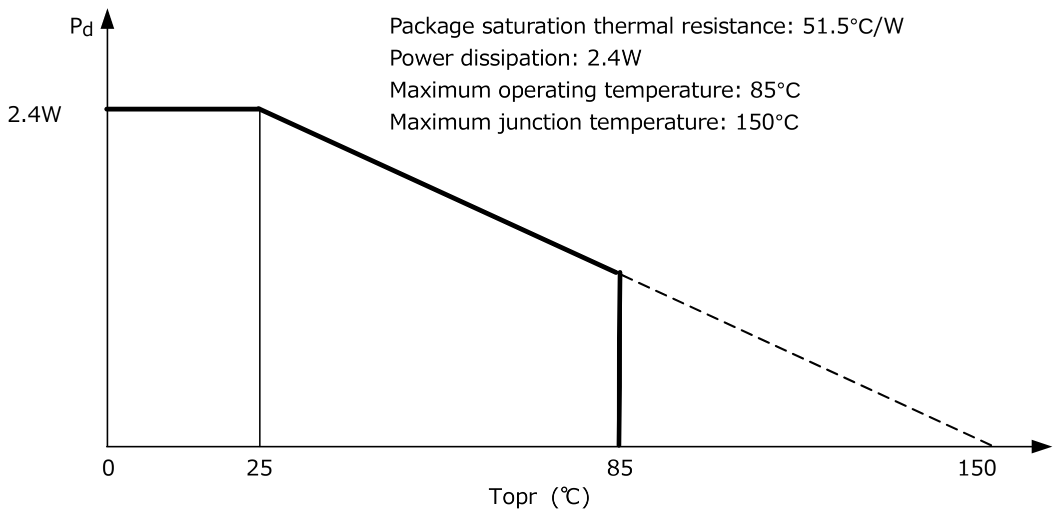
TSD (Thermal ShutDown) mode
All LED outputs are forced to OFF if the TSD detection temperature has reached.
The internal data are held.

Absolute Maximum Ratings (T_a=25°C)

Characteristics	Symbol	Rating	Unit
VL pin Supply Voltage	VL	29	V
Vcc pin Supply Voltage	Vcc	6.0	V
Input Voltage	V_{IN}	-0.3 to Vcc + 0.3 (Note 1)	V
Output Current	I_{OUT}	85 (Note 4)	mA/ch
Output Voltage	V_{OUT}	-0.3 to 29	V
Power Dissipation	P_d	2.4 (Note 2 and 3)	W
Thermal resistance	$R_{th\ (j-a)}$	51.5 (Note 2)	°C/W
Operating Temperature Rating	T_{opr}	-40 to 85	°C
Storage Temperature Rating	T_{stg}	-55 to 150	°C
Maximum junction Temperature	T_j	150	°C

Note 1: Do not exceed 6.0 V.
Note 2: When mounted on a PCB(Material: FR-4 compliant with JEDEC 4 layers board, Board size: 76.2×114.3×1.6mm)
Note 3: Power dissipation is reduced by 1/ $R_{th(j-a)}$ for each °C above 25°C ambient.
Note 4: Current may be further restricted due to ambient temperature or board condition.
T_a: Ambient temperature of ICs
T_{opr}: Ambient temperature of ICs to be operated
T_j: IC chip temperature during operating
For the design, it is recommended that the maximum of T_j is considered of the amount of use dissipation at about 120°C.

Power Dissipation

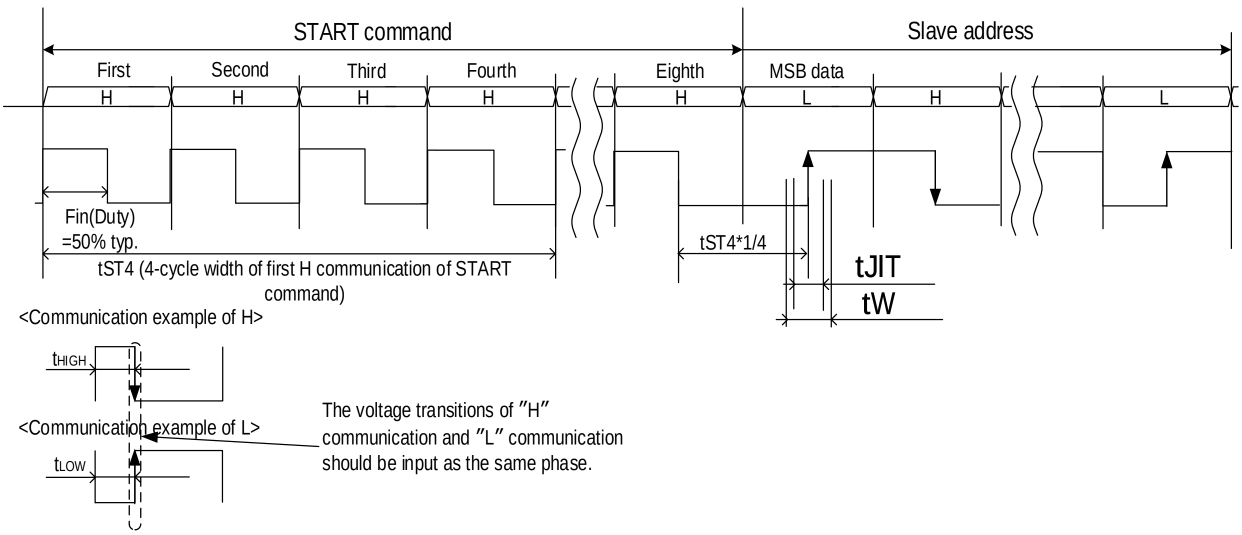


Operating Ranges (T_a=-40 to 85°C, Fin=0.5 to 2.0 MHz, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
VL pin Supply voltage	VL	—	7.0	—	28	V
Vcc pin supply voltage	Vcc	—	4.5	—	5.5	V
Output Voltage	$V_{OUT(ON)}$	All outputs	0.5	—	4	V
Output Current	I_{OUT}	All outputs	5	—	40	mA/ch
Input DATA Frequency	Fin	—	0.5	—	2.0	MHz
DATA Detection window width	tW	—	135	—	—	ns
Input DATA allowable jitter width	tJIT	The transition of input DATA potential is the center.	—	—	±54	ns
Input DATA minimum pulse width	tHIGH, tLOW	—	100	—	—	ns
Input Voltage	V_{IH}	DATA-IN	0.7 × Vcc	—	Vcc	V
	V_{IL}		GND	—	0.3 × Vcc	
	V_{ID0}	ID0, ID1, ID2 VREXT=1.128 V (typ.)	0	—	0.1	
	V_{ID1}		VREXT -0.1	VREXT	VREXT +0.1	
	V_{ID2}		Vcc - 0.1	—	Vcc	
VLOUT load current	ΔVI	Except Supply current	—	—	15	mA

Definition of input DATA (DATA-IN) and allowable width of jitter

The following figure shows representatively the allowable width of jitter because the transition of potential is monitored after Slave address communication after Start command. In all communications, if the jitter width is within tJIT, the receiving can be reliable.



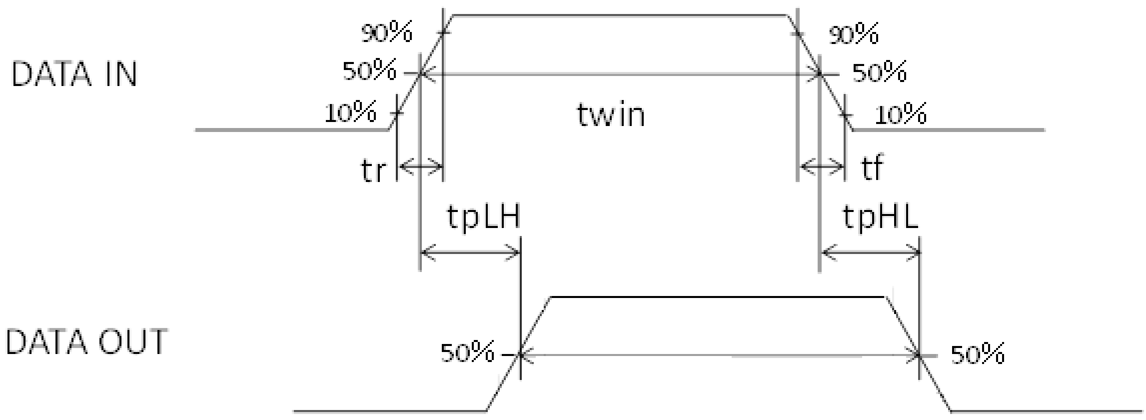
Note: Output format of control signal port

CMOS push-pull type is recommended for the output port of the controller.
When the open-drain output is used, the potential transition of H communication and L communication may not be same Duty, and the duty narrows the allowable jitter width. Therefore, pay attention to the communication wave.

Electrical Characteristics (T_a=25°C, VL=15V, Vcc=VLOUT, Unless otherwise specified)

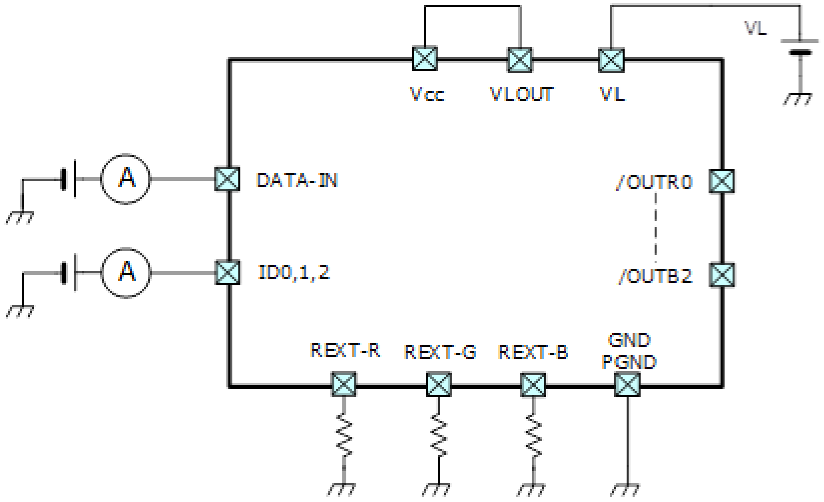
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output Current	I_{OUT1}	V_{OUT} =0.5V, REXT = 1.2kΩ	12.5	13.3	14.1	mA
Output Current Accuracy between channels	ΔI_{OUT2}	V_{OUT} = 0.5V, REXT =1.2kΩ All output ON	—	—	±3.0	%
Output leakage current	I_{OZ}	V_{OUT} = 28 V	—	—	1	μA
VLOUT pin voltage	VLout	—	4.5	—	5.5	V
Input current	I_{IH}	DATAIN	—	—	1	μA
	I_{IL}	DATAIN	—	—	-1	
	I_{ID}	ID0, ID1, ID2	—	—	±10	
Changes in constant output current dependent on Vcc	%/Vcc	Vcc = 4.5 V to 5.5 V	—	1	2	%
Supply Current	Icc (VL)	When applied VL=15 V REXT =1.2kΩ, V_{OUT} =0.5V,	—	7.8	15	mA
	Icc (Vcc)	When connected VL=GND REXT =1.2kΩ, V_{OUT} =0.5V,	—	7.4	12	
H Level DATA OUT Pin Output Voltage	VOH	IOH= -1mA	Vcc -0.4	—	—	V
L Level DATA OUT Pin Output Voltage	VOL	IOL= 1mA	—	—	0.4	V
DATAIN-DATAOUT Propagation Delay Time (Note)	tpLH	CL=15pF, tr=tf=3ns	—	—	20	ns
	tpHL		—	—	20	
PWM reference frequency	fPWM	Reference frequency of internal PWM counter	—	70	—	kHz

Note: DATA IN - DATA OUT definition

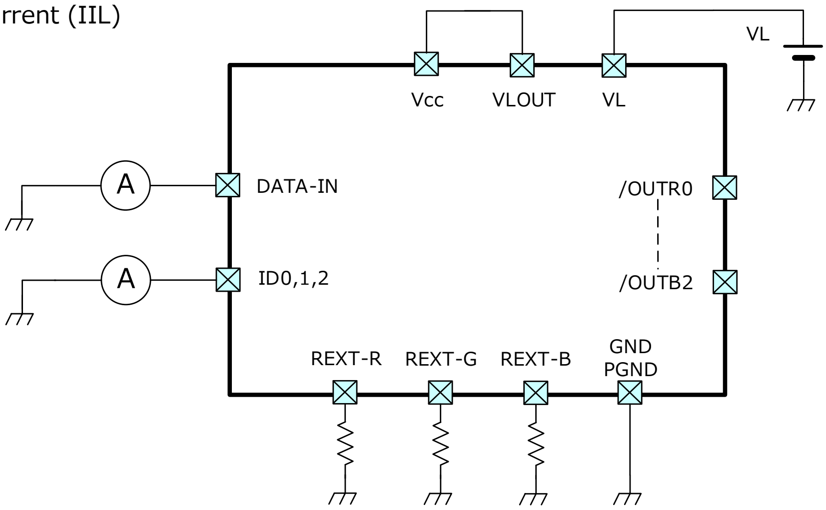


Test Circuit

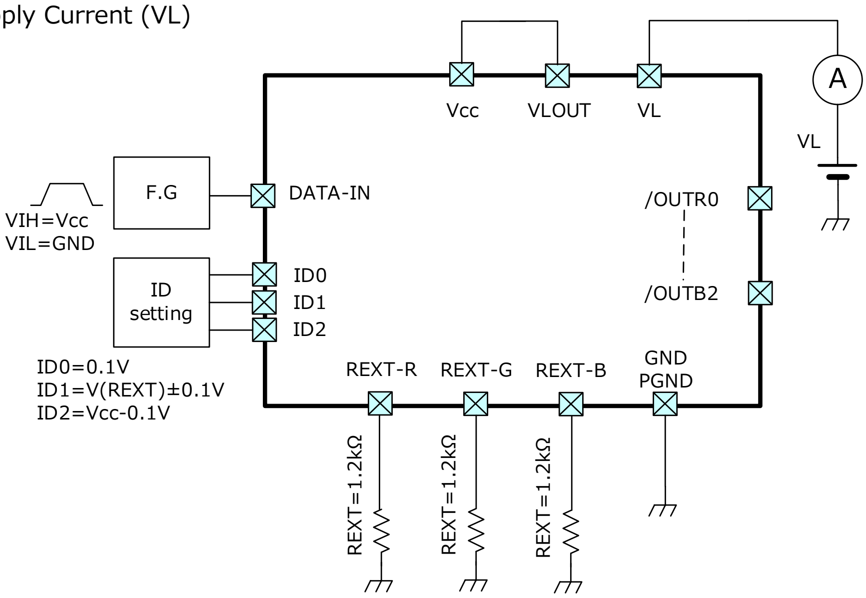
Test Circuit 1 Input Current (IIH)



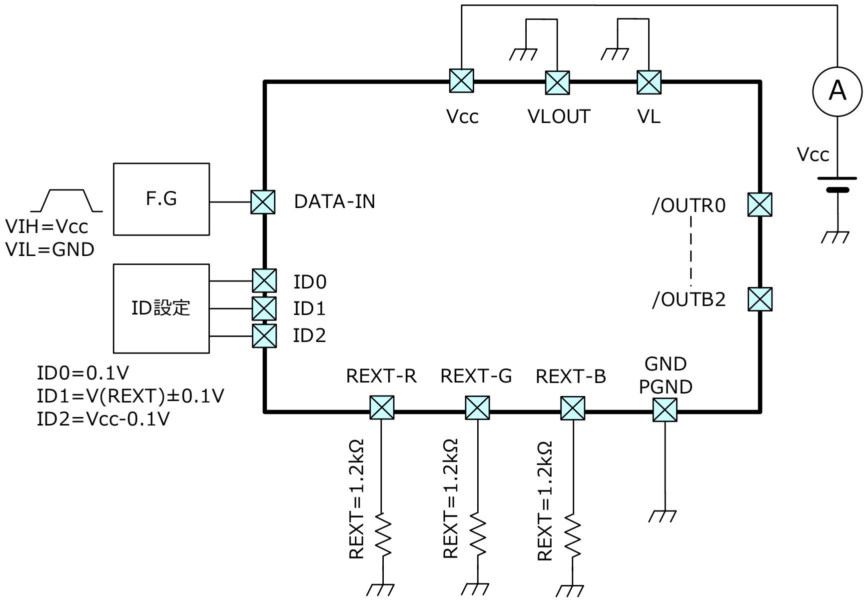
Test Circuit 2 Input Current (IIL)



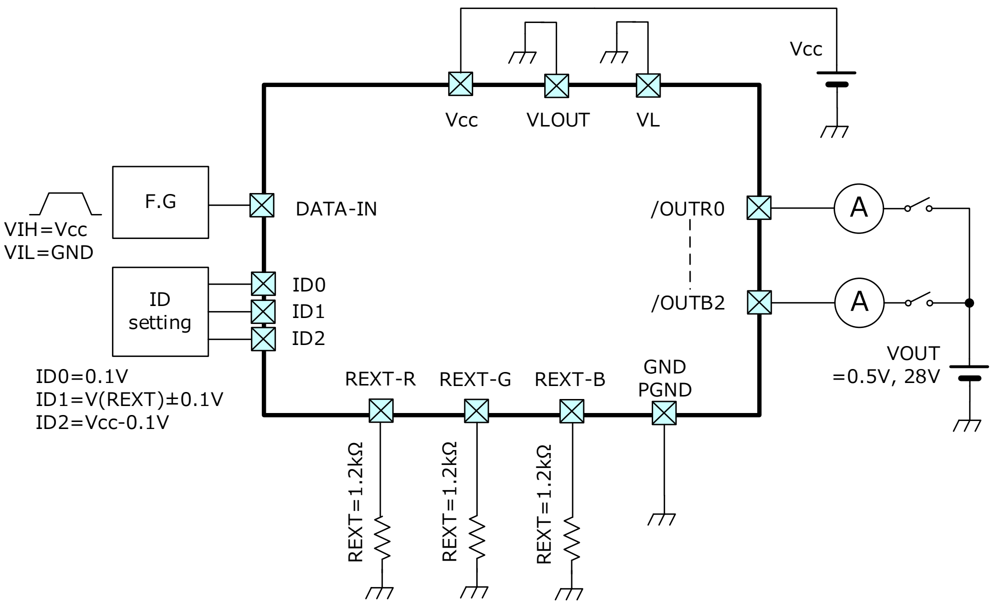
Test Circuit 3 Supply Current (VL)



Test Circuit 4 Supply Current(Vcc)

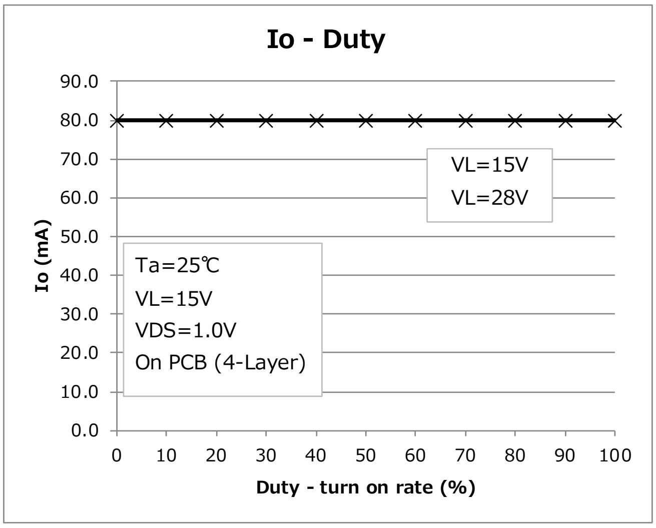


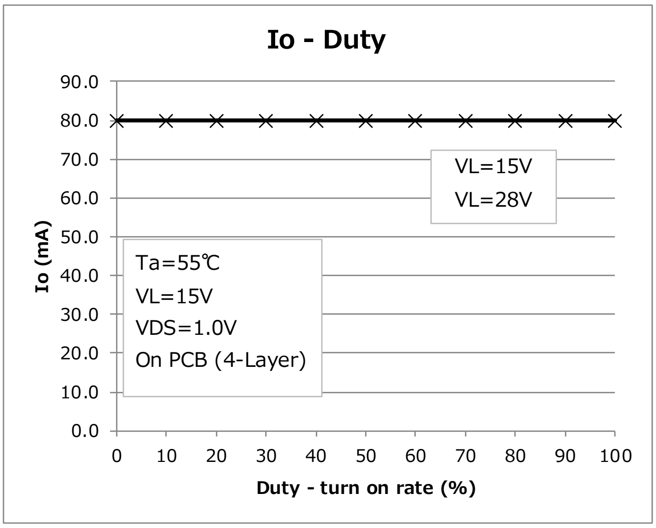
Test Circuit5 Output Current/ Output Leakage Current/ Output Current Accuracy/ Changes in Constant Output current dependent on Vcc

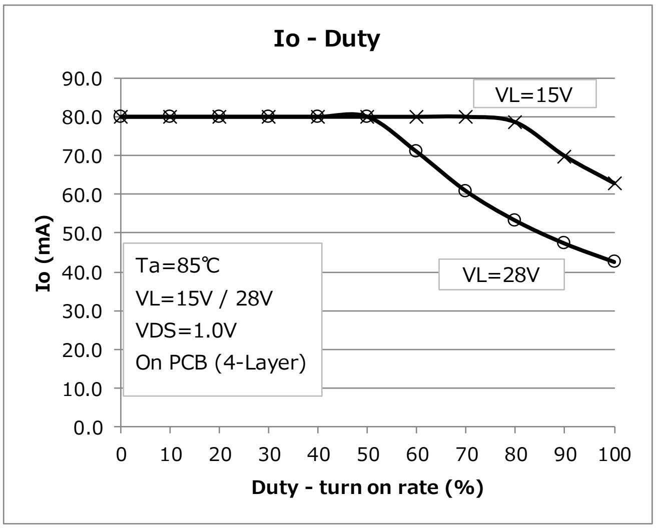


Output current - derating (illuminating rate) graph

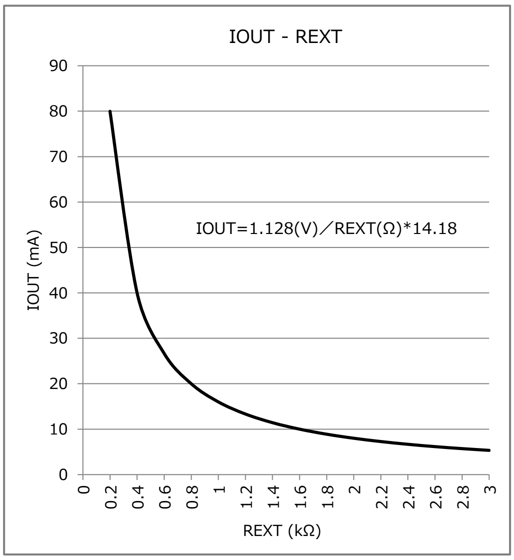
Board condition: Material: FR-4 (Compliant with JEDEC 4 layers board), Board size: 76.2×114.3×1.6 mm
When the pulse width is 25 ms or more, it is regarded as DC.



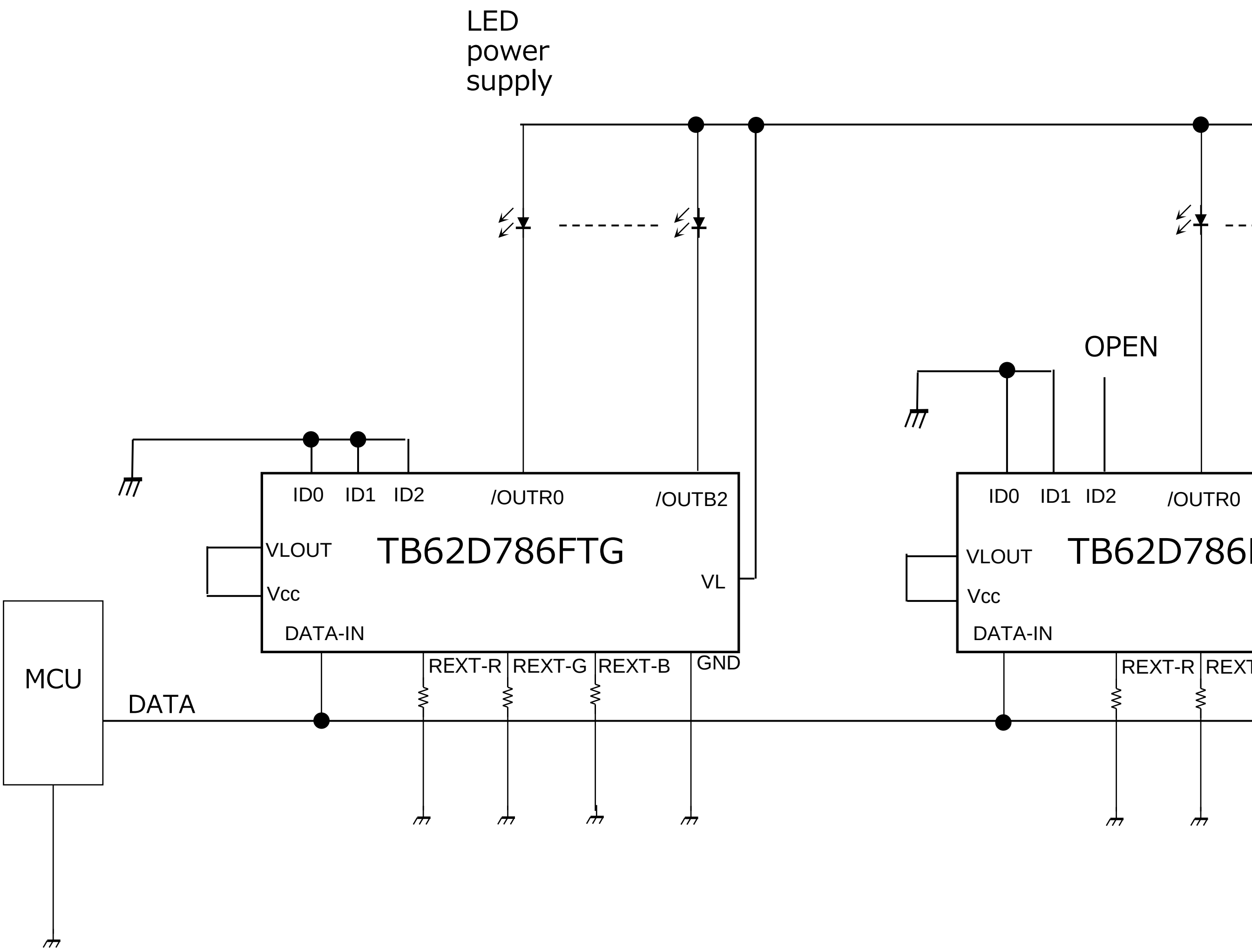




Output current - external resistance characteristic (typ.)



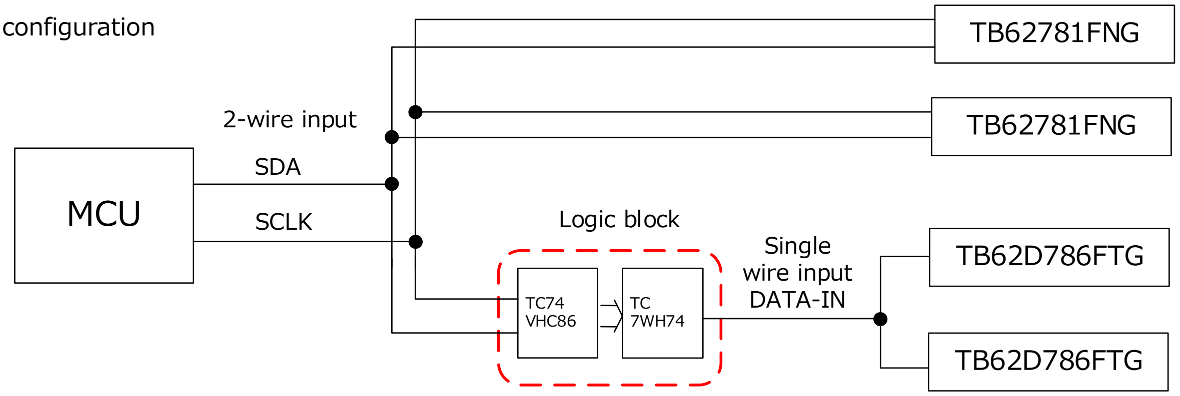
Application circuit example 1



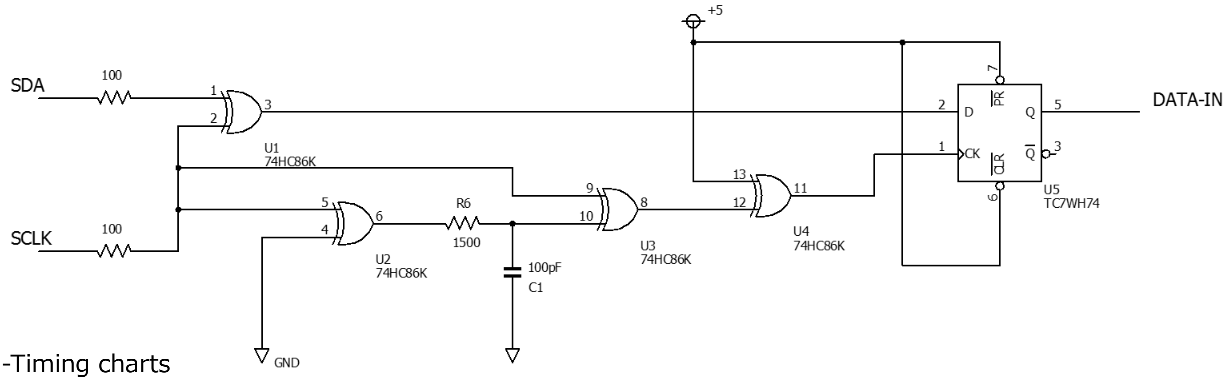
Application circuit example 2

When this product is controlled from same MCU ports of TB62781FNG, which is 2-wire input control LED driver, need to connect the Exclusive-OR gate (TC74VHC86) and D-Flip/Flop to preceding phase of the input of this product as shown below.
Since phase differences between DATA from MCU outputting and clock may occur, confirm the operation enough with the following configuration.

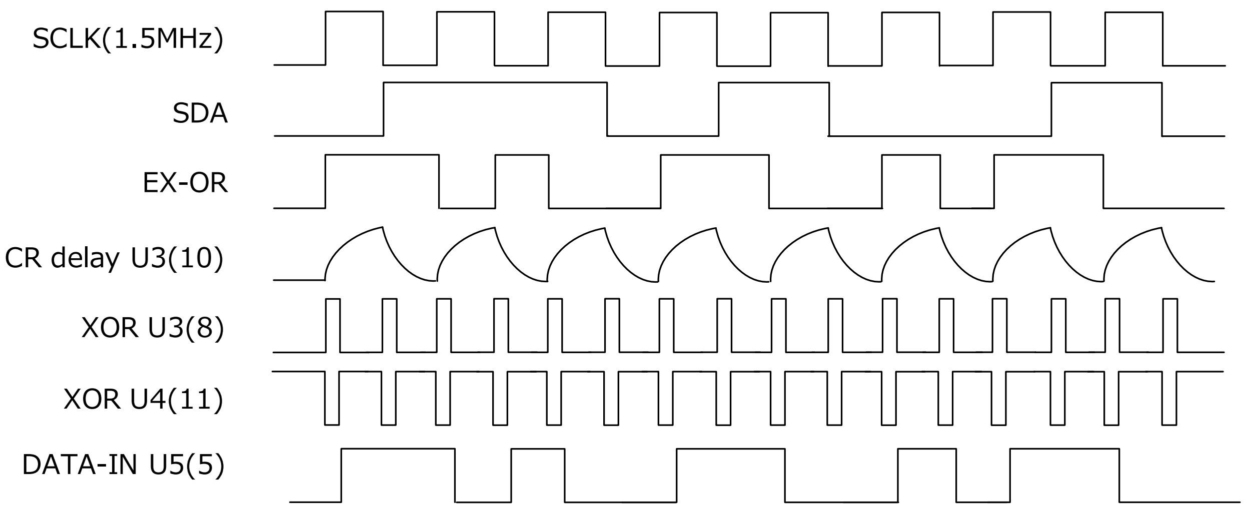
-System configuration



-Logic



-Timing charts

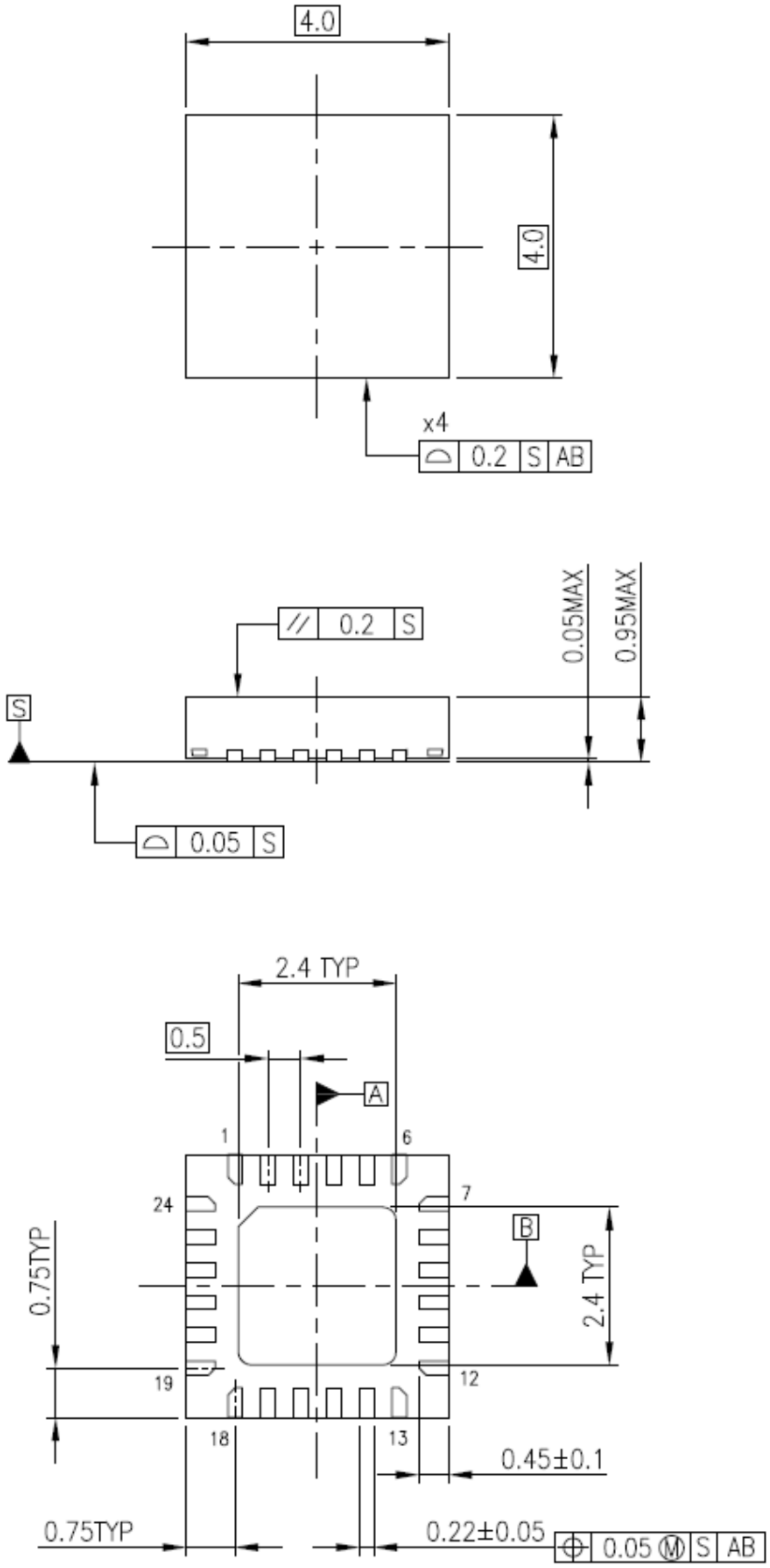


Note: When this circuit is used, the interval period should be fixed to SDA=SCLK=H.

Package Dimensions

P-VQFN24-0404-0.50-001

Unit: mm



Weight: 0.037g (Typ.)

Notes of Contents

1. Block diagram

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing charts

Timing charts may be simplified for explanatory purposes.

4. Application circuit example

The application circuit examples shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

5. Test circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative pins of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(3) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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