TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6613FTG

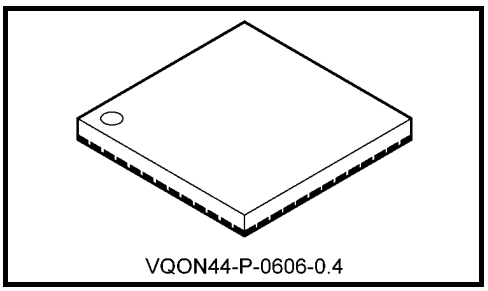
DC and Stepping Motor Driver

The TB6613FTG is a DC motor driver IC using LDMOS output transistors with low ON-resistance.

The TB6613FTG incorporates five PWM constant-current H-bridge drivers, of which four drivers can be used for micro stepping motor drives of up to two stepping motors.

The TB6613FTG is best suited to control various lens actuators in digital still cameras.

The three-wire serial interface provides control over the drivers, thus reducing the number of lines required for interfacing with the control IC.



Weight: 0.05 g (typ.)

Features

- Motor power supply voltage: VM ≤ 6 V (max)
- Control power supply voltage: V_{CC} = 3 V to 5.5 V
- Output current: I_{OUT} ≤ 0.8 A (max)
- Complementally P- and N-channel LDMOS output transistors
- Output ON-resistance: R_{ON} (upper and lower sum) = 1.5 Ω (@VM = V_{CC} = 5 V typ.)

Channels A, B, C and D

- Four H-bridge drivers capable of PWM constant-current control
  Supports up to two two-phase bipolar stepping motors (STMs) or up to four actuators.
- Each channel is individually configurable for either H-Bridge mode or STM μStep mode via the serial interface.
- In STM μStep mode, the micro stepping resolution is selectable from 6 bits (256 steps per full cycle) or 1 bit (8 steps per full cycle).

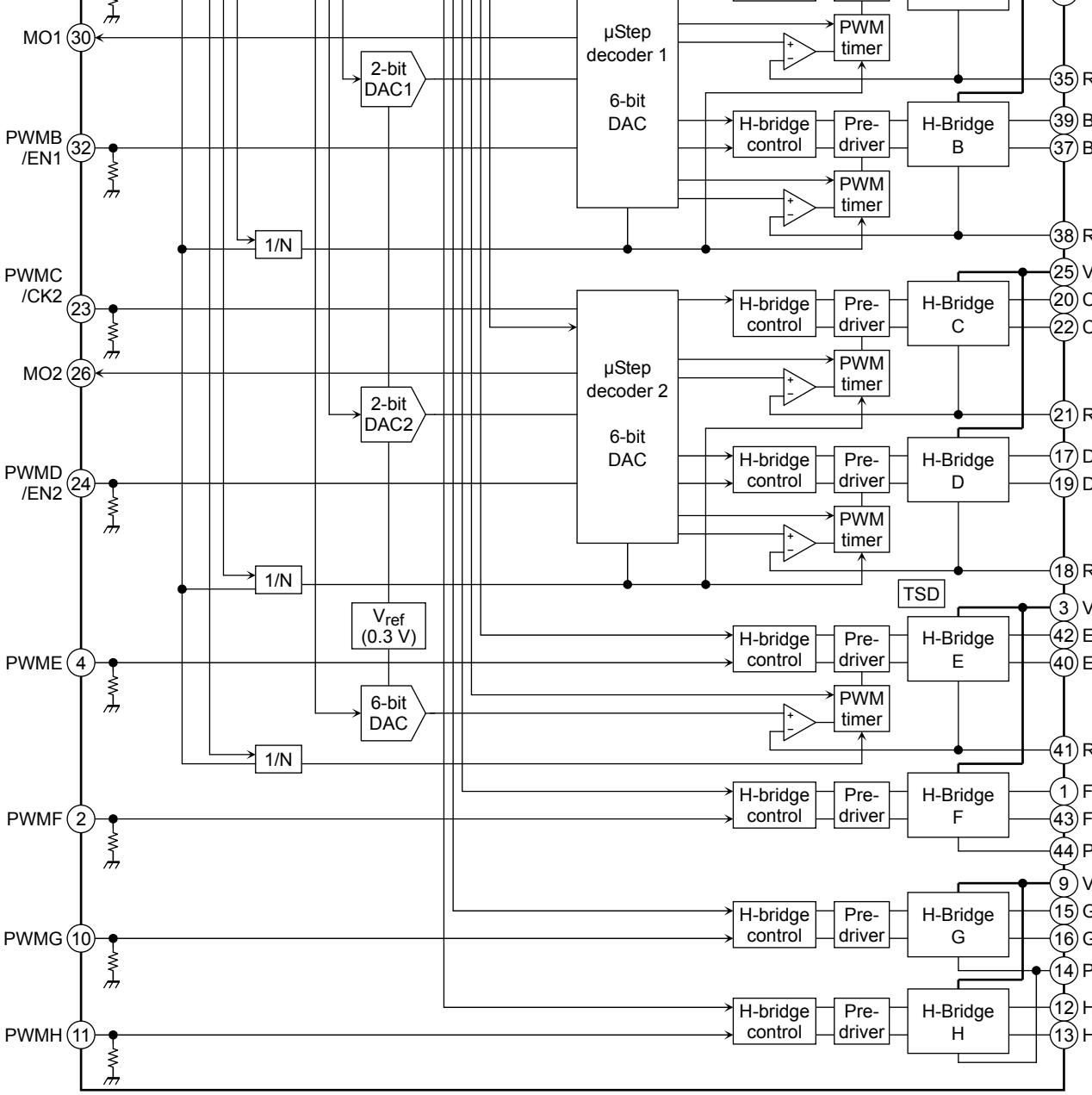
Channel E

- One PWM constant-current driver
- The constant-current reference voltage (Vref) is programmable via the internal 6-bit DAC.

Other Features

- Each channel has a DAC for setting constant-current values (Channels A to D = 2 bits in H-Bridge mode and 2 bits × 6 bits in μStep mode; Channel E = 6 bits)
- Dedicated standby (power-save) pin
- Thermal shutdown (TSD)
- Undervoltage lockout (UVLO): Resets and disables the internal circuitry when V_{CC} falls below 2.2 V (typ.).
- Small VQON44 package (0.4-mm lead pitch)

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.


MO1 30
PWMB /EN1 32
PWMC /CK2 23
MO2 26
PWMD /EN2 24
PWME 4
PWMF 2
PWMG 10
PWMH 11
2-bit DAC1
2-bit DAC2
6-bit DAC
1/N
1/N
1/N
µStep decoder 1
6-bit DAC
µStep decoder 2
6-bit DAC
PWM timer
H-bridge control
Pre-driver
H-Bridge B
H-Bridge C
H-Bridge D
H-Bridge E
H-Bridge F
H-Bridge G
H-Bridge H
TSD
V_{ref} (0.3 V)

Pin Function

No.	Pin Name	I/O	Function
1	FO1	O	Channel-F output 1
2	PWMF	I	PWM signal input (Channel F)
3	VM3	—	Motor power supply 3 (Channels E and F)
4	PWME	I	PWM signal input (Channel E)
5	V_{CC}	—	Power supply
6	MCK	I	Clock input for constant-current control
7	GND	—	Ground
8	STBY	I	Standby (power-save) control
9	VM4	—	Motor power supply 4 (Channels G and H)
10	PWMG	I	PWM signal input (Channel G)
11	PWMH	I	PWM signal input (Channel H)
12	HO1	O	Channel-H output 1
13	HO2	O	Channel-H output 2
14	PGND2	—	Motor ground 2 (Channels G and H)
15	GO1	O	Channel-G output 1
16	GO2	O	Channel-G output 2
17	DO1	O	Channel-D output 1
18	RFD	—	Connection pin for a current-sensing resistor (Channel D)
19	DO2	O	Channel-D output 2
20	CO1	O	Channel-C output 1
21	RFC	—	Connection pin for a current-sensing resistor (Channel C)
22	CO2	O	Channel-C output 2
23	PWMC/CK2	I	PWM signal input (Channel C)/μStep clock input 2
24	PWMD/EN2	I	PWM signal input (Channel D)/STM enable input 2
25	VM2	—	Motor power supply 2 (Channels C and D)
26	MO2	O	STM electrical degree monitor output 2, Open-drain output, need ext. pull-up resistor
27	DATA	I	Serial data input
28	CK	I	Serial clock input
29	LD	I	Serial load enable
30	MO1	O	STM electrical degree monitor output 1, Open-drain output, need ext. pull-up resistor
31	VM1	—	Motor power supply 1 (Channels A and B)
32	PWMB/EN1	I	PWM signal input (Channel B)/STM enable input 1
33	PWMA/CK1	I	PWM signal input (Channel A)/μStep clock input 1
34	AO2	O	Channel-A output 2
35	RFA	—	Connection pin for a current-sensing resistor (Channel A)
36	AO1	O	Channel-A output 1
37	BO2	O	Channel-B output 2
38	RFB	—	Connection pin for a current-sensing resistor (Channel B)
39	BO1	O	Channel-B output 1
40	EO2	O	Channel-E output 2
41	RFE	—	Connection pin for a current-sensing resistor (Channel E)
42	EO1	O	Channel-E output 1
43	FO2	O	Channel-F output 2
44	PGND1	—	Motor ground 1 (Channel F)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	6	V	V_{CC}
Motor supply voltage	VM	6	V	VM
Output voltage	V_{OUT}	−0.2 to 6	V	Channels A to H
	V_{MO}	V_{CC}	V	MO1, MO2 (Open-drain)
Output current	I_{OUT}	0.8	A	Channels A to H
	I_{MO}	1	mA	MO1, MO2 (Open-drain)
Input voltage	V_{IN}	−0.2 to 6	V	Control input pins
Power dissipation	P_D	4.17	W	Note
Operating temperature	T_{opr}	−20 to 85	°C	
Storage temperature	T_{stg}	−55 to 150	°C	

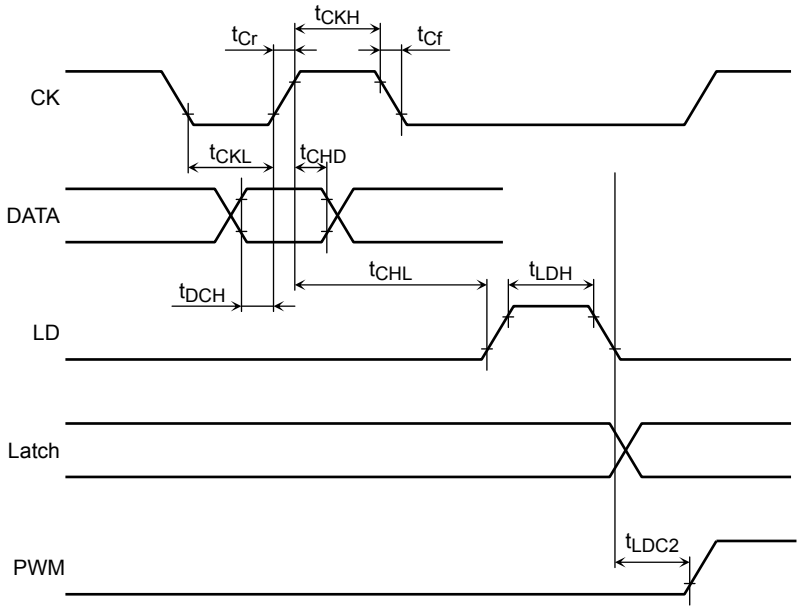
Note: When mounted on a single-side glass epoxy PCB (size: 76.4 mm × 114.3 mm × 1.6 mm) with a 40% dissipating copper surface.

Operating Conditions 1 (Ta = −20 to 85°C)

Characteristics	Symbol	Rating			Unit	Remarks
		Min	Typ.	Max		
Supply voltage for small-signal circuitry	V_{CC}	3	3.3	5.5	V	
Motor supply voltage	VM	2.5	—	5.5	V	
Output current	I_{OUT}	—	—	600	mA	VM = 3 to 5.5 V
		—	—	250		2.2 V ≤ VM ≤ 3 V
PWM frequency	f_{PWM}	—	—	100	kHz	
Master clock frequency	f_{MCK}	—	1	5	MHz	

Operating Conditions 2: Serial Data Controller (Ta = −20°C to 85°C)

Characteristics	Symbol	Rating		Unit
		Min	Max	
Clock pulse width Low	t_{CKL}	200	—	ns
Clock pulse width High	t_{CKH}	200	—	ns
Clock rise time	t_{Cr}	—	50	ns
Clock fall time	t_{Cf}	—	50	ns
Data setup time	t_{DCH}	30	—	ns
Data hold time	t_{CHD}	60	—	ns
CK to LD rising edge	t_{CHL}	200	—	ns
LD to PWM delay	t_{LDC2}	100	—	ns
Load pulse width High	t_{LDH}	2	—	μs
CK frequency	f_{CLK}	—	2.5	MHz



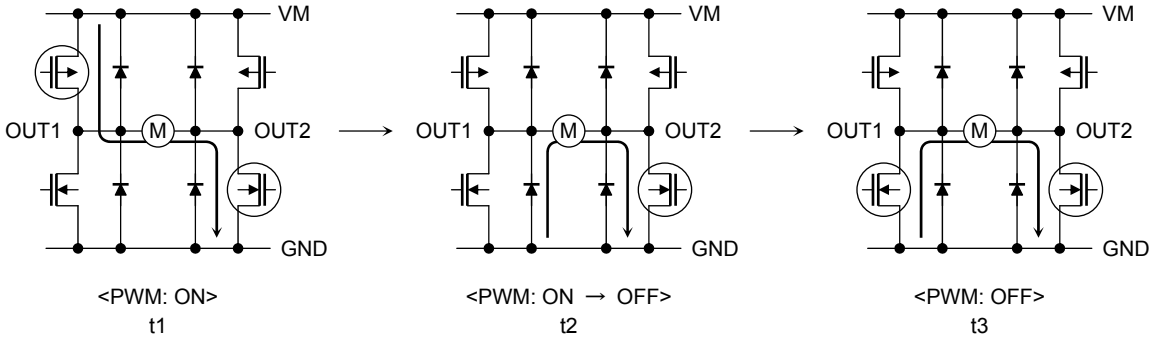
Principle of Operation

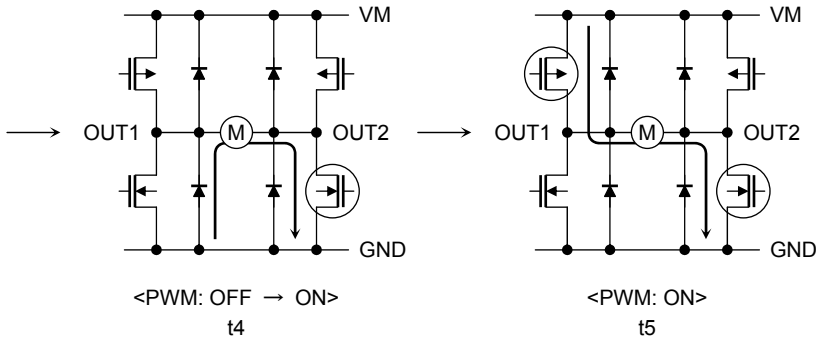
Bridge Outputs: Channels A through H

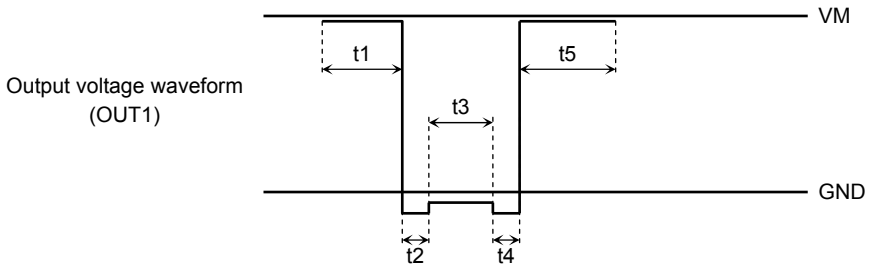
PWM Control

In PWM constant-current mode, the PWM chopper circuit alternates between on (t1, t5) and short brake (t3).

(To eliminate shoot-through current, a dead time (t2, t4) of 50 ns (design target only) is inserted when the PWM is turned on and off.)







Constant current control on H-bridge driver; Off-time fixed PWM constant current chopping operation

TB6613FTG operates Constant Current Control with off-time-fixed PWM operation.

The chop-off time is fixed by counting internally the external input driving clock, so the chop-off time could be adjusted by changing the frequency of driving clock or the number of internal counting (2, 4, 6, 8 counts(4steps) are selectable).

<Ex; Operation on four clock-counts>

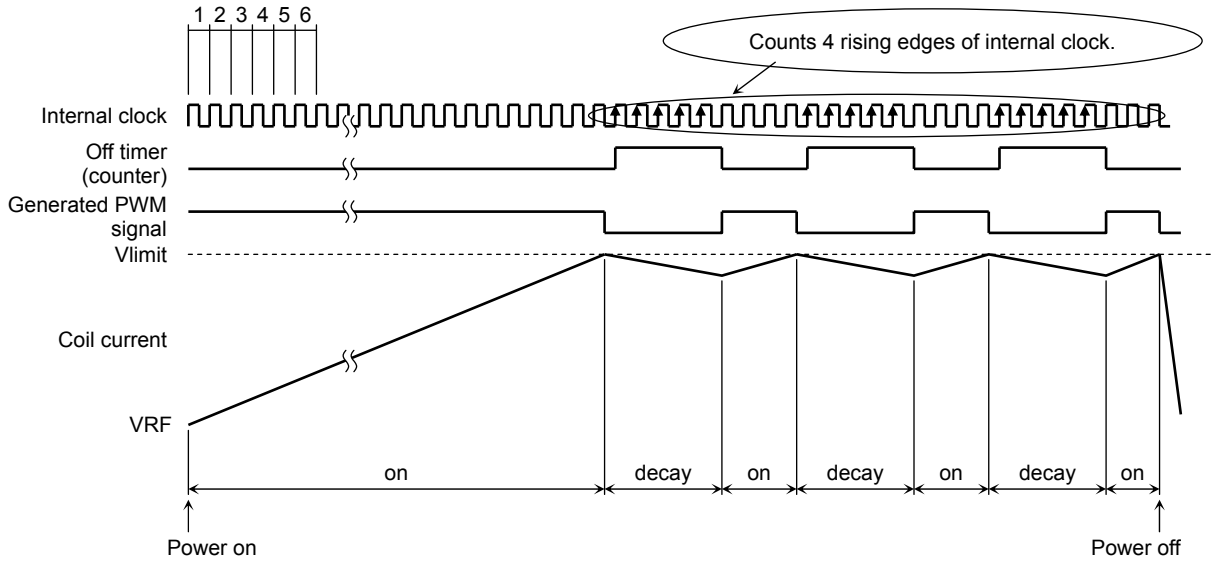
First, motor coil current is generated on chop-on starting, and when the voltage (VRF) on external current-sensing resistor rise and reach the reference voltage Vlimit (means current limit level) the current is to off on comparator operation.

The chop-off time is fixed with 4bits of internal clock counting from the first rising edge of internal clock just after the output high-side transistor is turned off.

(The counter is reset on the fifth rising edge of the internal clock)

This chop-off time control generates the PWM signal to drive On/Off the output transistors.

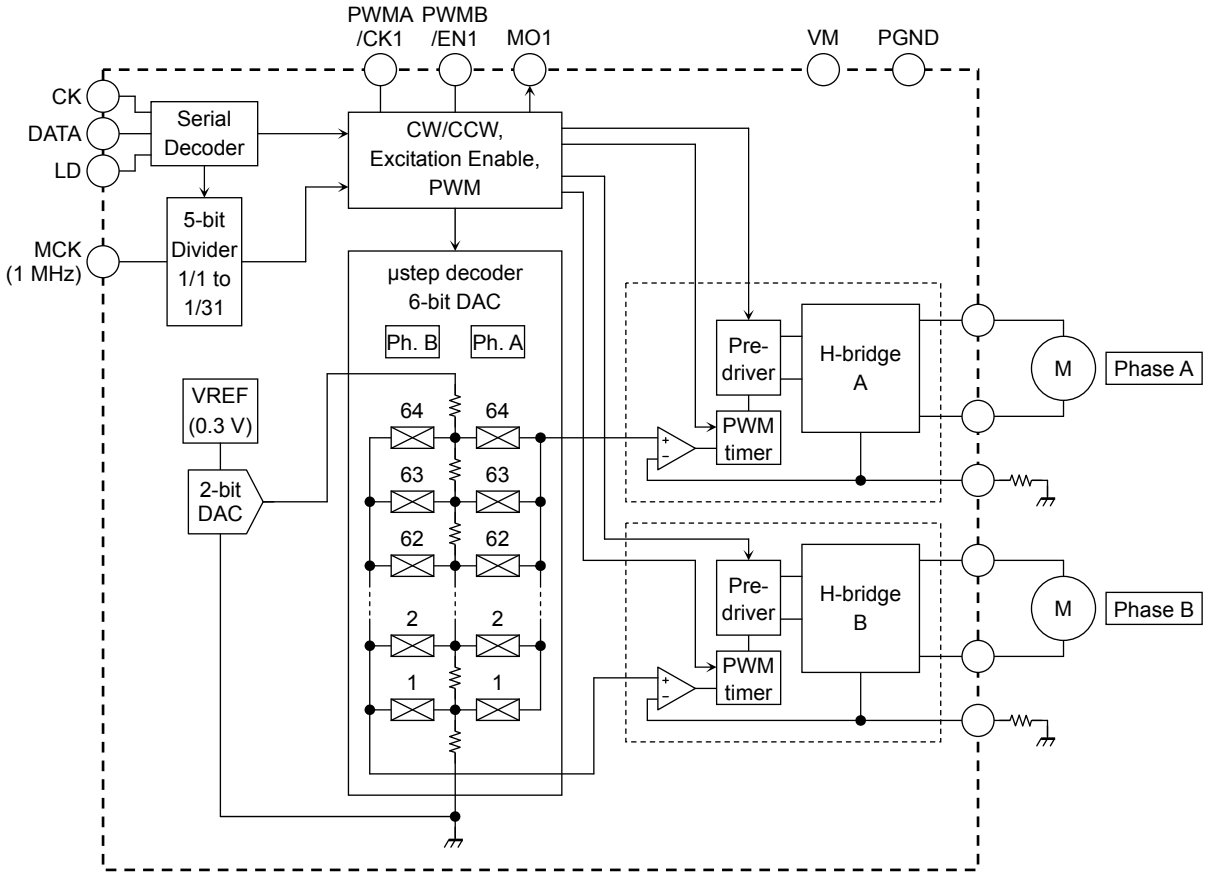
Timing Diagram of the PWM Constant-Current Chopper Circuit with a Turn-Off Period of Four Clock Cycles



(The upper limit of the coil current (IO peak) can be calculated as: IO = Vlimit/RNF.)

Micro step Control: Channels A, B, C and D

In PWM constant-current mode, when the TB6613FTG generates a PWM signal, it measures a constant turn-off period by counting the number of rising edges of the internal clock signal (divided clock of MCK).



- Pulse clock control: The TB6613FTG steps up the current at each rising edge of the clock input to the PWMA/CK1 (for channels A and B) or PWMC/CK2 (for channels C and D) pin. (Current step-ups actually occur synchronous to the internal clock signal derived from MCK.)

- µStep modes: Selectable from the following two modes:
  1-bit mode: 8 steps per full cycle
  6-bit mode: resolution = 256 steps per full cycle

- Enable control: Setting PWMB/EN1 (for channels A and B) or PWMD/EN2 (for channels C and D) High and Low enables and disables motor excitation.
  ENn = 1: Excitation enabled; ENn = 0: Excitation disabled

- Current decay modes: In STM µStep mode, the motor current recirculates back to the power supply in Fast-Decay mode when the Vref level changes during current step-down. The current decay rate is selectable from four modes.

- Electrical degree monitor: As the output current increases or decreases in steps with the CK input, a negative pulse is generated from the MO1 (or MO2) pin at every 90 or 360 electrical degrees.

- PWM chopping frequency: The PWM signal is generated by dividing the external MCK signal by up to 31, as programmed in a 5-bit register.

- Turn-off period: The turn-off period is selectable from 2, 4, 6 and 8 cycles of the internal clock signal, which is generated by dividing MCK internally.

- Constant-current setting: The maximum Vref voltage can be selected from 0.3 V, 0.225 V, 0.15 V and 0.075 V with a 2-bit DAC based on the 0.3-V on-chip reference voltage.
  This DAC output is divided by the 6-bit DAC under control of the micro step decoder to establish Vref for constant-current control.

Current Decay Mode: Only Applicable for Step-Down Control in STM μStep Mode

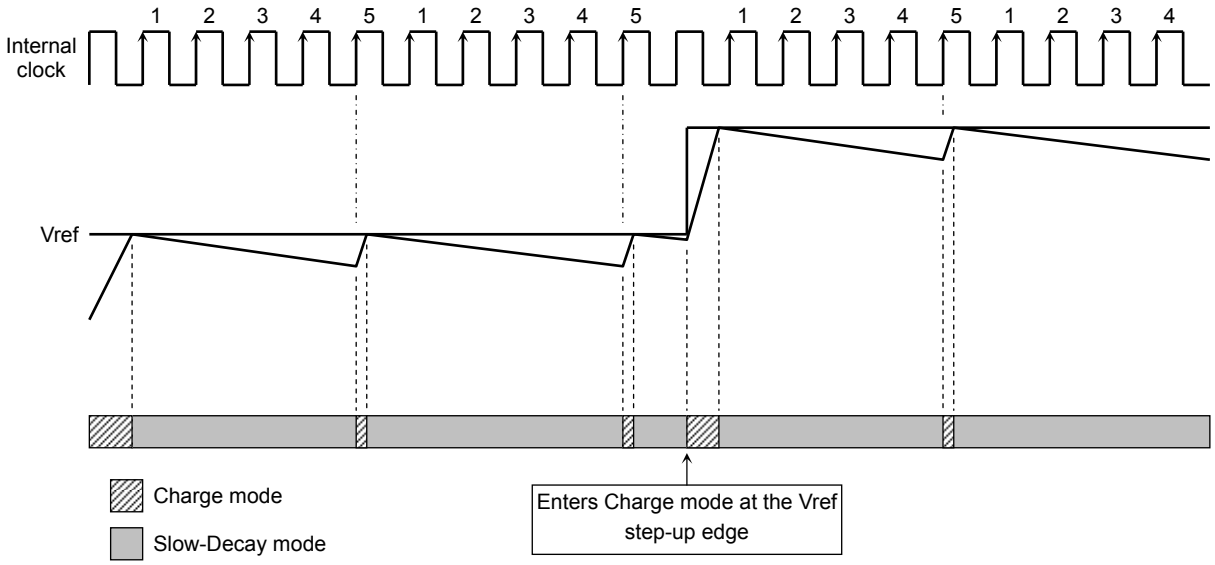
In STM μStep mode, the output current step-down slope may not match the changes of the target current level specified by Vref depending on the time constant of a motor coil, thus leading to a big distortion from the desired output current waveform.

To improve the matching between the output current and the target current level, the TB6613FTG enters Fast-Decay mode very briefly immediately after each Vref step-down. In this mode, the output current recirculates back to the power supply.

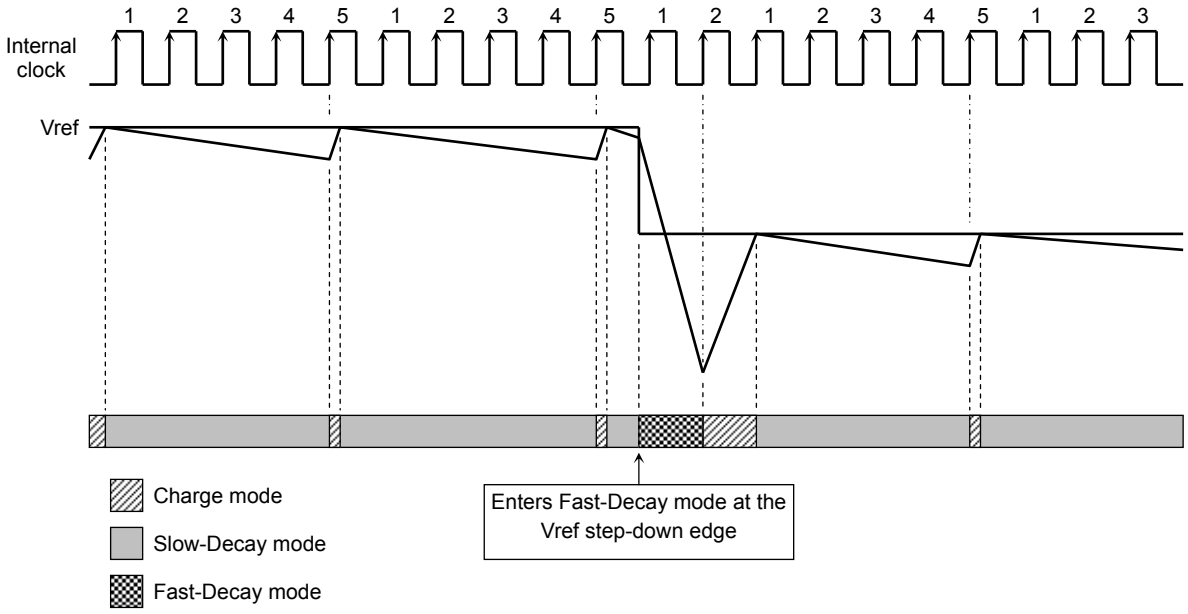
The Fast-Decay time is generated by counting the internal clock signal and selectable from the four modes listed below:

Fast-Decay Mode	Number of Internal Clock Cycle	Decay Rate
Fast0	0	No
Fast1	1	Small
Fast2	2	Medium
Fast3	3	Large

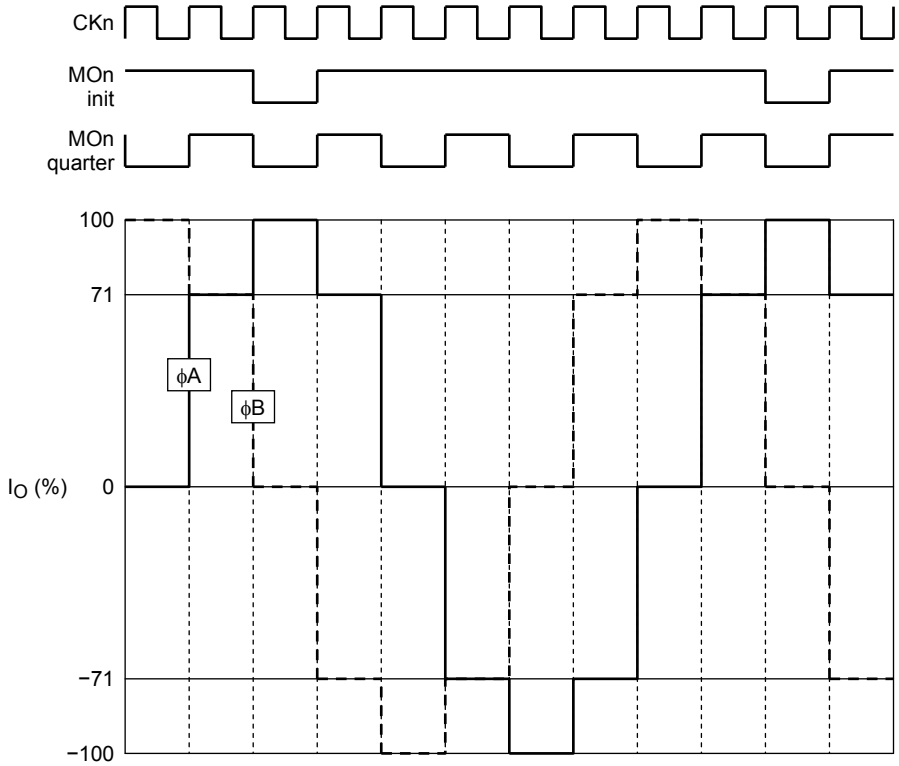
Current Step-Up Slope



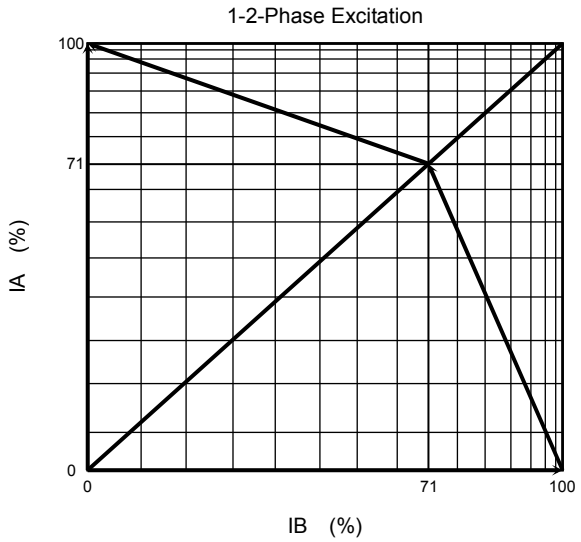
Current Step-Down Slope (when in Fast1 mode)



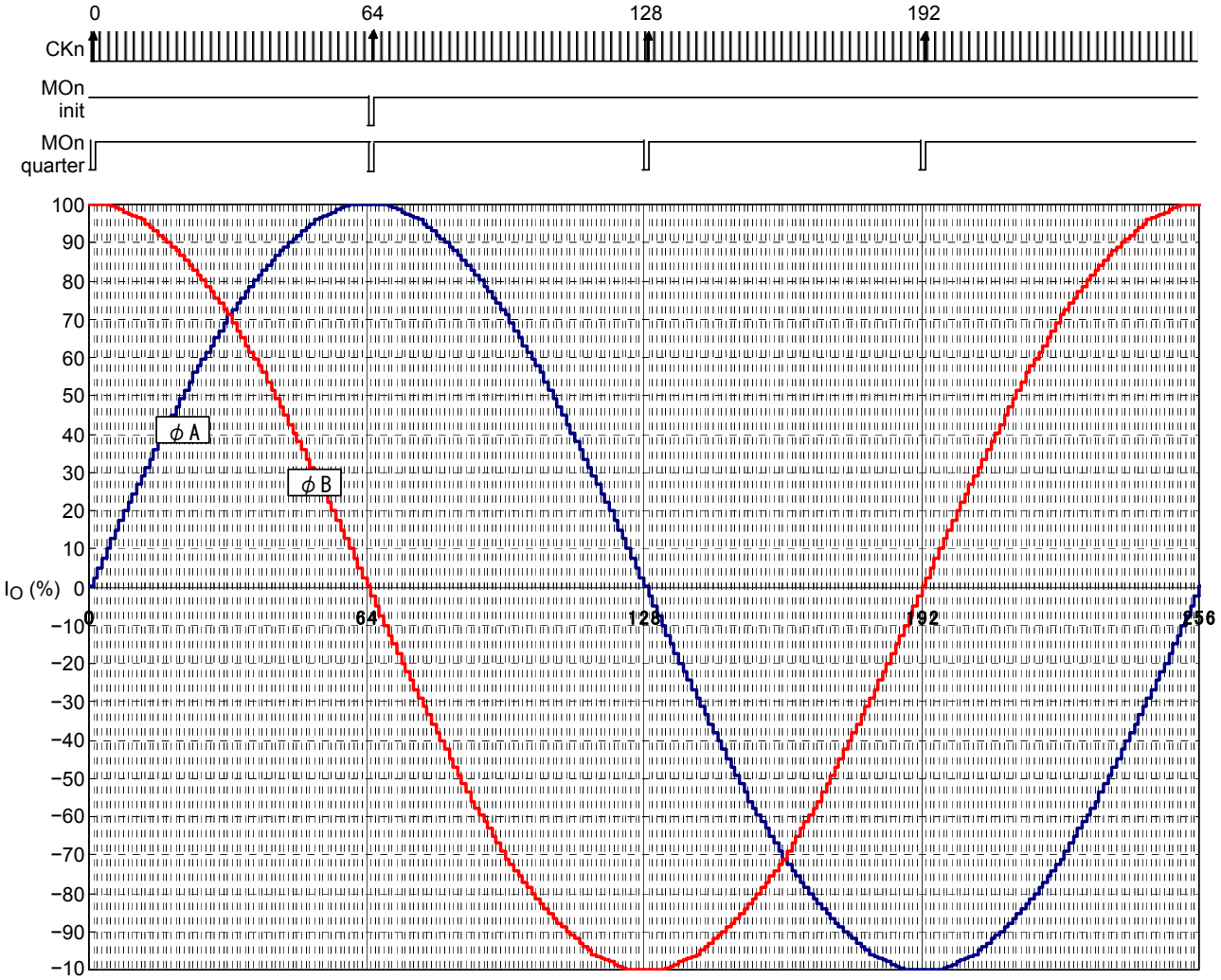
Timing Diagram of Micro step Operation with 1-Bit Resolution (8 steps per full cycle)



Output Current Vector

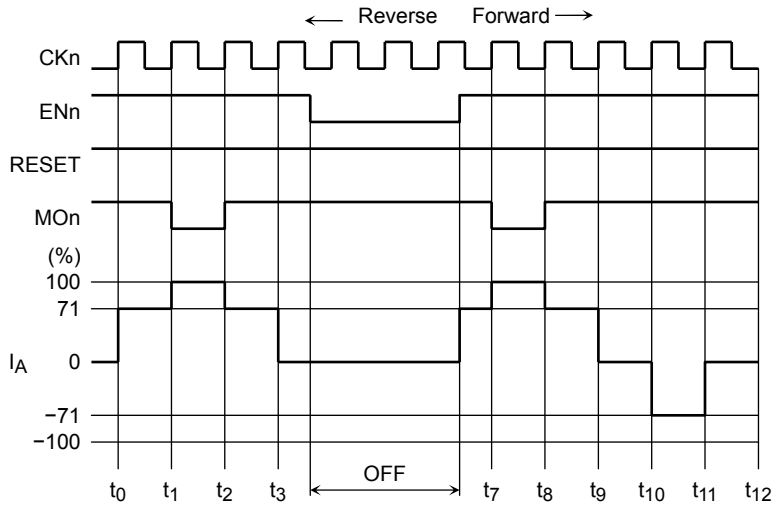


Timing Diagram of Micro step Operation with 6-Bit Resolution (256 steps per full cycle)



Relationship between the Enable and RESET Inputs and Output Signals

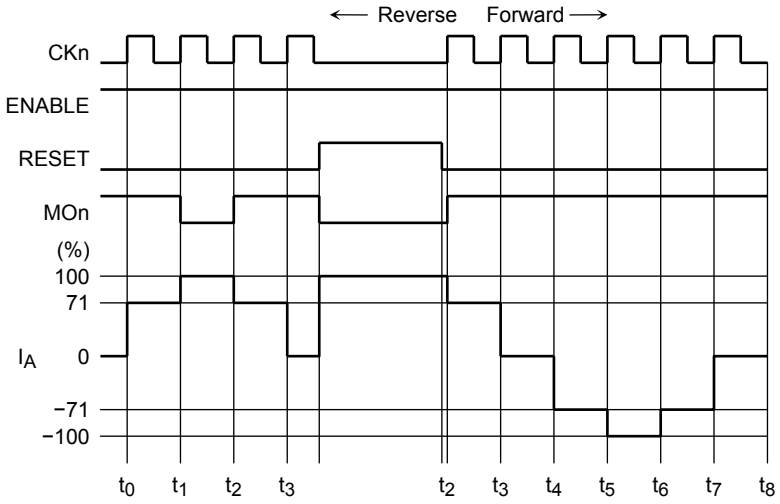
Enable (ENn Pin)



Setting the ENn signal Low disables only the output block, and the internal circuitry continues to operate in accordance with the CKn input. Therefore, when the ENn signal is set High again, the output current restarts as if phases had proceeded with the CKn signal.

When ENn = Low, the output signals are disabled regardless of the state of the RESET signal.
Setting the RESET signal Low while ENn = Low resets the counter.

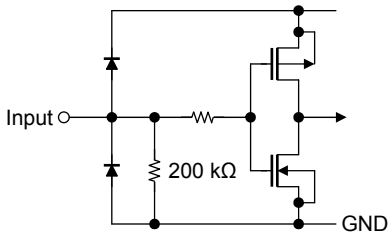
RESET (Serial Command)



Setting the RESET signal High causes the outputs to be put in the Initial state and the MOn output to be driven Low.
When the RESET signal goes is set Low again, the output current generation restarts from the Initial state at the next rising edge of CKn.

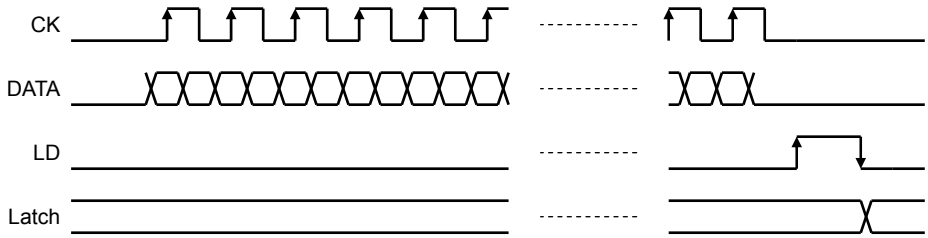
Input Pins

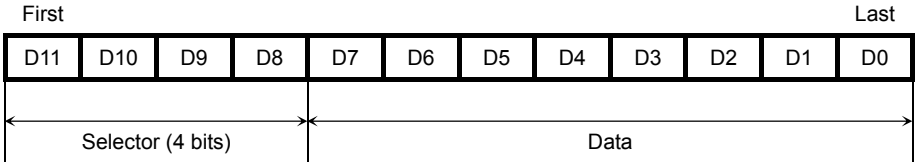
All input pins (CK, DATA, LD, PWMA/CK1, PWMB/EN1, PWMC/CK2, PWMD/EN2, PWME, PWMF, PWMG, PWMH, STBY, MCK) have a pull-down resister of about 200 kΩ.



Serial Data Format

12-Bit Serial Data





Register Organizations

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
0	0	0	0	mod1	stm1	if1	ick1: 5 bits					0
0	0	0	1	2-bit DAC1		mdr1	rst1	mo1	off1		—	1
0	0	1	0	p1a	p1b	sdfst1		scw1	—	—	—	2
0	0	1	1	mod2	p2a	p2b	if2	off2		—	—	3
0	1	0	0	mod3	stm3	if3	ick3: 5 bits					4
0	1	0	1	2-bit DAC2		mdr3	rst3	mo3	off3		—	5
0	1	1	0	p3a	p3b	Sdfst3		scw3	—	—	—	6
0	1	1	1	mod4	p4a	p4b	if4	off4		—	—	7
1	0	0	0	mod5	if5	6-bit DAC						8
1	0	0	1	off5		—	ick5: 5 bits					9
1	0	1	0	p5a	p5b	—	—	—	—	—	—	10
1	0	1	1	mod6	p6a	p6b	—	—	—	—	—	11
1	1	0	0	mod7	p7a	p7b	—	—	—	—	—	12
1	1	0	1	mod8	p8a	p8b	—	—	—	—	—	13
1	1	1	0	Don't access								14
1	1	1	1									15

modx	: H-bridge control	0 = Direct PWM mode (Table 1) 1 = Control mode of Table 2 (All channels)
stmx	: STM mode select	0 = H-Bridge mode 1 = STM µStep mode (*)
ifx	: Constant-current control	0 = Constant-current control disabled 1 = Constant-current control enabled (Channels A, B, C, D and E) * Valid only in H-Bridge mode (stmx = 0). Constant-current control is always enabled in STM µStep mode.
2-bit DACx	: 2-bit DAC setting	0 = 0.075 V; 1 = 0.15 V; 2 = 0.225 V; 3 = 0.3 V 4 levels in 0.075-V steps (*)
ickx	: Divide ratio for internal clock*	Divides the external MCK by 1 to 31. (*, channel E)
mdrx	: STM excitation mode	0 = µStep mode with 6-bit resolution 1 = 1-2-phase excitation mode (*)

sdfstx	: Fast-Decay mode	Specifies the Fast-Decay time in number of internal clock cycles: 0 = No Fast-Decay cycle; 1 = 1 cycle; 2 = 2 cycles; 3 = 3 cycles (*)
scwx	: STM rotation direction select	0 = Forward; 1 = Reverse (*)
rstx	: STM step counter reset	0 = Count mode; 1 = Reset (*)
mox	: Monitor signal interval	0 = Every 360 electrical degree 1 = Every 90 electrical degree (*)
offx	: PWM turn-off period	Specifies the PWM turn-off period in number of internal clock cycles: 0 = 2 cycles; 1 = 4 cycles; 2 = 6 cycles; 3 = 8 cycles (*, channel E)
pxa	: H-bridge control input a	See Tables 1 and 2 on next page (All channels)
pxb	: H-bridge control input b	See Tables 1 and 2 on next page (All channels)
6-bit DAC	: Channel-E 6-bit DAC setting*	MSB = 0.3 V (6 bits) (Channel E)

Note: Two registers at addresses 3 and 7 are only valid in H-Bridge mode (stmx = 0).

*: Detailed descriptions of register settings are provided in the tables on the following pages.

**: Do not access to address-14 or address-15 as these are for IC-testing in Toshiba.

Supplemental Register Descriptions

1. Each channel or micro step pair is separately addressed.

Address	Corresponding Channels
0, 1, 2, 3	Channels A and B (stm1 = 1: micro step pair 1 (A&B))
4, 5, 6, 7	Channels C and D (stm3 = 1: micro step pair 2 (C&D))
8, 9, 10	Channel E
11	Channel F
12	Channel G
13	Channel H

Note: Two registers at addresses 3 (channel-B setting) and 7 (channel-D setting) are only valid in H-Bridge mode (stmx = 0).

2. The character x in register names represents a channel number.

x	Corresponding Channels
x = 1	Channel A (The settings of stmx, ickx, 2-bit DACx, mdrx, rstx, mox, sdfstx and scwx are shared between channels A and B.)
x = 2	Channel B
x = 3	Channel C (The settings of stmx, ickx, 2-bit DACx, mdrx, rstx, mox, sdfstx and scwx are shared between channels C and D.)
x = 4	Channel D
x = 5	Channel E
x = 6	Channel F
x = 7	Channel G
x = 8	Channel H

3. ickx: Setting the divide ratio for the external MCK used to generate the internal clock

The external MCK is divided to generate an internal clock, as specified for each channel (micro step pair) by D4, D3, D2, D1 and D0 at addresses 0 (for channels A and B), 4 (for channels C and D) and 8 (for channel E).

Decimal	Binary	Address 0, 4 or 8					Divide Ratio for Internal Clock
		D4	D3	D2	D1	D0	
1	00001	0	0	0	0	1	1/1
2	00010	0	0	0	1	0	1/2
3	00011	0	0	0	1	1	1/3
4	00100	0	0	1	0	0	1/4
5	00101	0	0	1	0	1	1/5
6	00110	0	0	1	1	0	1/6
7	00111	0	0	1	1	1	1/7
8	01000	0	1	0	0	0	1/8
9	01001	0	1	0	0	1	1/9
10	01010	0	1	0	1	0	1/10
11	01011	0	1	0	1	1	1/11
12	01100	0	1	1	0	0	1/12
13	01101	0	1	1	0	1	1/13
14	01110	0	1	1	1	0	1/14
15	01111	0	1	1	1	1	1/15
16	10000	1	0	0	0	0	1/16
17	10001	1	0	0	0	1	1/17
18	10010	1	0	0	1	0	1/18
19	10011	1	0	0	1	1	1/19
20	10100	1	0	1	0	0	1/20
21	10101	1	0	1	0	1	1/21
22	10110	1	0	1	1	0	1/22
23	10111	1	0	1	1	1	1/23
24	11000	1	1	0	0	0	1/24
25	11001	1	1	0	0	1	1/25
26	11010	1	1	0	1	0	1/26
27	11011	1	1	0	1	1	1/27
28	11100	1	1	1	0	0	1/28
29	11101	1	1	1	0	1	1/29
30	11110	1	1	1	1	0	1/30
31	11111	1	1	1	1	1	1/31

4. 6-bit DAC: Setting the 6-bit DAC for channel E

The Vref voltage that determines the target current level for constant-current control of channel E can be specified by D5, D4, D3, D2, D1 and D0 at address 8.
The target current level is determined by this voltage level and the external current sensing resistor.

Decimal	Binary	Address 8						Voltage (mV)
		D5	D4	D3	D2	D1	D0	
0	000000	0	0	0	0	0	0	0.0
1	000001	0	0	0	0	0	1	4.8
2	000010	0	0	0	0	1	0	9.5
3	000011	0	0	0	0	1	1	14.3
4	000100	0	0	0	1	0	0	19.0
5	000101	0	0	0	1	0	1	23.8
6	000110	0	0	0	1	1	0	28.6
7	000111	0	0	0	1	1	1	33.3
8	001000	0	0	1	0	0	0	38.1
9	001001	0	0	1	0	0	1	42.9
10	001010	0	0	1	0	1	0	47.6
11	001011	0	0	1	0	1	1	52.4
12	001100	0	0	1	1	0	0	57.1
13	001101	0	0	1	1	0	1	61.9
14	001110	0	0	1	1	1	0	66.7
15	001111	0	0	1	1	1	1	71.4
16	010000	0	1	0	0	0	0	76.2
17	010001	0	1	0	0	0	1	81.0
18	010010	0	1	0	0	1	0	85.7
19	010011	0	1	0	0	1	1	90.5
20	010100	0	1	0	1	0	0	95.2
21	010101	0	1	0	1	0	1	100.0
22	010110	0	1	0	1	1	0	104.8
23	010111	0	1	0	1	1	1	109.5
24	011000	0	1	1	0	0	0	114.3
25	011001	0	1	1	0	0	1	119.0
26	011010	0	1	1	0	1	0	123.8
27	011011	0	1	1	0	1	1	128.6
28	011100	0	1	1	1	0	0	133.3
29	011101	0	1	1	1	0	1	138.1
30	011110	0	1	1	1	1	0	142.9
31	011111	0	1	1	1	1	1	147.6
32	100000	1	0	0	0	0	0	152.4
33	100001	1	0	0	0	0	1	157.1
34	100010	1	0	0	0	1	0	161.9
35	100011	1	0	0	0	1	1	166.7
36	100100	1	0	0	1	0	0	171.4
37	100101	1	0	0	1	0	1	176.2
38	100110	1	0	0	1	1	0	181.0

Decimal	Binary	Address 8						Voltage (mV)
		D5	D4	D3	D2	D1	D0	
39	100111	1	0	0	1	1	1	185.7
40	101000	1	0	1	0	0	0	190.5
41	101001	1	0	1	0	0	1	195.2
42	101010	1	0	1	0	1	0	200.0
43	101011	1	0	1	0	1	1	204.8
44	101100	1	0	1	1	0	0	209.5
45	101101	1	0	1	1	0	1	214.3
46	101110	1	0	1	1	1	0	219.0
47	101111	1	0	1	1	1	1	223.8
48	110000	1	1	0	0	0	0	228.6
49	110001	1	1	0	0	0	1	233.3
50	110010	1	1	0	0	1	0	238.1
51	110011	1	1	0	0	1	1	242.9
52	110100	1	1	0	1	0	0	247.6
53	110101	1	1	0	1	0	1	252.4
54	110110	1	1	0	1	1	0	257.1
55	110111	1	1	0	1	1	1	261.9
56	111000	1	1	1	0	0	0	266.7
57	111001	1	1	1	0	0	1	271.4
58	111010	1	1	1	0	1	0	276.2
59	111011	1	1	1	0	1	1	281.0
60	111100	1	1	1	1	0	0	285.7
61	111101	1	1	1	1	0	1	290.5
62	111110	1	1	1	1	1	0	295.2
63	111111	1	1	1	1	1	1	300.0

Note: The voltage values are typical values.

Function Tables

The drive method in H-Bridge mode (stmx = 0) can be selected from Tables 1 and 2, via the modx bit.
(Channels E, F, G and H are always in H-Bridge mode regardless of the stmx setting.)

Table 1

modx = 0, stmx = 0

pxa	pxb	PWMx	OUTxA	OUTxB	Drive Mode
0	0	X	Z	Z	Stop
0	1	L	L	L	Short brake
0	1	H	L	H	Reverse
1	0	L	L	L	Short brake
1	0	H	H	L	Forward
1	1	X	L	L	Short brake

Table 2

modx = 1, stmx = 0

pxa	pxb	PWMx	OUTxA	OUTxB	Drive Mode
0	X	X	Z	Z	Stop
1	0	L	H	L	Forward
1	0	H	L	H	Reverse
1	1	X	L	L	Short brake

Function Table: STBY pin, UVLO and TSD circuitry, rstx bit (internal register)

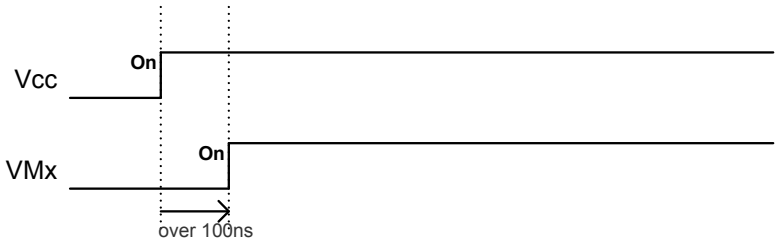
Function	STBY (Note 1)	UVLO	TSD	rstx
Internal Register	Cleared	Cleared	Not affected	Not affected
Driver	Turned off	Turned off	Turned off	Turned on (controlled by the ENn pin)

Note 1: STBY: L = Standby (power-save) mode; H = Normal operation mode

Note : All registers are cleared to zero.

Power supply sequence

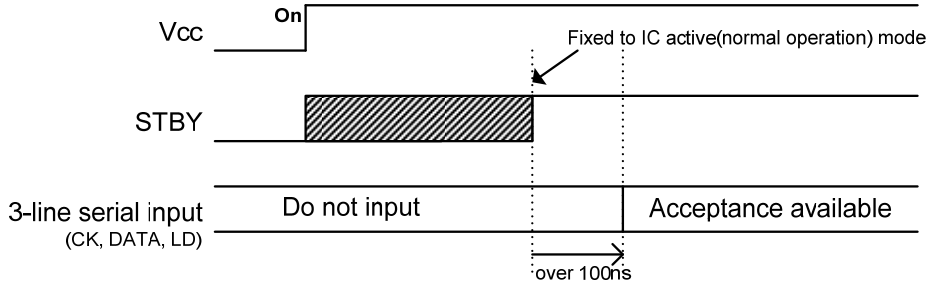
The power supply sequence for TB6613FTG is required for proper operation.
The power up sequence between Vcc and VMx(x=1,2,3,4) is shown below.



VMx(x=1,2,3,4) must be supplied after waiting over 100ns period from the Vcc is supplied.
If VMx are supplied without the waiting time or Vcc supply, IC could not start the normal operation and go into some error mode in a case.

Data communication initialization Sequence

A proper initialization sequence is also needed for a host to communicate with TB6613FTG.
The initialization sequence is shown below.



Input the Serial Signal (3-line) after waiting over 100ns period from the STBY fixed to "H", that means IC normal operation starts.
If without the 100ns waiting, IC could not accept the Serial Signal correctly in a case.

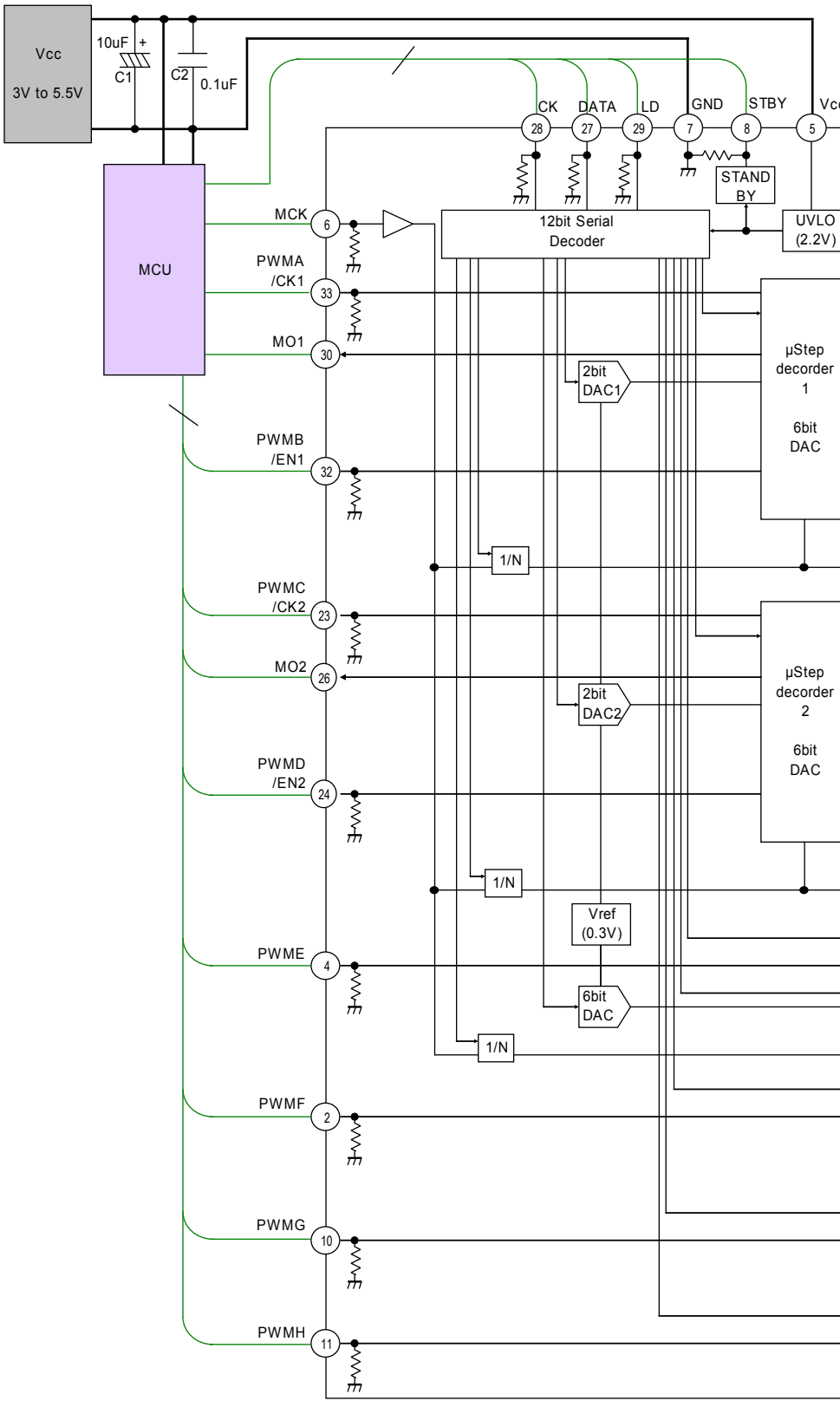
Electrical Characteristics (V_{CC} = 3.3 V, VM = 5 V, Ta = 25°C, unless otherwise specified.)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Supply current		I_{CC}	All 8 channels in Forward mode	—	2	4	mA
		$I_{CC\ (STB)}$	Standby mode (STBY = 0 V)	—	0.1	10	μA
		$I_{M\ (STB)}$		—	0	1	
Serial, STBY, PWM and CLK inputs	Input voltage	V_{INH}		V_{CC} × 0.7	—	V_{CC} + 0.2	V
		V_{INL}		−0.2	—	V_{CC} × 0.3	
	Input current	I_{INH}	V_{IH} = 3 V	5	15	25	μA
		I_{INL}	V_{IL} = 0 V	—	—	1	
Output saturation voltage (Channels A to H)		$V_{sat\ (U + L)}$	I_O = 0.2 A, V_{CC} = 5 V	—	0.3	0.4	V
			I_O = 0.6 A, V_{CC} = 5 V	—	0.9	1.2	
Output leakage current (Channels A to H)		$I_{L\ (U)}$	VM = 6 V	—	—	1	μA
		$I_{L\ (L)}$		—	—	1	
Output diode forward voltage		$V_{F\ (U)}$	I_F = 0.6 A (Design target only)	—	1	—	V
		$V_{F\ (L)}$		—	1	—	
Voltage comparator offset for constant-current control		Comp ofs	RF = 0.5 Ω, Vref = 0.1 V (including DAC)	−10	—	10	mV
6-bit DAC	Nonlinearity	LB	Channel E	−3	—	3	LSB
	Differential linearity error	DLB		−2	—	2	
Micro step reference level	6-bit mode	θ	See Appendix on next page.	—	—	—	%
	1-bit mode	Half step	(Design target only)	—	71	—	
V_{CC} under voltage lockout (UVLO)	UVLO trip threshold	UVLD	(Design target value)	—	2.0	—	V
	UVLO recovery	UVLC		—	2.2	—	
Thermal shutdown threshold		TSD	(Design target only)	—	170	—	°C
Thermal shutdown hysteresis		ΔTSD		—	20	—	
Delay between Vcc to VMx		Td1	(Design target only) Vcc, VM1,2,3,4	—	100	—	ns
Delay between STBY=H to Serial communication		Td2	(Design target only) STBY, CK, DATA, LD	—	100	—	

Appendix: Micro step Reference Level with 6-Bit Resolution (Design target only)

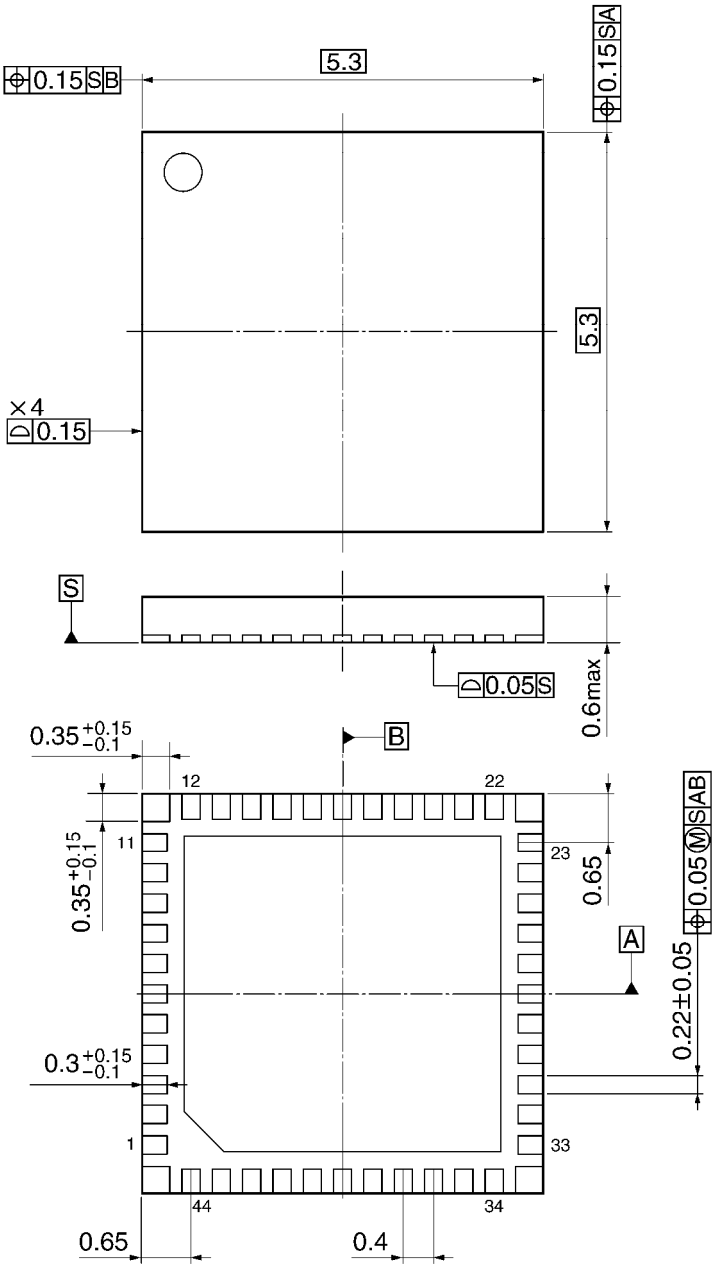
θ	Min	Typ.	Max	Unit	θ	Min	Typ.	Max	Unit
θ63	—	100	—		θ31	—	71	—	
θ62	—	100	—		θ30	—	69	—	
θ61	—	100	—		θ29	—	67	—	
θ60	—	100	—		θ28	—	65	—	
θ59	—	100	—		θ27	—	63	—	
θ58	—	99.5	—		θ26	—	61.25	—	
θ57	—	99	—		θ25	—	59.5	—	
θ56	—	98.5	—		θ24	—	57.75	—	
θ55	—	98	—		θ23	—	56	—	
θ54	—	97.5	—		θ22	—	53.75	—	
θ53	—	97	—		θ21	—	51.5	—	
θ52	—	96.5	—		θ20	—	49.25	—	
θ51	—	96	—		θ19	—	47	—	
θ50	—	95	—		θ18	—	44.75	—	
θ49	—	94	—		θ17	—	42.5	—	
θ48	—	93	—	%	θ16	—	40.25	—	%
θ47	—	92	—		θ15	—	38	—	
θ46	—	91	—		θ14	—	35.75	—	
θ45	—	90	—		θ13	—	33.5	—	
θ44	—	89	—		θ12	—	31.25	—	
θ43	—	88	—		θ11	—	29	—	
θ42	—	86.75	—		θ10	—	26.75	—	
θ41	—	85.5	—		θ9	—	24.5	—	
θ40	—	84.25	—		θ8	—	22.25	—	
θ39	—	83	—		θ7	—	20	—	
θ38	—	81.5	—		θ6	—	17.5	—	
θ37	—	80	—		θ5	—	15	—	
θ36	—	78.5	—		θ4	—	12.5	—	
θ35	—	77	—		θ3	—	10	—	
θ34	—	75.5	—		θ2	—	7.5	—	
θ33	—	74	—		θ1	—	5	—	
θ32	—	72.5	—		θ0	—	2.5	—	

Application Circuit Example



Package Dimensions

VQON44-P-0606-0.4 Unit: mm



Weight: 0.05 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

The following conditions apply to solderability:
About solderability, following conditions were confirmed
(1)Use of Sn-37Pb solder Bath
·solder bath temperature: 230°C·dipping time: 5 seconds·the number of times: once·use of R-type flux
(2)Use of Sn-3.0Ag-0.5Cu solder Bath
·solder bath temperature: 245°C·dipping time: 5 seconds·the number of times: once·use of R-type flux

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