

TOSHIBA Bi-CD Integrated Circuit Silicon Monolithic

# TB67S158NG

## 1. Summary/Features/Appearance

**Constant voltage control DMOS driver incorporating 2 function modes (full parallel input and serial input).**

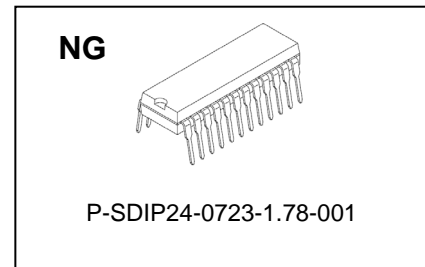
### Summary

The TB67S158 is a constant voltage control DMOS driver. It can operate maximum of two unipolar stepping motors (max).

MODE1: Full parallel input (similar to transistor array)

MODE2: Serial input

Output voltage of 80V and maximum current of 1.5A are realized by applying BiCD process. Motor can be driven by single power supply of VM with the internal regulator.



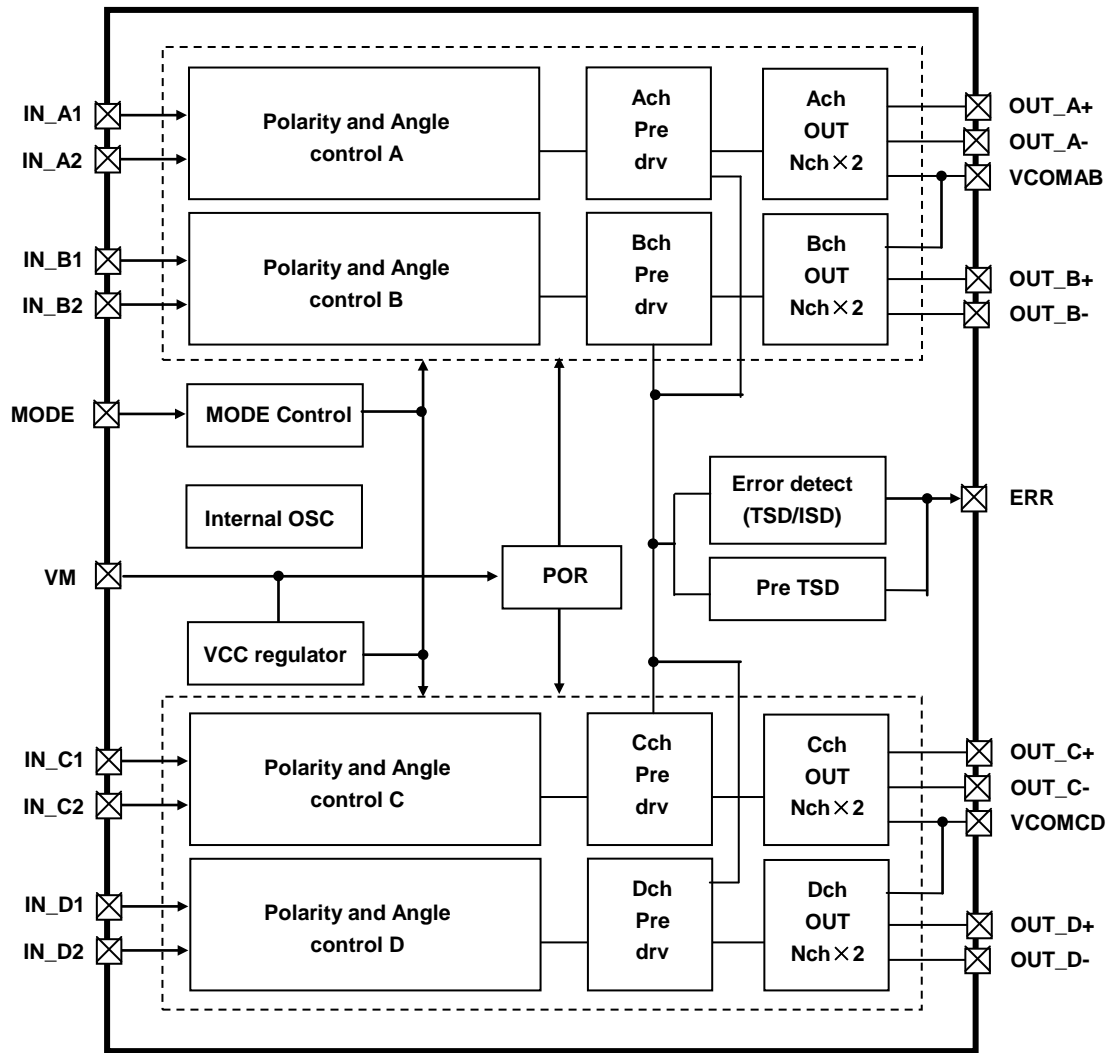
Weight: 1.4g(typ.)

### Features

- Capable of operating maximum of two 2-phase unipolar stepping motors by one chip.
- High voltage and current (as for specifications, please refer to the absolute maximum ratings and operation ranges).
- Low on resistance ( $R_{on}=0.5\Omega$  (typ.)) of output step is realized by BiCD process.
- Built-in VCC regulator for internal circuit control (capable of operating by only VM power supply)
- Capable of constant voltage driving (corresponding to 2-phase and 1-2-phase excitation drives)
- Built-in thermal shutdown circuit (TSD), over current detection (ISD), and power on reset of VM power supply.
- ALERT signal can be outputted to outside when thermal shutdown circuit (TSD) or over current detection (ISD) operates.

Note) Please be careful about the thermal conditions during use.

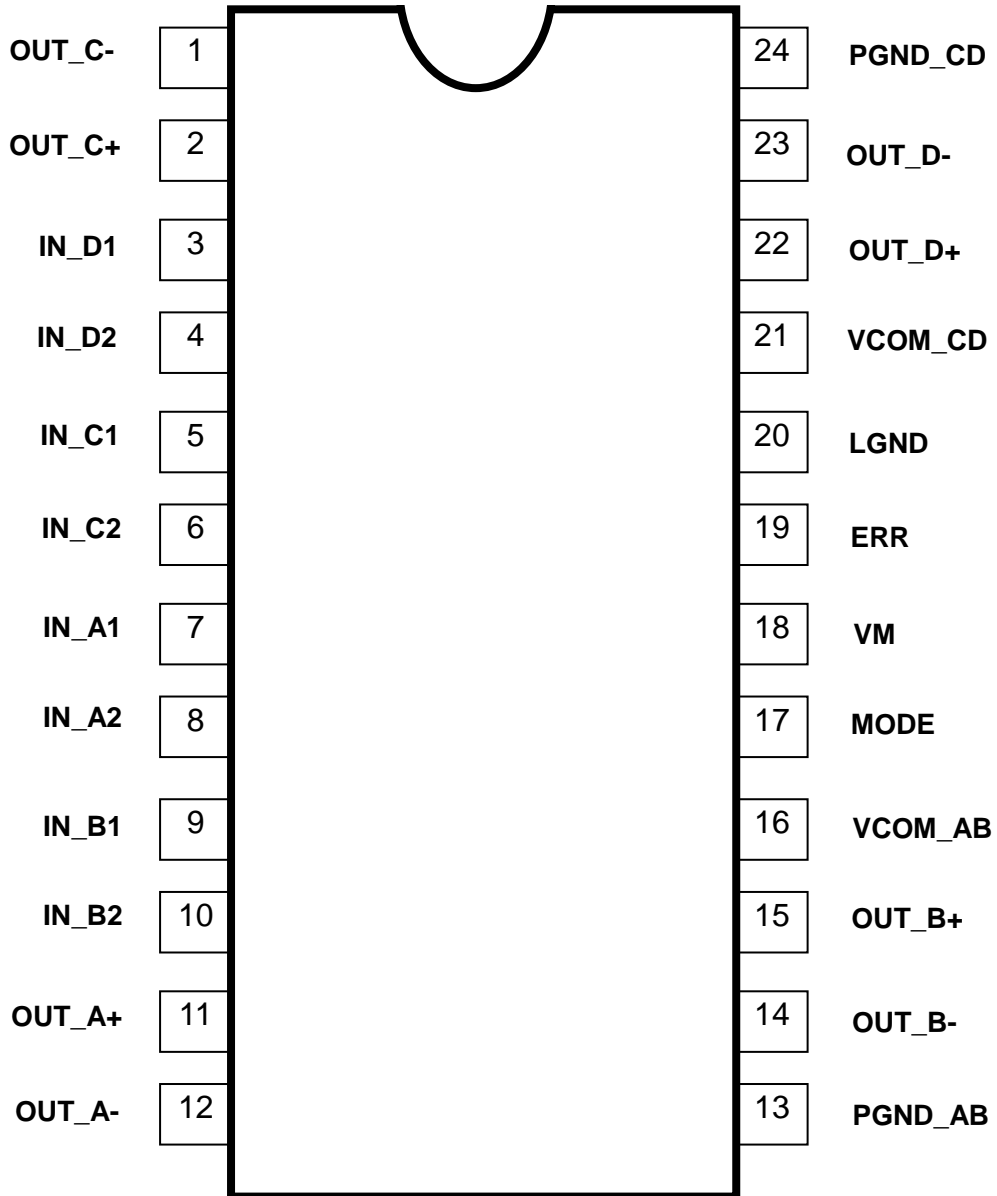
2. Block diagram: MODE1 (Full parallel mode)



3. Pin name/assignment

Pin assignment (TB67S158NG) MODE1 (Full parallel mode)

(Top View)



**3-1. Application Notes**

1) All the grounding wires of the device must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

2) When setting pin of each mode is controlled by SW, the voltage should be pull-up to the power supply which is the same voltage of the input signal or pull-down to the GND in order to avoid Hi-Z.

3) Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.

4) Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, OUT, GND, etc.) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

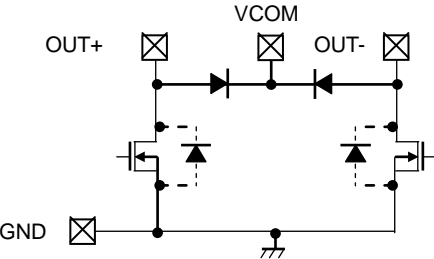
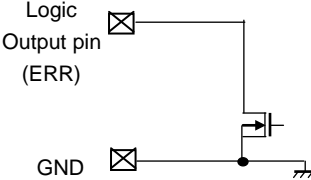
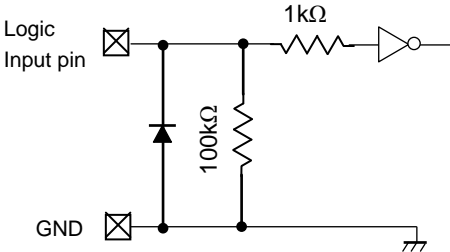
### 3-2. Pin assignment and description of TB67S158 (SDIP)

Pin No.	Full parallel (MODE=L)	Serial/Parallel (MODE=H)	Full parallel (MODE=L)	Serial/Parallel (MODE=H)
1	OUT_C-	OUT_C-	Output - pin for phase C	Output - pin for phase C
2	OUT_C+	OUT_C+	Output + pin for phase C	Output + pin for phase C
3	IN_D1	DATA	OUT_D+ ON pin	Input pin for serial data
4	IN_D2	CLK	OUT_D- ON pin	Input pin for serial clock
5	IN_C1	ALM	OUT_C+ ON pin	Output pin for thermal detection
6	IN_C2	NC	OUT_C- ON pin	NC
7	IN_A1	CLR	OUT_A+ ON pin	Clear pin for storage register
8	IN_A2	GATE	OUT_A- ON pin	Gate pin for register data
9	IN_B1	STBY	OUT_B+ ON pin	Standby setting pin
10	IN_B2	LATCH	OUT_B- ON pin	Input pin for serial latch
11	OUT_A+	OUT_A+	Output + pin for phase A	Output + pin for phase A
12	OUT_A-	OUT_A-	Output - pin for phase A	Output - pin for phase A
13	PGND_AB	PGND_AB	Power ground pin	Power ground pin
14	OUT_B-	OUT_B-	Output - pin for phase B	Output - pin for phase B
15	OUT_B+	OUT_B+	Output + pin for phase B	Output + pin for phase B
16	VCOM_AB	VCOM_AB	Common pin for phase A and B	Common pin for phase A and B
17	MODE	MODE	Switching pin for I/F	Switching pin for I/F
18	VM	VM	Pin for main power supply	Pin for main power supply
19	ERR	ERR	ERR output	ERR output
20	LGND	LGND	Logic_GND	Logic_GND
21	VCOM_CD	VCOM_CD	Common pin for phase C and D	Common pin for phase C and D
22	OUT_D+	OUT_D+	Output + pin for phase D	Output + pin for phase D
23	OUT_D-	OUT_D-	Output - pin for phase D	Output - pin for phase D
24	PGND_CD	PGND_CD	Power ground pin	Power ground pin

4. Functional/Operation description

4-1.Pin interface

TB67S158NG



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**Protection circuit**

Note: Logic pin is pull-down or pull-up by the resistor of about 100 k $\Omega$  in the IC.  
(Confirm the input equivalent circuit.)

**Functional description**ISD (over current detection)

ISD turns off the output of the motor when it detects over current (exceeding absolute maximum rating) in the output transistors. It is cleared when VM power supply is applied again or configured standby mode.

TSD (thermal shutdown circuit)

TSD turns off all outputs of the motor when it detects abnormal temperature ( $T_j = 160^\circ\text{C}$  (typ.)) of the IC. It is cleared when VM power supply is applied again or configured standby mode.

VMR (VM power supply monitor) circuit

When the voltage of VM is higher than the specified value, output is set high level. When it is lower than the specified value, output is set low (internal status).

POR (Power On Reset) circuit

When both VMR and VCCR are high: Logic transistors = active, Other states: Logic transistors = OFF

**5. MODE pin**

MODE	Function	
L	MODE1	Full parallel control I/F (Similar operation of transistor array)
H	MODE2	Serial/Parallel conversion control I/F

**6. Pin function of full parallel control I/F (Mode1)**

IN\_X pin can control each transistor directly like transistor array.

IN_A1	IN_A2	IN_B1	IN_B2	Function
L		-	-	OUT_A+ = OFF
H		-	-	OUT_A+ = ON
-	L	-	-	OUT_A- = OFF
-	H	-	-	OUT_A- = ON
-	-	L	-	OUT_B+ = OFF
-	-	H	-	OUT_B+ = ON
-	-	-	L	OUT_B- = OFF
-	-	-	H	OUT_B- = ON

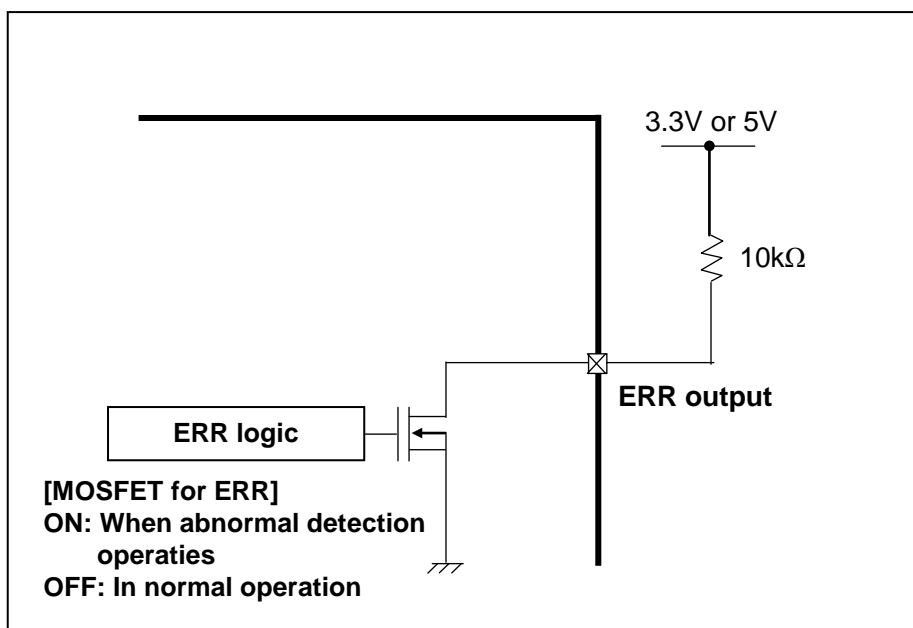
IN_C1	IN_C2	IN_D1	IN_D2	Function
L		-	-	OUT_C+ = OFF
H		-	-	OUT_C+ = ON
-	L	-	-	OUT_C- = OFF
-	H	-	-	OUT_C- = ON
-	-	L	-	OUT_D+ = OFF
-	-	H	-	OUT_D+ = ON
-	-	-	L	OUT_D- = OFF
-	-	-	H	OUT_D- = ON



**6-1. ERR (output function of abnormal detection)**

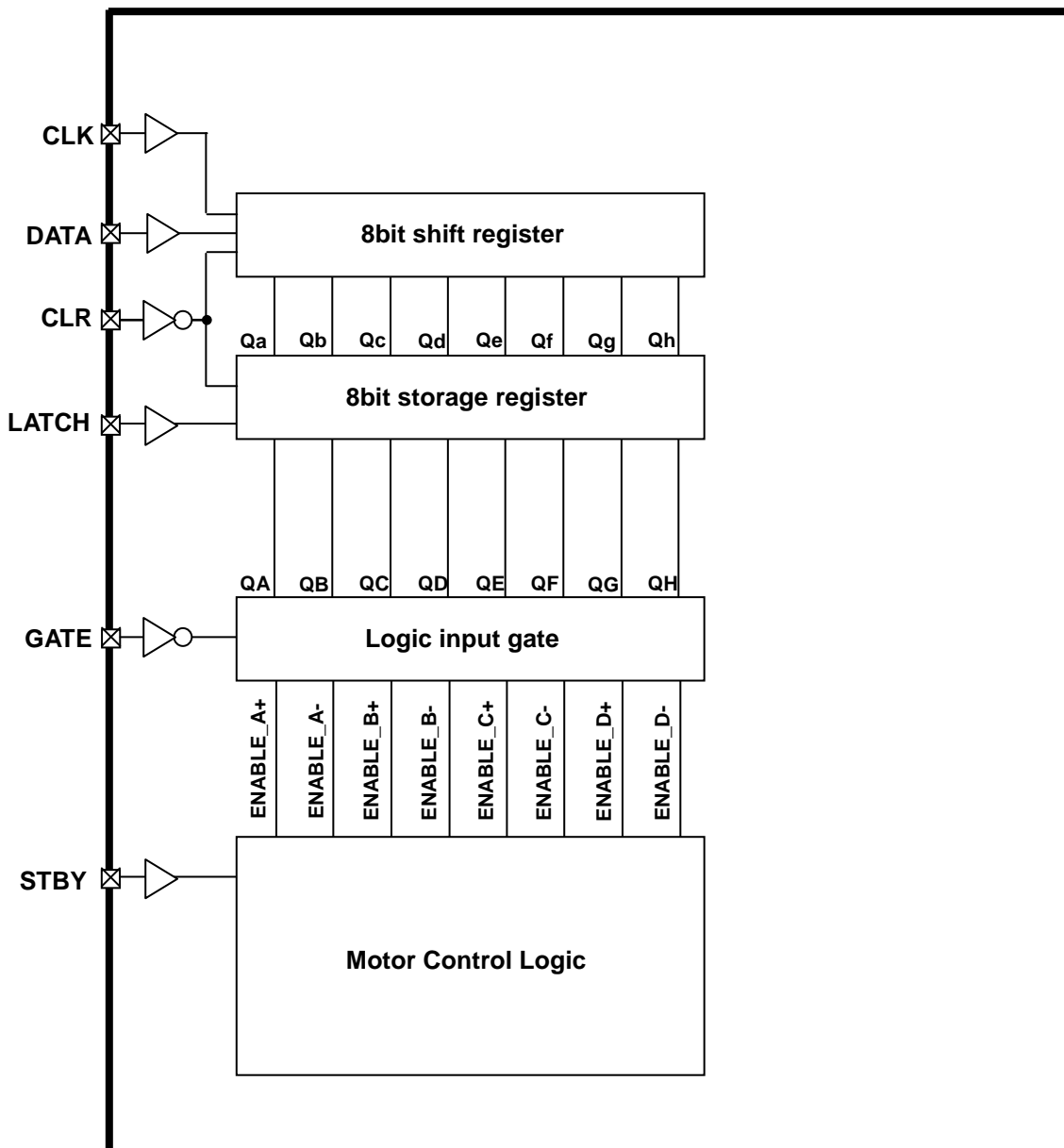
ERR output	Function
H	Normal operation
L	Abnormal detection (TSD or ISD)

ERR pin is a logic output pin of open drain type. It outputs high level (pull-up voltage level) in the normal operation. It outputs low (GND level) when TSD or ISD operates. When TSD or ISD detection is cleared, high level is outputted.



**7. Pin function of serial/parallel conversion control I/F (Mode2)**

**7-1. Input interface (8bit shift register + 8bit storage register)**



\* Initial value for each logic pin when signal is not inputted

Pin name	Initial value
CLK	Low
DATA	Low
CLR	Low
LATCH	Low
GATE	High
STBY	Low

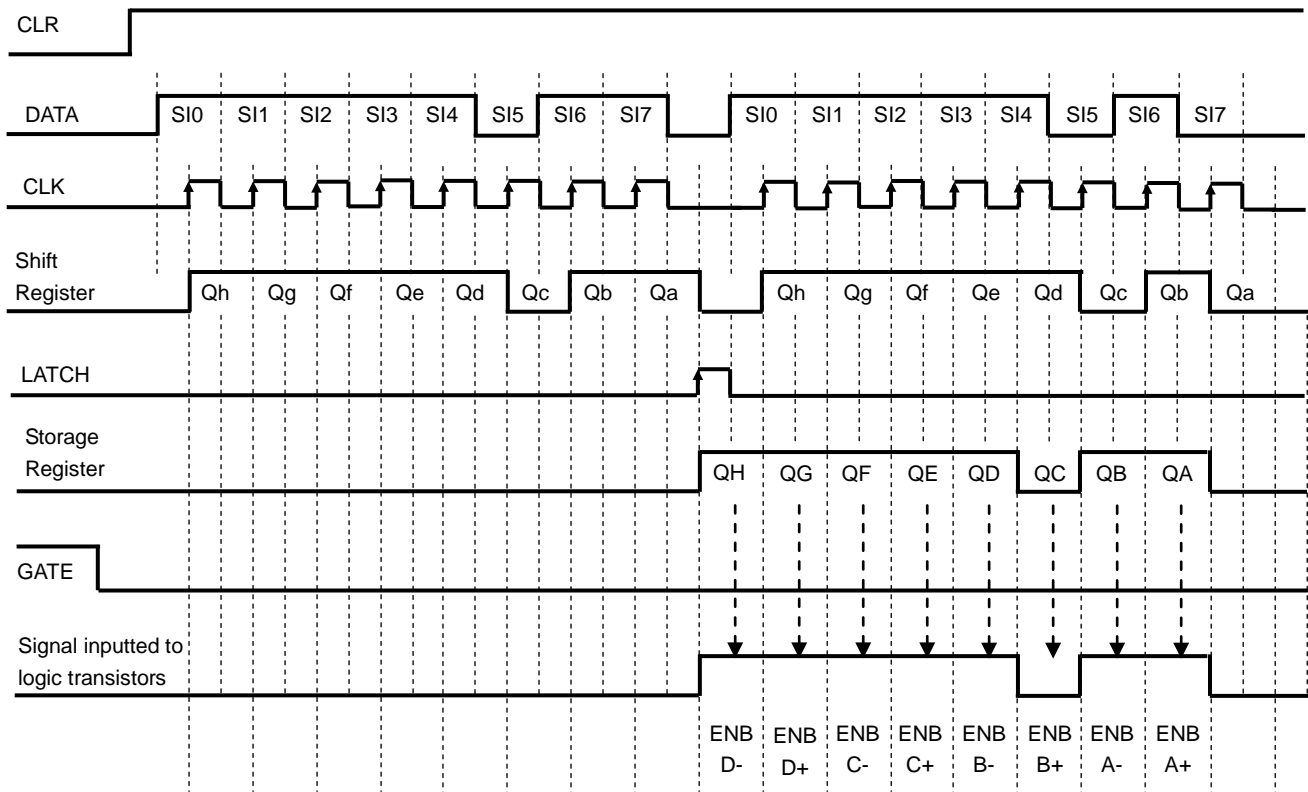
Initial state for each logic pin when signal is not inputted is as follows.

LATCH: Low=sift register/storage register: initial state

GATE: High=ENABLE\_X+,ENABLE\_X-=Disable \* "X" of ENABLE\_X stands for A, B, C, and D.

STBY=Low: standby state

## Timing chart of input signal (normal input)



### \*Truth table

Input					Function
CLK	DATA	CLR	LATCH	GATE	
X	X	X	X	L	Data of ENABLE_X+ and ENABLE_X-: Not applicable
X	X	X	X	H	Data of ENABLE_X+ and ENABLE_X-: Applicable
X	X	L	X	X	Data stored in the storage register is cleared
L	↑	H	X	X	The first step of the shift register: 'L', Others: data of each prior step is stored.
H	↑	H	X	X	The first step of the shift register: 'H', Others: data of each prior step is stored.
X	↓	H	X	X	Shift register keeps prior state.
X	X	H	↑	X	Data of shift register is stored in the storage register.
X	X	H	↓	X	Storage register keeps prior state.

Truth table: X=Don't care

\* "X" of ENABLE\_X stands for A, B, C, and D.

\* Note: To operate logic output normally, SCK must be configured low in data transfer and complete.

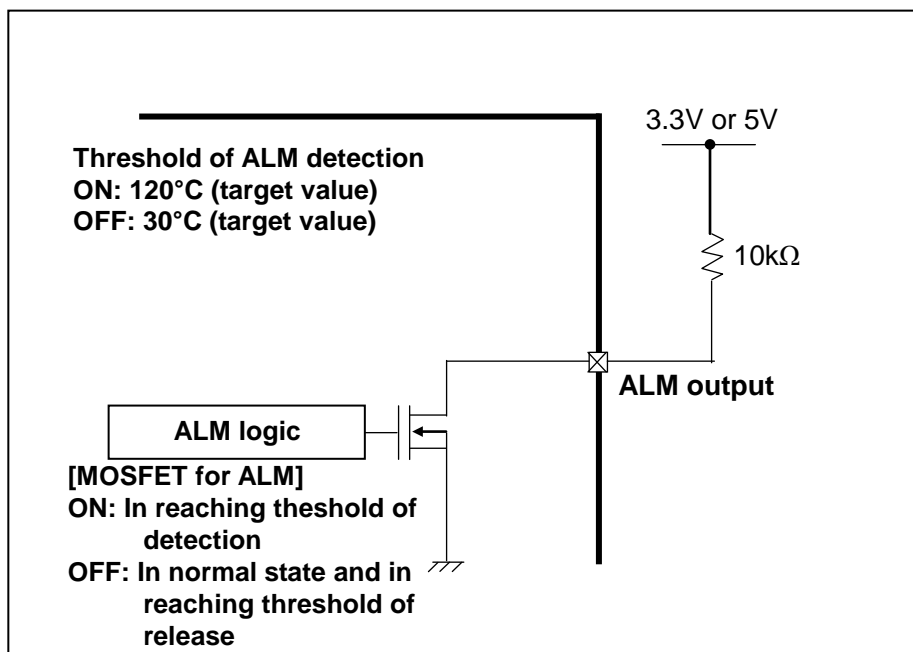
### • Description of logic signal

Signal name	H	L	Notes
ENABLE_X	Output ON	Output OFF	When ENABLE_x is set low, output of corresponded channel is turned off (Hi-Z).
STBY	Motor operation: enable	Turn off all functions of the IC	When STBY is set L, motor output is turned off. (Motor cannot operate).

**7-2. Function of ALM (output function of thermal shutdown alarm)** (Enable in serial/parallel conversion control I/F)

ALM output	Function
H	Normal operation
L	Thermal shutdown alarm function (Thermal_Alarm)

ALM pin is a logic output pin of open drain type. It outputs high (pull-up voltage level) in normal state. When the temperature of the IC reaches specified threshold (Thermal\_Alarm), low level (GND level) is outputted. Function of ALM is cleared automatically when the temperature of the IC falls 20°C (target value) lower than the threshold of Thermal Alarm.



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**8. Absolute maximum ratings (Ta=25°C)**

Characteristics	Symbol	Rating	Unit	
Motor power supply VM	VM(max)	80	V	
Motor output voltage	VOOUT(max)	80	V	
Motor output current	IOOUT(max)	1.5	A	
Internal logic power supply	VCC(max)	6.0	V	
Logic input voltage	VIN(H)(max)	6.0	V	
	VIN(L)(min)	-0.4	V	
Open drain output pin (ERR,ALM) voltage range	Vod(max)	6.0	V	
Open drain output pin(ERR,ALM) inflow current range	Iod(max)	20	mA	
Power dissipation (Note)	SDIP24	PD	1.78	W
Operating temperature	Topr	-20 to 85	°C	
Storage temperature	Tstg	-55 to 150	°C	
Junction temperature	Tj(max)	150	°C	

Note: Monolithic. When the temperature (Ta) exceeds 25°C, derate the value by 14.2mW/°C.

Ta: Ambient temperature of the IC

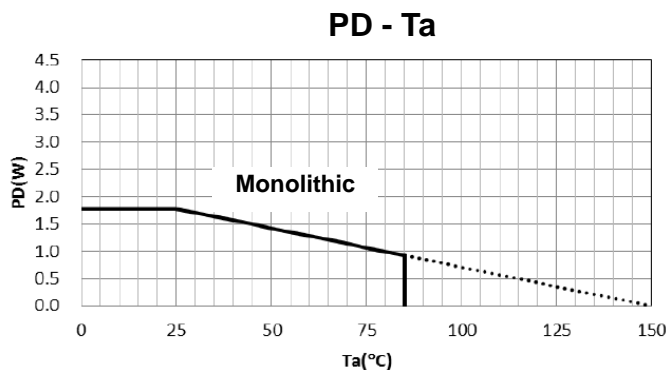
Topr: Ambient temperature of the IC under operation.

Tj: Chip temperature of the IC under operation. The maximum of Tj is limited by the temperature of TSD (thermal shutdown circuit). It is recommended to design the IC by considering the maximum of the usage current of 120°C.

**Absolute maximum ratings**

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied. All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

■(For reference) Relation of power dissipation and ambient temperature



## 9. Operation ranges (Ta=-20 to 85°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Motor power supply VM	VM		10	24	60	V
Motor output voltage	VOUT	Connecting to zener (24V)	10	48	60	V
Motor output current	IOUT	Ta=25°C per phase	-	1.0	1.5	A
Logic input voltage	VIN(H)	Logic input high level	2.0	-	5.5	V
	VIN(L)	Logic input low level	0	-	0.8	V
Open drain pin voltage range	Vod(range)	ERR,ALM pin	3.0	-	5.5	V
Open drain pin inflow current range	Iod(range)	ERR,ALM pin	-	-	10	mA

(Note): Please use the device with extra margin regarding the absolute maximum ratings.

## 10. Electrical characteristics

### 10-1. DC electrical specifications 1 (Ta=25°C, VM=24V, unless specified otherwise)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage		VIH	Logic input voltage High level	2.0	-	5.5	V
		VIL	Logic input voltage Low level	GND	-	0.8	V
Input hysteresis		VIN(HYS)	(Note 1)	100	-	300	mV
Logic input current	High	IIN(H)	Logic input voltage High level (VIN=3.3V)	-	33	55	μA
	Low	IIN(L)	Logic input voltage Low level	-	-	1	μA
IM consumption current		IM1	Output pins: open, VIN=VIL, Standby mode	-	0.7	1.0	mA
		IM2	Output pins: open, Normal operation Motor output steps: no operation	-	1.3	2.0	mA
Open drain logic output pin voltage		VOL	IOL=5mA (output pins: Low)	-	-	0.5	V
Regenerative diode Forward voltage		VFN	VM=24V, IOU=1.5A, Tj=25°C	-	1.2	-	V
Output transistor Drain-Source On-resistance		RON(D-S)	IOU=1.5A Tj=25°C	-	0.5	0.7	Ω

(Note 1): VIN (H) is defined as the VIN voltage that causes the outputs to change when the voltage of the test pin is gradually raised from 0 V. VIN (L) is defined as the VIN voltage that causes the outputs to change when the voltage of the pin is then gradually lowered. The difference between VIN (L) and VIN (H) is defined as the input hysteresis.

## 10-2. DC electrical specifications 2 (Ta=25°C, VM=24V, unless specified otherwise)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Temperature threshold of thermal shutdown detection (TSD) (Note 1)	TjTSD	-	140	160	170	°C
VM recovery voltage	VMR	-	7.0	8.0	9.0	V
Over current detection (ISD) threshold (Note 2)	ISD	-	1.6	3.0	4.0	A

### Note1) About Thermal shutdown (TSD)

When the junction temperature of the IC reaches the TSD threshold, the TSD circuit operates and turns off the output transistors. Noise rejection blanking time is provided to avoid misdetection by switching. (As for details, refer to the section of "Blanking time of TSD".) The IC drives in the standby mode while TSD operates. Once the TSD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power supply, or setting the device to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore it is not recommended to be used aggressively.

### Note2) About Over-current detection (ISD)

When the output current reaches the threshold, the ISD circuit operates and turns off the output transistors. Noise rejection blanking time is provided to avoid misdetection by switching. (As for details, refer to the section of "Blanking time of ISD".) While ISD operates, the IC drives in the standby mode. After ISD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power supply, or setting the device to standby mode.

## Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF. If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

## Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuits; they do not necessarily guarantee the complete IC safety. If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit. The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

## IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.



**10-3. AC electrical specifications (Ta=25°C, VM=24V, unless specified otherwise)**

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Logic input frequency	fLogic	-	1.0	-	150	kHz
Minimum clock pulse width	twp	-	700	-	-	ns
	tw <sub>n</sub>	-	700	-	-	ns
Output transistor Switching characteristics	t <sub>r</sub>	-	0.2	0.25	0.3	μs
	t <sub>f</sub>	-	0.2-	0.25	0.3	μs
	t <sub>pLH</sub>	Between "Logic" and "OUT"	-	1.2	-	μs
	t <sub>pHL</sub>		-	1.2	-	μs
Over current detection (ISD) masking time	tISD(Mask)	Internal oscillation: 4.0MHz	-	2.0	-	μs
Over current detection (ISD) operating time	tISD		2.0	-	4.0	
Thermal shutdown detection (TSD) masking time	tTSD(Mask)	Internal oscillation: 4.0MHz	-	8.0	-	μs

**Timing chart: Switching characteristics of output transistors**

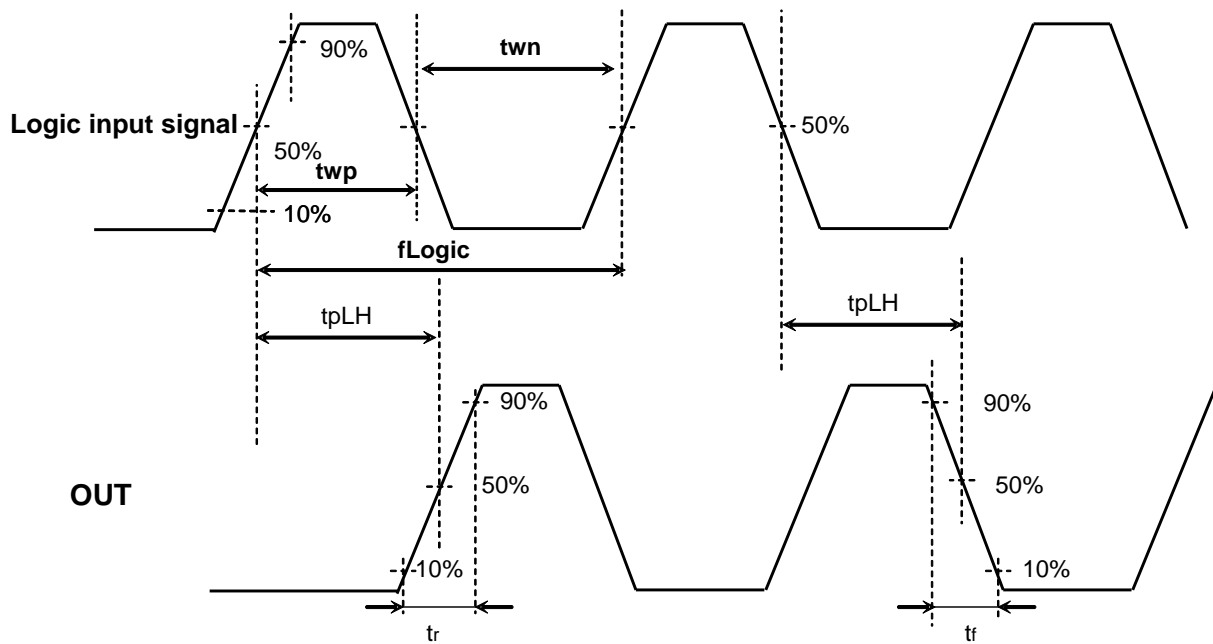


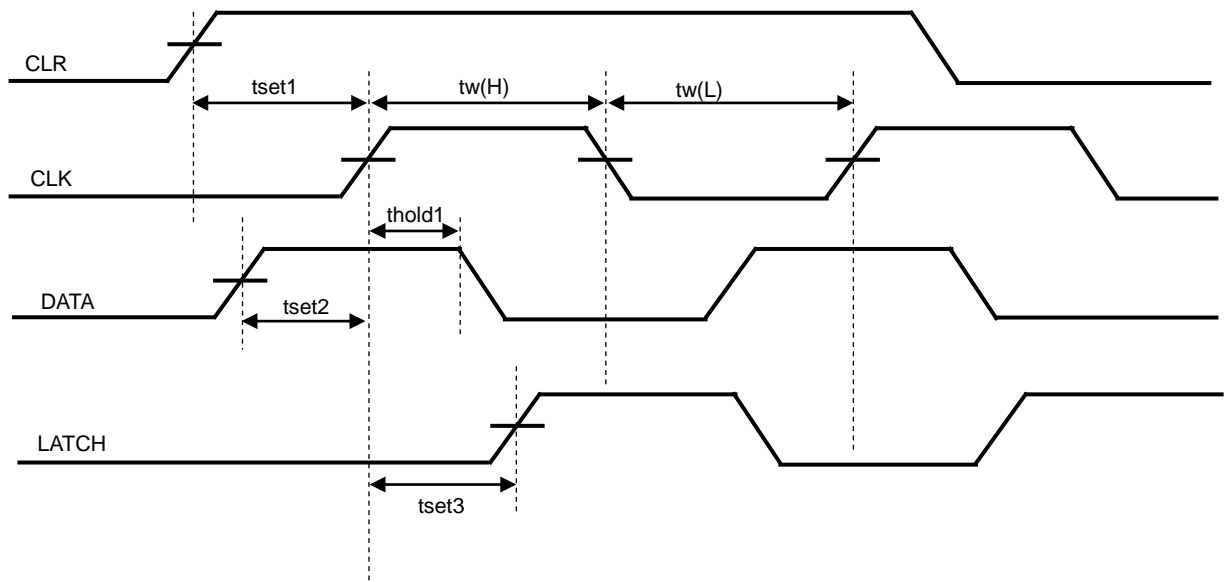
Figure 1 Logic input and switching characteristics of output transistors

Timing charts may be simplified for explanatory purposes.

**10-4. AC electrical specifications [Serial/Parallel conversion] (Ta = 25°C, VM = 24 V)**

Characteristics	Symbol	Electrical characteristics	Test condition	Min	Typ.	Max	Unit
Minimum pulse width (SCK, RCK, and SI input signals)	tw(H)	AC	-	250	-	-	ns
	tw(L)		-	250	-	-	ns
Minimum setting up time	tset1		CLR→CLK	50	-	-	ns
	tset2		DATA→CLK	50	-	-	ns
	tset3		CLK→LATCH	50	-	-	ns
Cycle time of minimum clock signal (SCK and RCK)	tcyc		-	500	-	-	ns
Minimum hold time	thold1		-	-	-	-	ns
			CLK→DATA	50	-	-	ns

**Timing chart: Switching characteristics of output transistors**



Timing charts may be simplified for explanatory purposes.

**Power consumption of the IC**

Power consumption of the IC is separated into two; consumed by output transistors and by logic transistors.

**1. Power consumption of power transistors (when  $R_{ON} (D-S) = 0.5 \Omega$ )**

Electrical power of output block is consumed by transistors.

Electrical power of the transistors in one motor drive is indicated as follows;

$$P (out) = 2 (\text{number of channels}) \times I_{out} (A)^2 \times R_{on} (\Omega) \dots\dots\dots (1)$$

When  $R_{on} = 0.5 \Omega$  and  $I_{out} = 1.0 A$ ,

$$P (out) = 2 (ch) \times 1.0(A)^2 \times 0.5 (\Omega) \dots\dots\dots (2)$$

$$= 1.0(W)$$

**2. Power consumption of logic and IM system**

It is calculated by separating the states into driving mode and turning off mode.

$$I (IM2) = 2 \text{ mA (max)}$$

Power consumption can be estimated from below formula.

$$P (IM) = 24 (V) \times 0.002 (A) \dots\dots\dots (3)$$

$$= 0.048 (W)$$

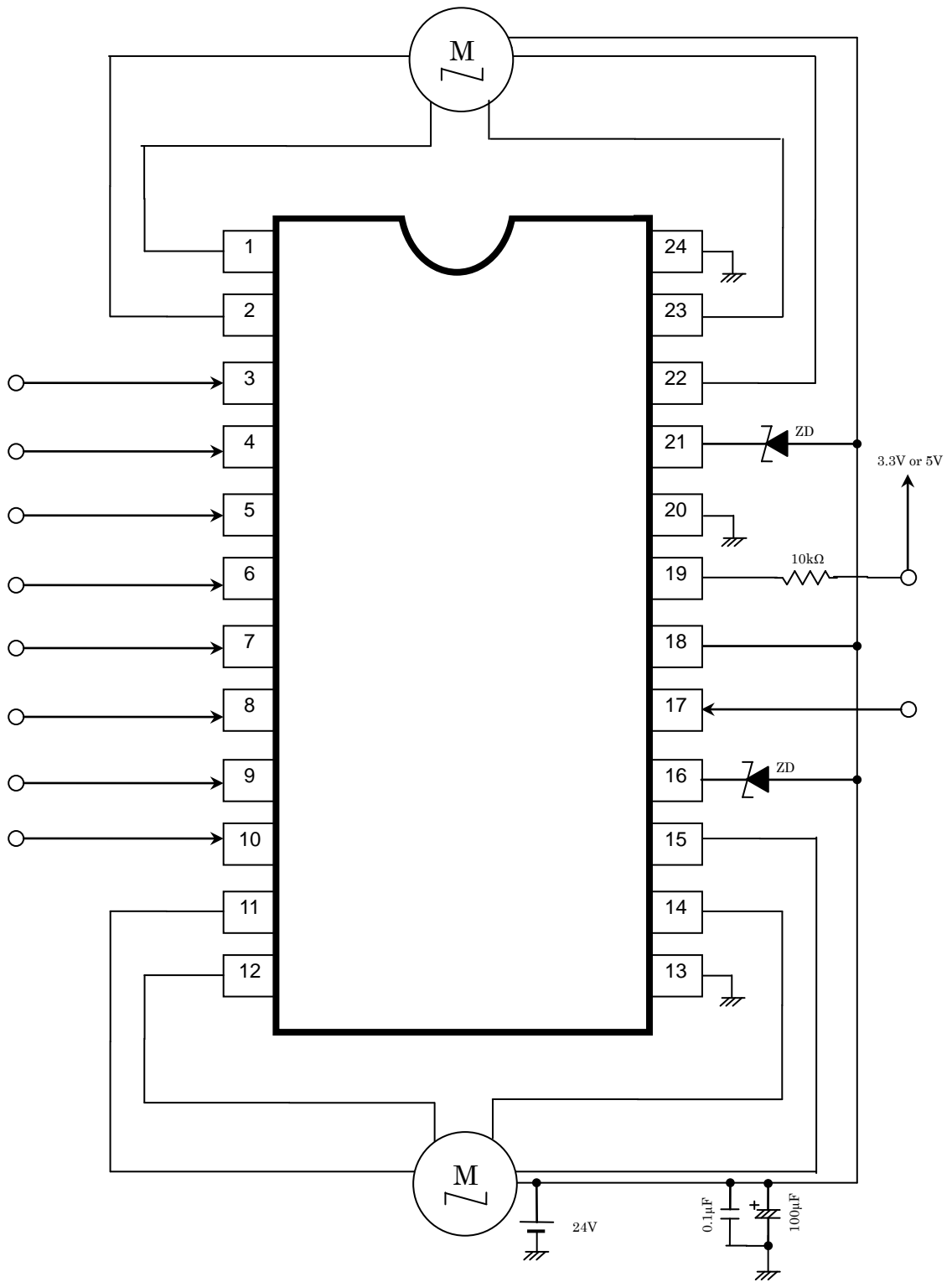
**3. Power consumption**

Whole power consumption (P) is calculated from the result of the calculations of (2) and (3).

$$P = P (out) + P (IM) = 1.048 (W)$$

As for thermal design for the board, take enough margin to design after evaluating the IC with the actual board.

**11. Application circuit**

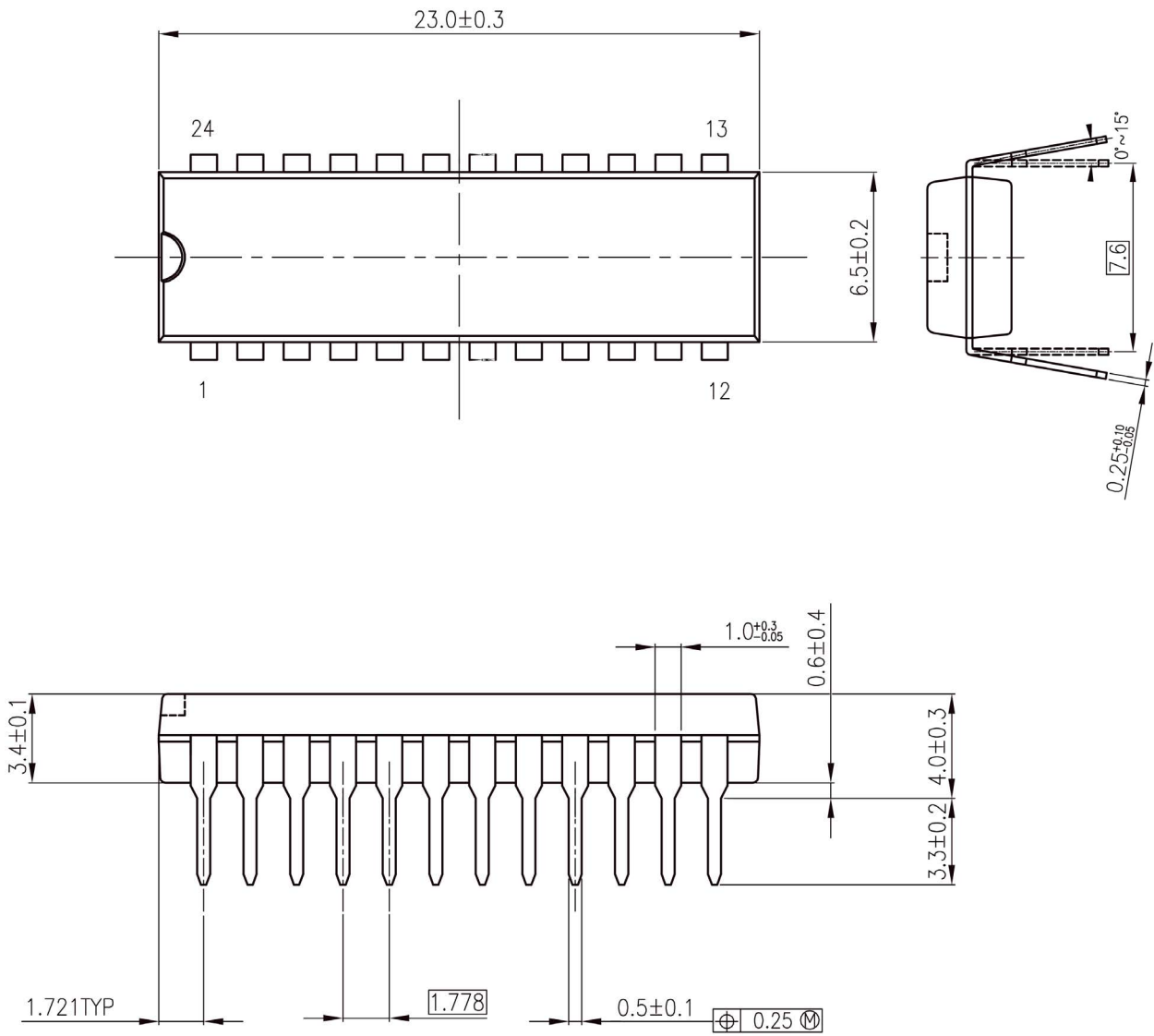


The application circuits shown in this document are provided for reference purposes only. It does not guarantee the mass production design.

**12. Package dimensions**

P-SDIP24-0723-1.78-001

Unit: mm



Weight: 1.4 g (typ.)

## Notes on Contents

### Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### Timing Charts

Timing charts may be simplified for explanatory purposes.

### Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

### Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## IC Usage Considerations

### Notes on handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.  
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.  
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.  
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

## **Points to remember on handling of ICs**

### **Overcurrent detection Circuit**

Overcurrent detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the overcurrent detection circuits operate against the overcurrent, clear the overcurrent status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the overcurrent detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

### **Thermal Shutdown Circuit**

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

### **Heat Radiation Design**

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature ( $T_j$ ) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

### **Back-EMF**

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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