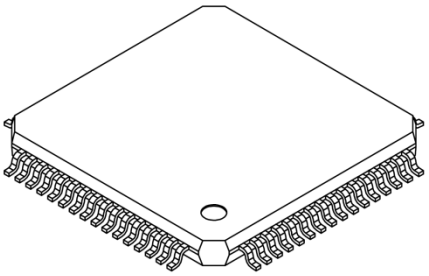
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB9081FG

Automotive GATE-driver for Brushless motor

TB9081FG is Pre-driver IC automotive for brushless motor.
Fail-safe relay pre-drivers are also built in in addition to 3-phase pre-drivers.
The charge pump, the motor current detection circuit, the oscillator, and the SPI communication circuit are built in.
The miscellaneous abnormal detections are carried and the operation after failure detection conditions and failure detections can be set up. About each setup, these can set up through a SPI communication.
Also, it has built-in ABIST / LBIST functions for diagnosing the normal operation of the miscellaneous abnormal detection function.



LQFP64-P-1010-0.50E

Weight: 0.35 g (typ.)

Features

- 3-phase pre-drivers : PWM control to 20kHz
- Build-in fail-safe relay pre-drivers
- Build-in Charge Pump
- High response Current Detection circuit
- Miscellaneous-abnormal-detection circuits
  (Under voltage (VB, VCC) / Over voltage (VCC) / Over temp. / FET short-circuit detection)
- Build-in ABIST/LBIST functions
- Operating voltage range : VB=4.5 to 28V, VCC=3.0 to 5.5V
- Operational temperature range : -40 to 125°C
- Package : LQFP-64pin (0.5mm pitch)
- AEC-Q100 Qualified
- TM-SIL™
  - Developed according to ISO 26262 ASIL-D
  - Safety Manual and Safety Analysis Report
  - Functional redundancy and built-in ABIST and LBIST
  - SPI interface with CRC check

The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

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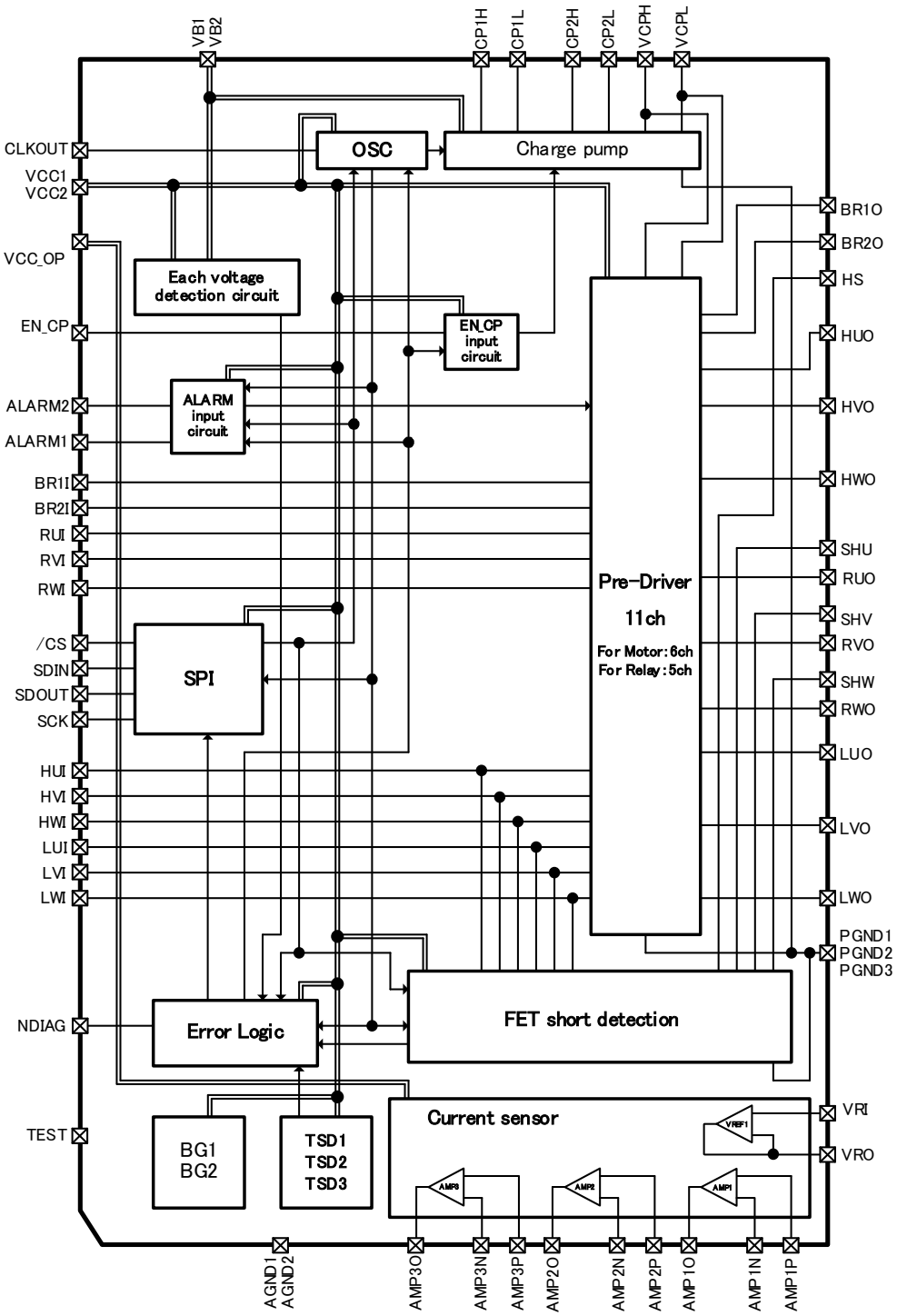
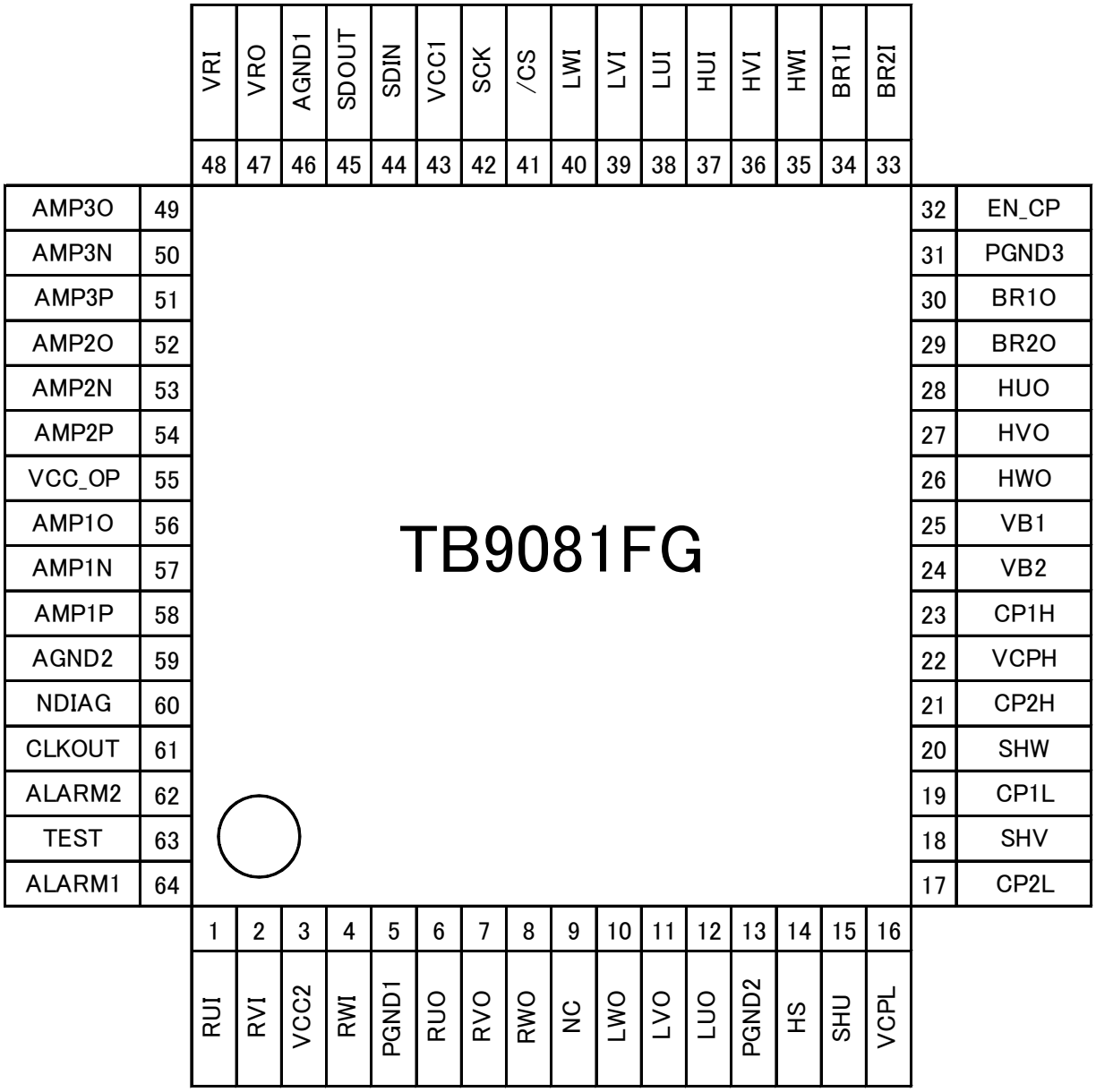
Internal block diagram



Notes 1: Some of the functional blocks, circuit, or constants in the block diagram may be omitted or simplified for explanatory purpose. (including individual block diagram)

Package pin layout (top view)



Pin description

Pin No.	Symbol	Input/output	Definition	Pull-Up/Down		Notes
1	RUI	IN	U-Phase Motor Relay Input	Pull-Down	50kΩ	-
2	RVI	IN	V-Phase Motor Relay Input	Pull-Down	50kΩ	-
3	VCC2	Power supply	Power supply 2 (3.3V or 5V)	-	-	-
4	RWI	IN	W-Phase Motor Relay Input	Pull-Down	50kΩ	-
5	PGND1	GND	Power GND1	-	-	-
6	RUO	OUT	U-Phase Motor Relay Output	-	-	push-pull
7	RVO	OUT	V-Phase Motor Relay Output	-	-	push-pull
8	RWO	OUT	W-Phase Motor Relay Output	-	-	push-pull
9	NC	-	-	-	-	-
10	LWO	OUT	Pre-Driver Output LW	-	-	push-pull
11	LVO	OUT	Pre-Driver Output LV	-	-	push-pull
12	LUO	OUT	Pre-Driver Output LU	-	-	push-pull
13	PGND2	GND	Power GND2	-	-	-
14	HS	IN	High-side Drain Input	-	-	-
15	SHU	IN	Motor Connect PIN U-phase	-	-	-
16	VCPL	Power supply	Charge-pump voltage (for low sides)	-	-	-
17	CP2L	OUT	2nd Charge Pump Drive Output	-	-	push-pull
18	SHV	IN	Motor Connect PIN V-phase	-	-	-
19	CP1L	OUT	1st Charge Pump Drive Output	-	-	push-pull
20	SHW	IN	Motor Connect PIN W-phase	-	-	-
21	CP2H	IN/OUT	2nd Charge Pump Output	-	-	-
22	VCPH	Power supply	Charge-pump voltage (for high sides)	-	-	-
23	CP1H	IN/OUT	1st Charge Pump Output	-	-	-
24	VB2	Power supply	Power Supply2 (Battery 12V)	-	-	-
25	VB1	Power supply	Power Supply1 (Battery 12V)	-	-	-
26	HWO	OUT	Pre-Driver Output HW	-	-	push-pull
27	HVO	OUT	Pre-Driver Output HV	-	-	push-pull
28	HUO	OUT	Pre-Driver Output HU	-	-	push-pull
29	BR2O	OUT	BR2 Power supply relay Output	-	-	push-pull
30	BR1O	OUT	BR1 Power supply relay Output	-	-	push-pull
31	PGND3	GND	Power GND 3	-	-	-
32	EN_CP	IN	Charge-pump enable signal	Pull-Down	50kΩ	-
33	BR2I	IN	BR2 Power supply relay Input	Pull-Down	50kΩ	-
34	BR1I	IN	BR1 Power supply relay Input	Pull-Down	50kΩ	-
35	HWI	IN	Pre-Driver Input HW	Pull-Down	50kΩ	-
36	HVI	IN	Pre-Driver Input HV	Pull-Down	50kΩ	-
37	HUI	IN	Pre-Driver Input HU	Pull-Down	50kΩ	-
38	LUI	IN	Pre-Driver Input LU	Pull-Down	50kΩ	-
39	LVI	IN	Pre-Driver Input LV	Pull-Down	50kΩ	-
40	LWI	IN	Pre-Driver Input LW	Pull-Down	50kΩ	-
41	/CS	IN	SPI chip select	Pull-Up	50kΩ	-
42	SCK	IN	SPI clock input	Pull-Down	50kΩ	-
43	VCC1	Power supply	Power supply 1 (3.3V or 5V)	-	-	-
44	SDIN	IN	SPI input	Pull-Down	50kΩ	-
45	SDOUT	OUT	SPI Output	-	-	push-pull
46	AGND1	GND	The GND 1 for analog circuits	-	-	-
47	VRO	OUT	Reference voltage amplifier Output	-	-	-
48	VRI	IN	Reference voltage amplifier input	-	-	-
49	AMP3O	OUT	Current-detection amplifier Output 3	-	-	push-pull
50	AMP3N	IN	Current-detection amplifier input 3 (-)	-	-	-
51	AMP3P	IN	Current-detection amplifier input 3 (+)	-	-	-
52	AMP2O	OUT	Current-detection amplifier Output 2	-	-	push-pull
53	AMP2N	IN	Current-detection amplifier input 2 (-)	-	-	-
54	AMP2P	IN	Current-detection amplifier input 2 (+)	-	-	-
55	VCC_OP	Power supply	The power supply for Current-detection amplifier (5V/3.3V)	-	-	-
56	AMP1O	OUT	Current-detection amplifier Output 1	-	-	push-pull
57	AMP1N	IN	Current-detection amplifier input 1 (-)	-	-	-
58	AMP1P	IN	Current-detection amplifier input 1 (+)	-	-	-
59	AGND2	GND	The ground 2 for analog circuits	-	-	-
60	NDIAG	OUT	Error Output Pin	-	-	push-pull
61	CLKOUT	OUT	Clock output	-	-	push-pull
62	ALARM2	IN	Pre-driver enable 2	Pull-Down	50kΩ	-
63	TEST	IN	Test terminal	Pull-Down	50kΩ	-
64	ALARM1	IN	Pre-driver enable 1	Pull-Down	50kΩ	-

●Description of an internal signal name

Internal signal name	Description	State	
		H	L
abst_pass	Normal signal of ABIST	ABIST normal	ABIST abnormal
abst_end	End signal of ABIST	ABIST end	ABIST unfinished
gate_en_u	Pre-driver output enabling signal (U phase)	Enable	Disable
gate_en_v	Pre-driver output enabling signal (V phase)	Enable	Disable
gate_en_w	Pre-driver output enabling signal (W phase)	Enable	Disable
gate_en_r	Pre-driver output enabling signal (relay)	Enable	Disable
gate_off_u	Error output signal (Pre-driver output enabling, U phase)	Enable	Disable
gate_off_v	Error output signal (Pre-driver output enabling, V phase)	Enable	Disable
gate_off_w	Error output signal (Pre-driver output enabling, W phase)	Enable	Disable
gate_off_r	Error output signal (Pre-driver output enabling, relay)	Enable	Disable
cp_en	Enabling signal for charge pump circuit	Enable	Disable
cp_off	Error output signal (charge pump circuit enabling)	Enable	Disable
vbl1	VB1/VB2 under voltage detection signal 1	Detection	Release
vbl2	VB1/VB2 under voltage detection signal 2	Detection	Release
vcl1	VCC1/VCC2 under voltage detection signal 1	Detection	Release
vcl2	VCC1/VCC2 under voltage detection signal 2	Detection	Release
por_x	Internal reset signal	Reset release	Reset
vch	VCC1/VCC2 over voltage detection signal	Detection	Release
vphh	VCPH clamp voltage detection signal	Detection	Release
tsd1det	Over temperature detection signal1	Detection	Release
tsd2det	Over temperature detection signal2	Detection	Release
tsd3det	Over temperature detection signal3	Detection	Release
shuho	Short-circuit detection signal (U phase low side)	Detection	Release
shvho	Short-circuit detection signal (V phase low side)	Detection	Release
shwho	Short-circuit detection signal (W phase low side)	Detection	Release
shulo	Short-circuit detection signal (U phase high side)	Detection	Release
shvlo	Short-circuit detection signal (V phase high side)	Detection	Release
shwlo	Short-circuit detection signal (W phase high side)	Detection	Release

<Usage power supply/GND list>

Symbol	Pin name	Function/Application
Vb	VB1,VB2	Battery power supply
Vcc	VCC1,VCC2	External 5V/3.3V power supply
Vccop	VCC_OP	The power supply for current detection amplifier (5V/3.3V)
Vcph	VCPH	Charge pump voltage (for high sides)
Vcpl	VCPL	Charge pump voltage (for low sides)
AGND	AGND1,AGND2	GND for analog circuitry
PGND	PGND1,PGND2,PGND3	Power GND

Functional descriptions

(1) Charge pump circuit

TB9081FG build in Charge pump for Pre-Drivers and it can control external Nch MOSFETs directly. Two charge pump voltages the object for the high side drive of a motor and the object for the relay drive of a motor, and for the low side drive of a motor is generated.

The charge pump voltage (Vcph) for a high side drive and a relay drive control by an internal circuit, and if Vcph goes up to Vb+12V (Typ.), a charge pump will suspend operation. Furthermore, in consideration of an overvoltage state, if Vcph goes up to 37V (Typ.), a charge pump will stop, and if Vcph is less than 36.5V (Typ.), a charge pump will resume operation.

The charge pump voltage (Vcpl) for a low side drive is generated from Vcph. If Vcpl goes up to 16V (Typ.), a clamp will start and it will not become the voltage more than clamp voltage.

It is possible to build the switching circuit (CP_SW) in the Vb side of a charge pump circuit, to make a transistor turn off by CP_SW, and to stop the supply to Vcph from Vb. Vcc voltage turns off the transistor of CP_SW on condition of the conditions as for which below Vcc voltage detection voltage becomes, or EN_CP=L. For details, please refer to a (7) EN_CP circuit.

Moreover, it is possible to operate or stop a charge pump by terminal EN_CP. The charge pump operates at the time of EN_CP="H", and it stops at the time of EN_CP="L" and also suspends the supply to Vcph from Vb .

A Vcph output voltage is set to 0V at the time of the charge-pump stop by EN_CP="L."

When the charge pump is stopped by the control in the IC, Vcph output voltage will become the "Vb-3VF".

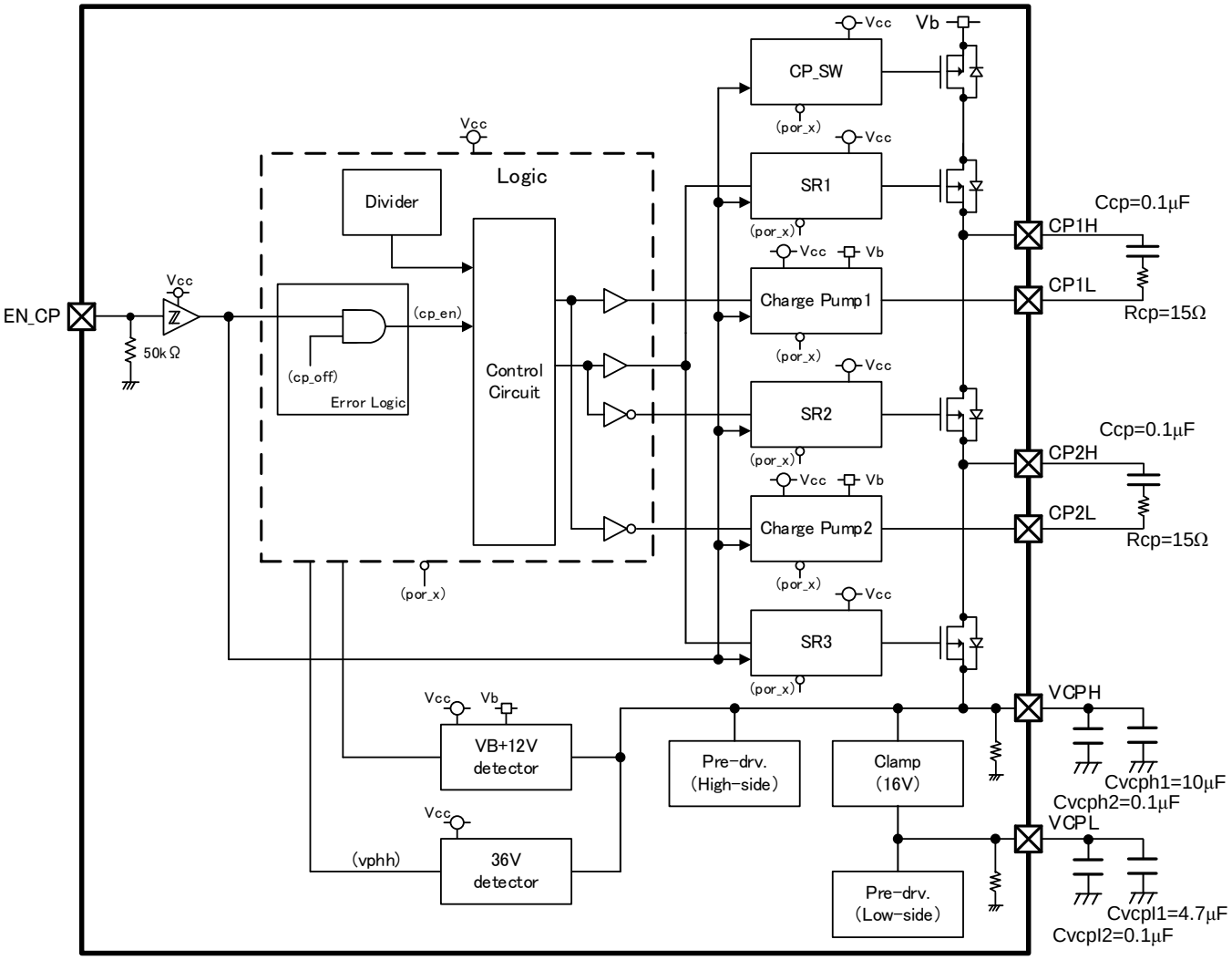


Fig.1- a Charge pump circuit Block Diagram

(2) Pre-drivers

TB9081FG has the pre-driver circuit it is for the motor relay drive, for the power relay drive, for the low-side drive of the motor and for the high-side drive of the motor. Each pre-driver circuit has a respective input and output terminals are controlled by a signal inputted to the input terminals.

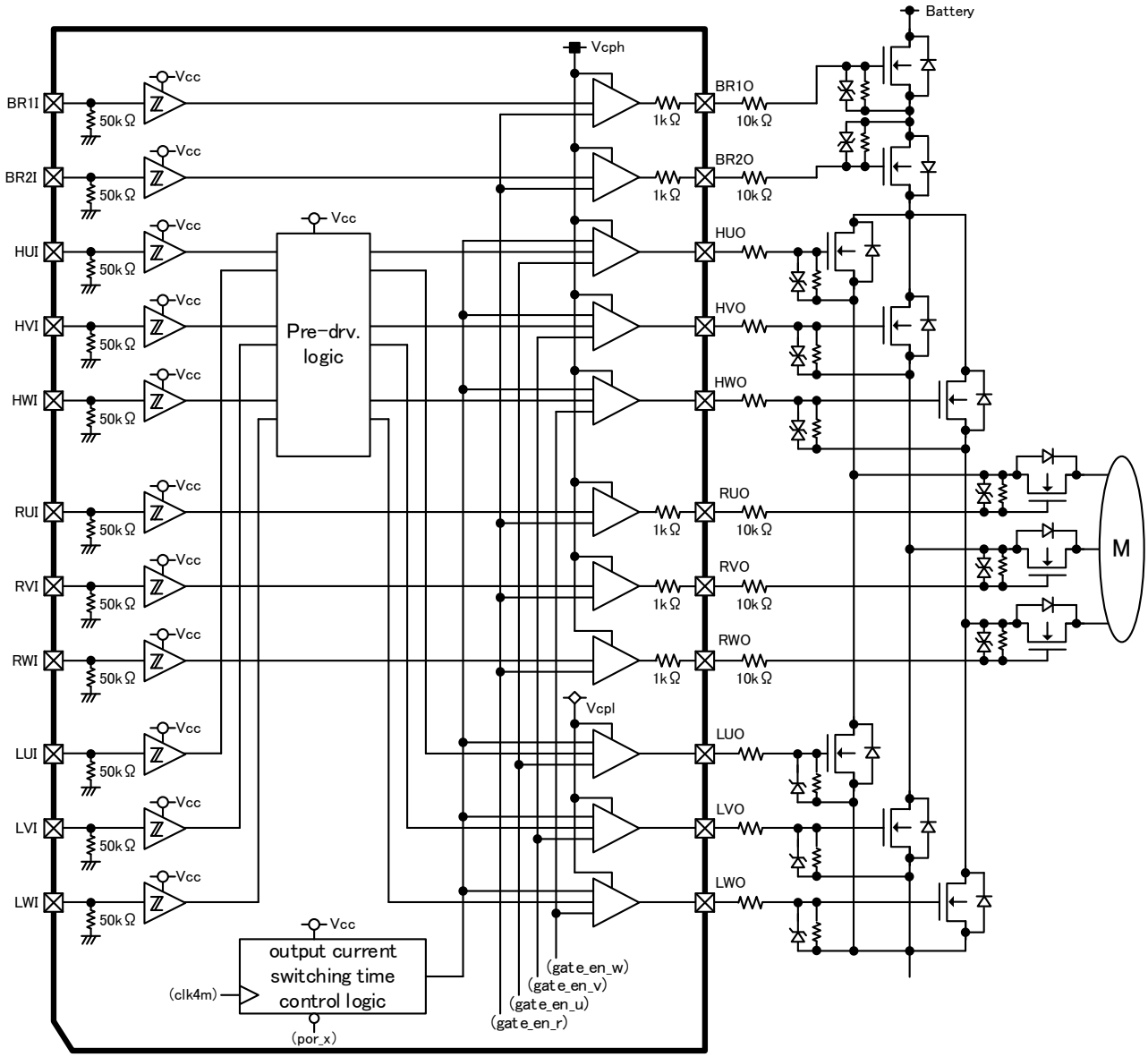


Fig.2- a Pre-driver circuit Block Diagram

<A power supply relay drive circuit, a motor relay drive circuit>

A power supply relay drive circuit is a circuit which controls FET for a relay on the battery power-supply side.

A motor relay drive circuit is a circuit which controls FET for a relay on the motor side.

A truth table is shown in table 2-a and 2-b. Refer to the (6) ALARM input circuit for the details of the internal signal (gate_en_r) in a truth table.

Moreover, resistance 1kΩ is built in the output of a power supply relay drive and a motor relay drive.

Furthermore, the diode for prevention of backflow at the time of reverse connection is built in the output of a power supply relay drive circuit.

- Table 2- a Input/output truth table 1 (power supply relay drive circuit)

- Power supply relay drive circuit 1

Input	Internal signal	Output	Notes
BR1I	(gate_en_r)	BR1O	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Power supply relay drive circuit 2

Input	Internal signal	Output	Notes
BR2I	(gate_en_r)	BR2O	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Table 2- b Input/output truth table 2 (motor relay drive circuit)

- Motor relay drive circuit 1 (U phase)

Input	Internal signal	Output	Notes
RUI	(gate_en_r)	RUO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Motor relay drive circuit 2 (V phase)

Input	Internal signal	Output	Notes
RVI	(gate_en_r)	RVO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Motor relay drive circuit 3 (W phase)

Input	Internal signal	Output	Notes
RWI	(gate_en_r)	RWO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

<A high side drive circuit, a low side drive circuit>

A high side drive circuit is a circuit which drives FET of the high side of a motor. A low side drive circuit is a circuit which drives FET of the low side of a motor. A high side drive circuit and a low side drive circuit built in each 3ch.

An input signal (HUI/HVI/HWI, LUI/LVI/LWI) is changed by a control block, and output (HUO/HVO/HWO, LUO/LVO/LWO) is outputted. A truth table is shown in table 2-c. Refer to the (6) ALARM input circuit for the details of the internal signal (gate_en_u, gate_en_v, gate_en_w) in a truth table.

When HUI/LUI, HVI/LVI, and HWI/LWI are H/H, an output will be L/L (prohibition input). The operation at the time of prohibition input detection can be set up through a SPI communication.

Moreover, the current at the time of Turn on/Turn off of a high side drive circuit and a low side drive circuit is the current limit after 8 μs (typ.). This current-limiting time can be set up a 3 value or no limit time through a SPI communication.

When gate_en_u, gate_en_v, and gate_en_w switch from “H” to “L” by the failure detection and ALARM1 or ALARM2 outputting low, and then, the high side drive circuit and the low side drive circuit output high, it switches to “L”. At this time, it has an output current capability which is decided by the ON resistance and the gate resistance of the output driver during the current limit time. However, only Vcc under voltage detection, the output current capability will be the output limit current Iolmtl even within the current limit time.

- Table 2- c Input/output truth table 3 (a high side drive circuit, a low side drive circuit)

- FET drive circuit 1 (U phase)

Input		Internal signal	Output		Notes
HUI	LUI	(gate_en_u)	HUO	LUO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

- FET drive circuit 2 (V phase)

Input		Internal signal	Output		Notes
HVI	LVI	(gate_en_v)	HVO	LVO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

- FET drive circuit 3 (W phase)

Input		Internal signal	Output		Notes
HWI	LWI	(gate_en_w)	HWO	LWO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

(3) Current detector

TB9081FG are built three amplifiers for motor-current detection and one amplifier for reference voltage generation (Fig3- a).
The amplifiers for motor-current detection can amplify the difference voltage which produces according to the current which flows through the shunt resistance connected to the motor actuator.
The amplifier for reference voltage generation is used as buffer amplifier for reference voltage generation.
As an external configuration of the current detection, it is available in either 1 shunt configuration or 3 shunt configuration.

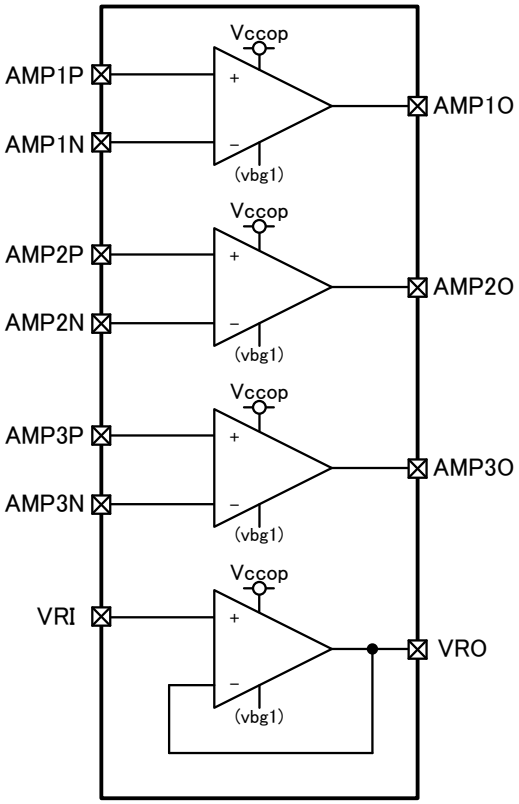


Fig.3- a Motor-current detection circuit Block Diagram

(4) Oscillator /divider

The oscillator has composition with built-in CR, and an Oscillation frequency is Fc=4MHz (typ.). An oscillator will start operation after internal signal (por_x) release.
4 MHz (clk4m) is used as the system clock of a logic circuit, and an operation clock of the digital filter of the short-circuit detector of external FET.
Clock 1MHz (clk1m), it is used as an operation clock of the digital filter of an ALARM detector.
Clock 500kHz (clk500k), it is used as an operation clock of a charge pump.
Clock 16kHz (clk16k), it is used as an operation clock of ABIST.
CLKOUT output (terminal) will output a clock set by the SPI (clk4m, clk500k, clk16k).

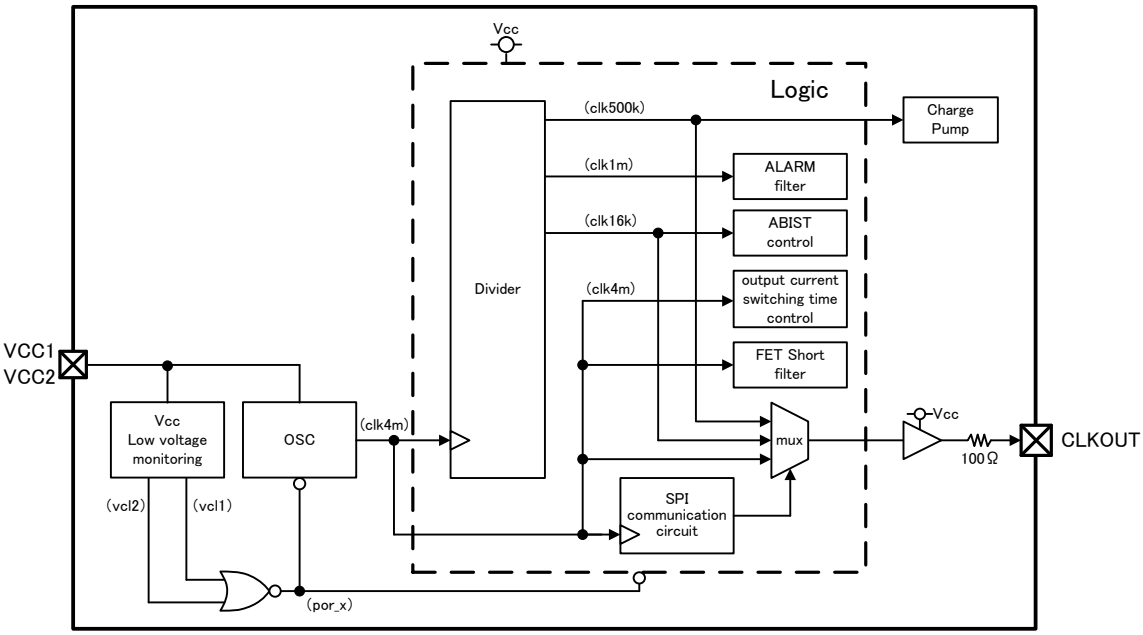


Fig.4- a Oscillator, divider Block Diagram

<Timing chart of divider>

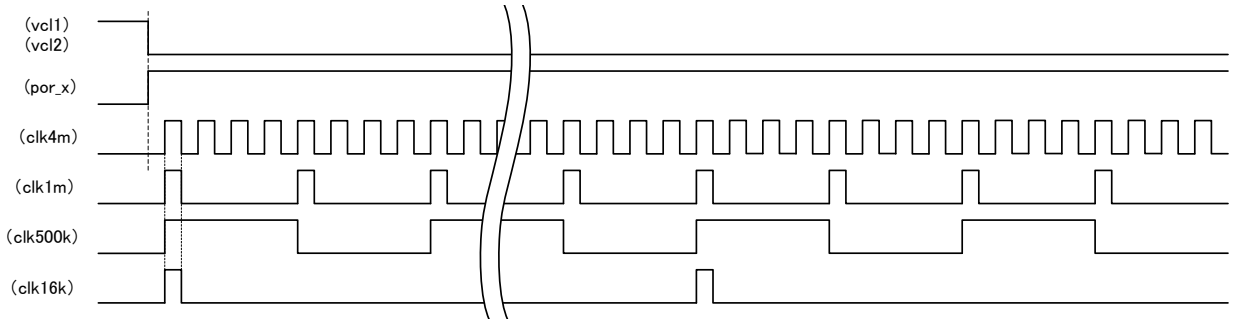


Fig.4-b Timing chart of divider

(5) Abnormal detection circuit

TB9081FG is built in miscellaneous abnormal detection circuit, such as the under voltage detection (VB1, VB2, VCC1, VCC2), over voltage detection (VCC1, VCC2), over temperature detection, external FET short-circuit detection and frequency abnormal detection.
The contents of a monitoring function list and the internal signal are shown below.
The details of operation are indicated in (5-1) and after.
When failure detection turns off the pre-driver circuit, the short-circuit detection function becomes invalid. When the operation returns from the abnormalities after that and the operation of a pre-driver circuit returns, a short-circuit detection function becomes effective again.

●Monitoring function list

Monitoring function	SPI Setup	Setup bit	Operation in detection *Note 1 *Note 5	Initial value	ABIST	Register writing	NDIAG * Note 2 * Note 4
VB1/VB2 Under voltage	Valid	00	pre-driver circuit OFF	−	−	○	L hold
		01	pre-driver circuit OFF	○		○	L
		1*	pre-driver circuit OFF	−		○	H
VCC1/VCC2 Under voltage	Invalid	−	Pre-driver / charge pump / dividing circuit OFF	−	−	−	L
VCC1/VCC2 Over voltage	Valid	00	Pre-driver / charge pump circuit continued operation	−	○	○	L hold
		01	Pre-driver circuit OFF	○			
		10	Pre-driver / charge pump circuit OFF	−			
		11	pre-driver / charge pump circuit OFF-hold	−			
Over temperature	Valid	00	Pre-driver / charge pump circuit continued operation	−	○	○	L hold
		01	pre-driver circuit OFF	−			
		10	pre-driver / charge pump circuit OFF	○			
		11	pre-driver / charge pump circuit OFF-hold	−			
External FET Short-circuit	Valid	000	Pre-driver / charge pump circuit continued operation	−	−	○	L hold
		001	Pre-driver-circuit(only detection phase) OFF	−			
		010	Pre-driver circuit (only detection phase) OFF-hold	○			
		011	Pre-driver circuit (all phases) OFF	−			
		100	Pre-driver circuit (all phases) OFF-hold	−			
		101	Pre-driver (all phases) / charge pump circuit OFF	−			
		110	Pre-driver (all phases) / charge pump circuit OFF-hold	−			
		111	No detection	−		−	H
Abnormalities in frequency	Valid	000	Pre-driver / charge pump circuit continued operation	−	○ (Low frequency)	○	L hold
		001	Pre-driver circuit OFF	−			
		010	Pre-driver / charge pump circuit OFF	−			
		011	Pre-driver / charge pump OFF-hold	−			
		1**	No detection	○		−	H
Pre-driver prohibition input detection *Note 3	Valid	0	Pre-driver OFF, when inputting inhibit signals. charge pump circuit continued operation	○	−	−	H
		1	Pre-driver OFF, when inputting inhibit signals. charge pump circuit continued operation	−		○	L hold
SPI communication error	Invalid	−	Pre-driver / charge pump circuit continued operation	−	−	○	L hold

*:don't care

Note 1) It describes about Pre-driver, charge pump and divider.
The definition of OFF and OFF-hold is as follows.
OFF: the operation after returning from an abnormal state is possible.
OFF-hold: Hold OFF even after returning from an abnormal state.

Note 2) It describes about NDIAG operation in detection.
The `L hold` hold the output NDIAG=L even after releasing from the abnormal detection.

Note 3) If register setting=0, there is no register writing and NDIAG becomes H, even in case of the abnormal detection.
If register setting=1, it has register writing and NDIAG becomes L, in case of the abnormal detection.

Note 4) if set to other than `L hold` in NDIAG, register will be cleared and NDIAG=H by recovering from the abnormal detection,

Note 5) Both Pre-driver circuit (all phases) OFF and Pre-driver circuit OFF turn off power relay and motor relay Pre-driver. Pre-driver-circuit(only detection phase) OFF turns off the high side and the low side Pre-driver of detected phase only.

(5-1) VB1/VB2 under voltage detection

Under voltage detection of VB1/VB2 is performed. Two detection comparators and two filters are built in. If at least one filter outputs “H”, under voltage detection is performed.
The band gap voltage recognized as the reference of a detection comparator is generated from a separate band gap circuit (BG1 and BG2).

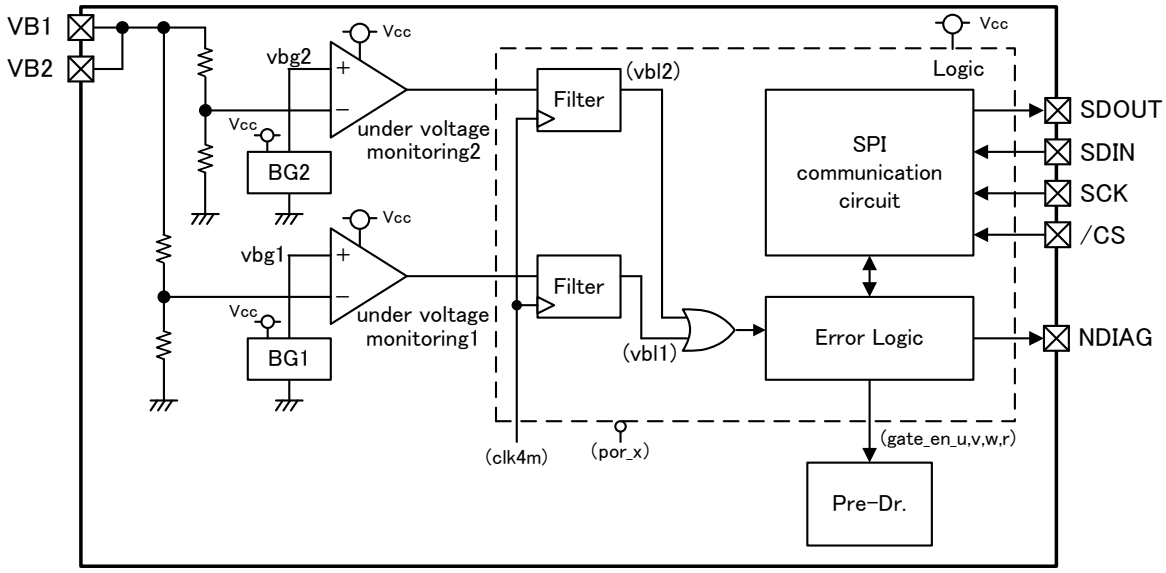


Fig.5-1a VB1/VB2 under voltage detection Block Diagram

➢ A-(1) Under voltage of Vb

If VB1 voltage and VB2 voltage are less than the threshold value of the under voltage detection voltage (vthbll), L detection comparator of Vb outputs “H”.

➢ A-(2) Under voltage detection of Vb

After the detection filter time (Tbl), Vb under voltage detection signal (vbl1 and vbl2) outputs high, the under voltage state is detected, and the pre-driver circuit is turned off. The oscillating circuit and the charge pump circuit are not turned off.

The pre-driver circuit holds OFF until the under voltage is released.

The NDIAG output state after detection can be chosen among the 3 modes through SPI communication.

A setup does not become effective even if the mode is changed in Vb under voltage detection state. The setup becomes effective after Vb under voltage is released and the register (uvb) is cleared.

➢ A-(3) Return of Vb voltage (under voltage release)

If VB1 voltage and VB2 voltage exceed vthblh, Vb under voltage detection signal (vbl1 and vbl2) outputs low, the under voltage state is released, and the pre-driver circuit recovers to the normal operation. In case NDIAG outputs low, it outputs high when the register (uvb) is cleared through SPI communication.

During under voltage detection, NDIAG outputs low because the register (uvb) is not cleared.

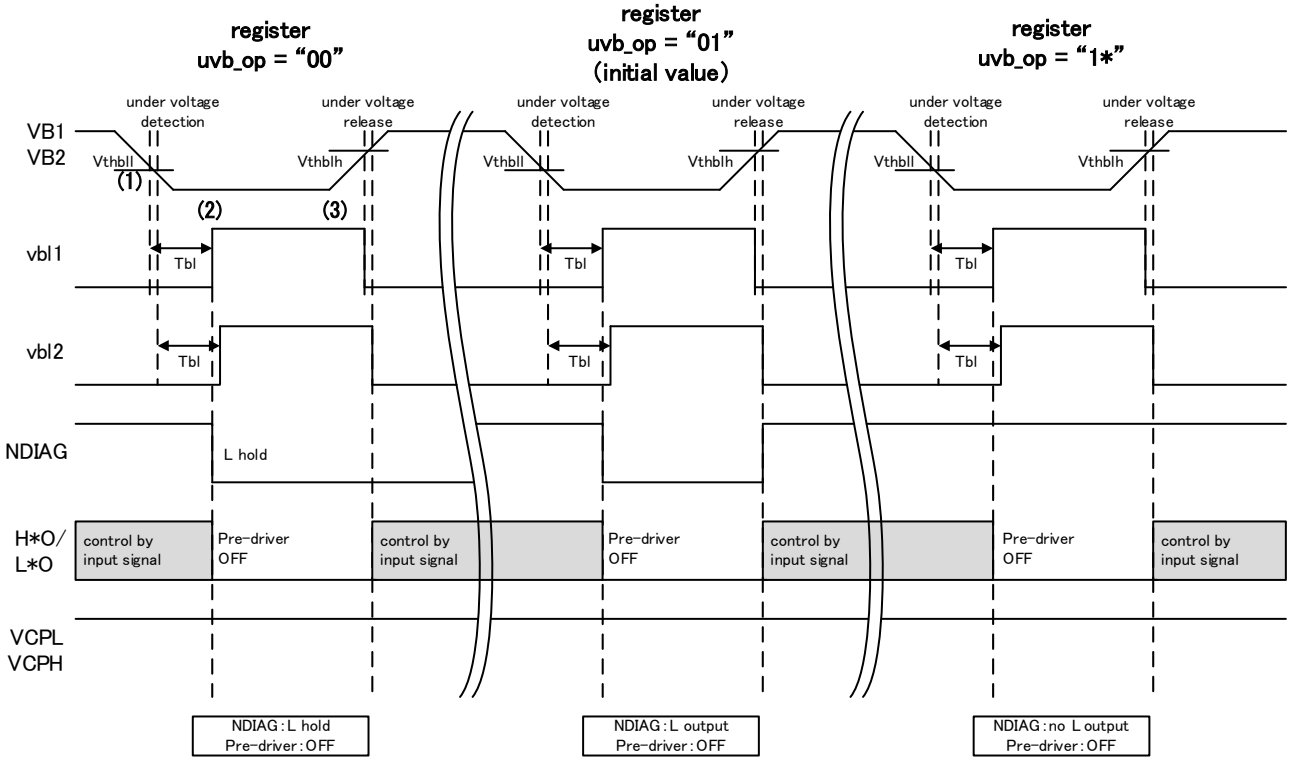


Fig.5-1b Timing chart of VB1/VB2 under voltage detection

(5-2) VCC1/VCC2 under voltage detection

Under voltage detection of VCC1/VCC2 is performed. Two detection comparators are built in. If at least one comparator outputs “H”, under voltage detection is performed.
The band gap voltage recognized as the reference of a detection comparator is generated from a separate band gap circuit (BG1 and BG2).

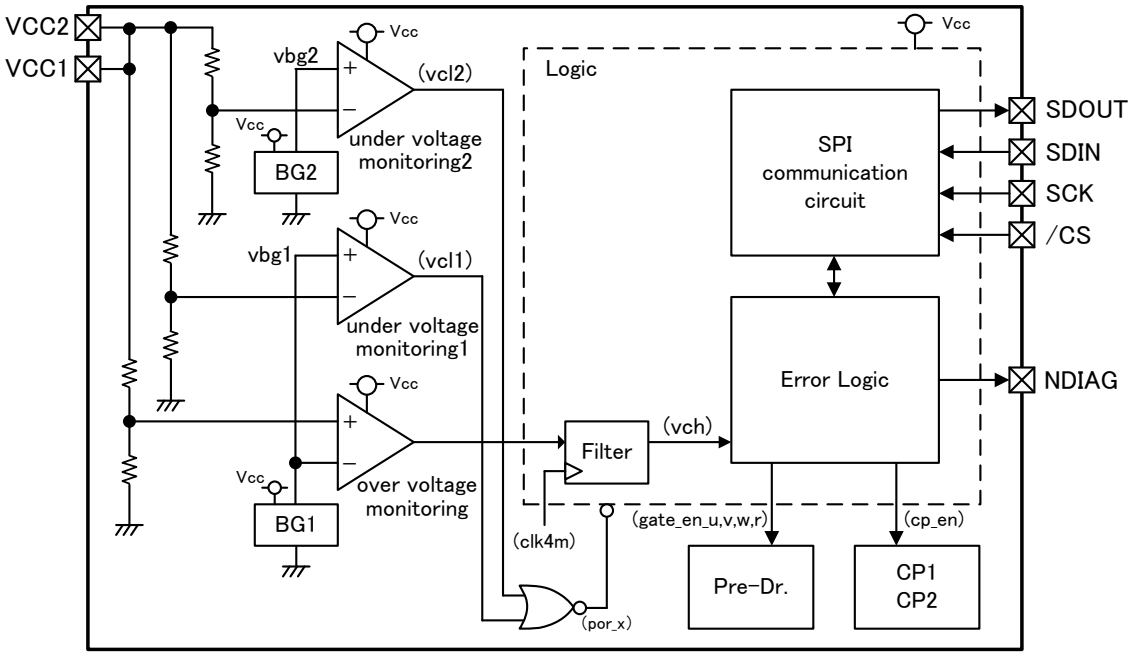


Fig.5-2a VCC1/VCC2 under voltage detection Block Diagram

➢ B-(1) Under voltage of Vcc

VCC1 voltage and VCC2 voltage are less than the threshold value of the under voltage detection voltage (vthcll).

➢ B-(2) Under voltage detection of Vcc

After the response relaxation time (Tcl), Vcc under voltage detection signal (vcl1 and vcl2) outputs high, the under voltage state is detected, por_x outputs low, and NDIAG outputs low. Then, the pre-driver circuit, the charge pump, and the oscillating circuit are turned off.

Each circuit holds OFF until the under voltage is released.

➢ B-(3) Return of Vcc voltage (under voltage release)

If VCC1 voltage and VCC2 voltage exceed vthclh, Vcc under voltage detection signal (vcl1 and vcl2) outputs low, and the under voltage state is released.

➢ B-(4) Recover of normal operation

After LBIST and ABIST are performed, the normal operation recovers in case the judgment of BIST "OK". The charge pump circuit starts operation and the pre-driver circuit is turned on. In case the judgment of BIST "NG", the charge pump circuit and the pre-driver circuit do not operate.

NDIAG outputs high in the judgment of "OK", and low in the judgment of "NG".

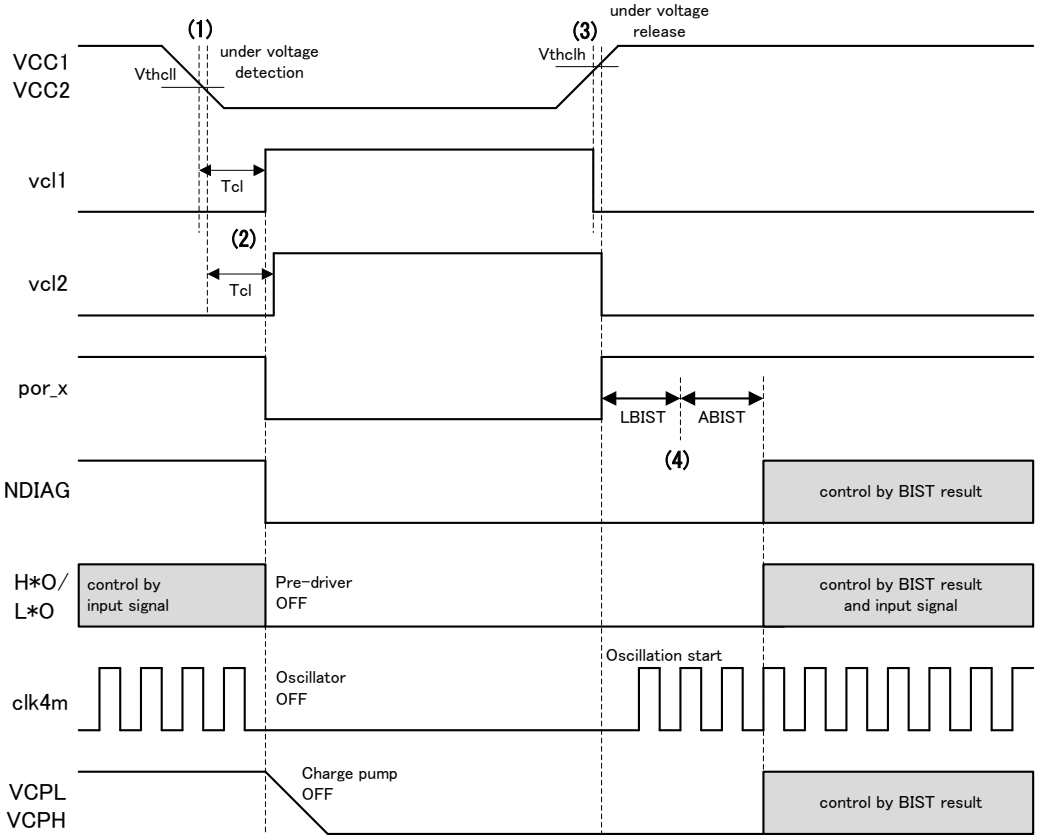


Fig.5-2b Timing chart of VCC1/VCC2 under voltage detection

* When Vcc is lower than the detection voltage of Vcc under voltage further, IC will be the stand-by state. In the stand-by state, functions other than Vcc under voltage detection are turned off.

(5-3) VCC1/VCC2 over voltage detection

Over voltage detection of VCC1/VCC2 is performed. The detection comparator and the filter are built in. If the filter outputs high, over voltage detection is performed.

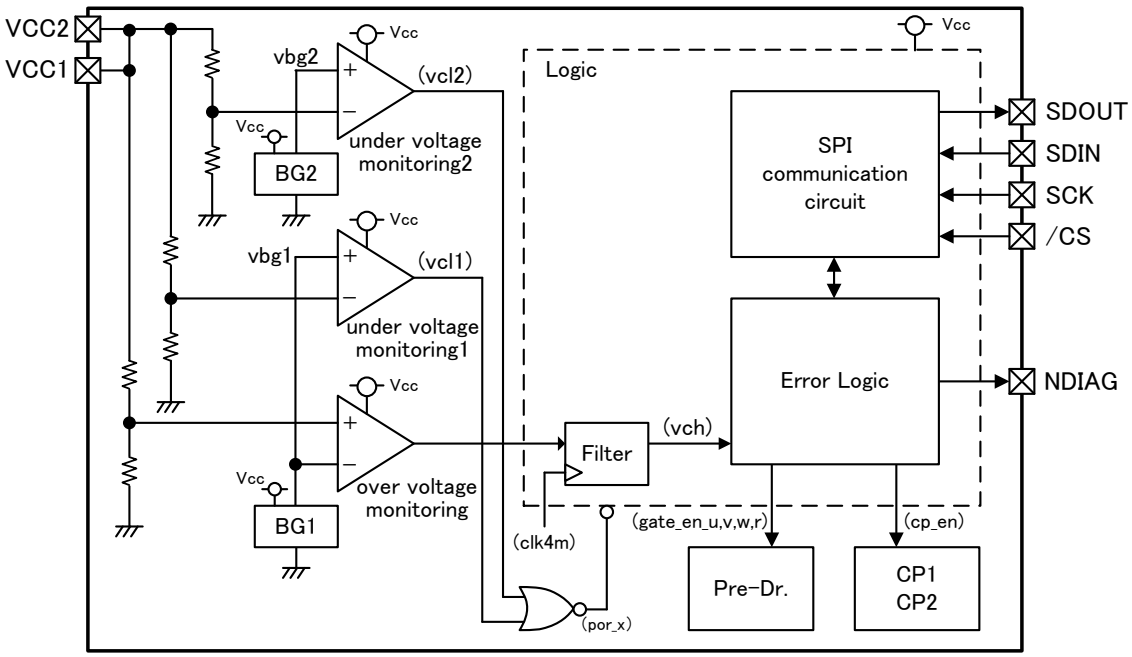


Fig.5-3a VCC1/VCC2 over voltage detection Block Diagram

➢ C-(1) Vcc voltage rise

If VCC1 voltage and VCC2 voltage exceed the threshold value of over voltage detection (vthchh), H detection comparator of Vcc outputs high.

➢ C-(2) Over voltage detection of Vcc

After the detection filter time (Tch), Vcc over voltage detection signal (vch) outputs high and NDIAG outputs low.

The operation after detection can be chosen among 4 modes through SPI communication.

A setup does not become effective even if the mode is changed in Vcc over voltage detection state. The setup becomes effective after Vcc over voltage is released and the register (ovc) is cleared.

➢C-(3) Return of Vcc voltage (over voltage release)

If VCC1 voltage and VCC2 voltage are less than vthchl, Vcc over voltage detection signal (vch) outputs low and the over voltage is released.

In the case of register ovc_op is 11, even if the over voltage is released, each circuit continues OFF and NDIAG keeps outputting low. When the register (ovc_op) is 00, 01, and 10, each circuit operates normally and NDIAG keeps outputting low. When the register (ovc) is cleared through SPI communication, each circuit operates normally and NDIAG outputs high.

During over voltage detection, the register (ovc) is not cleared and NDIAG outputs low.

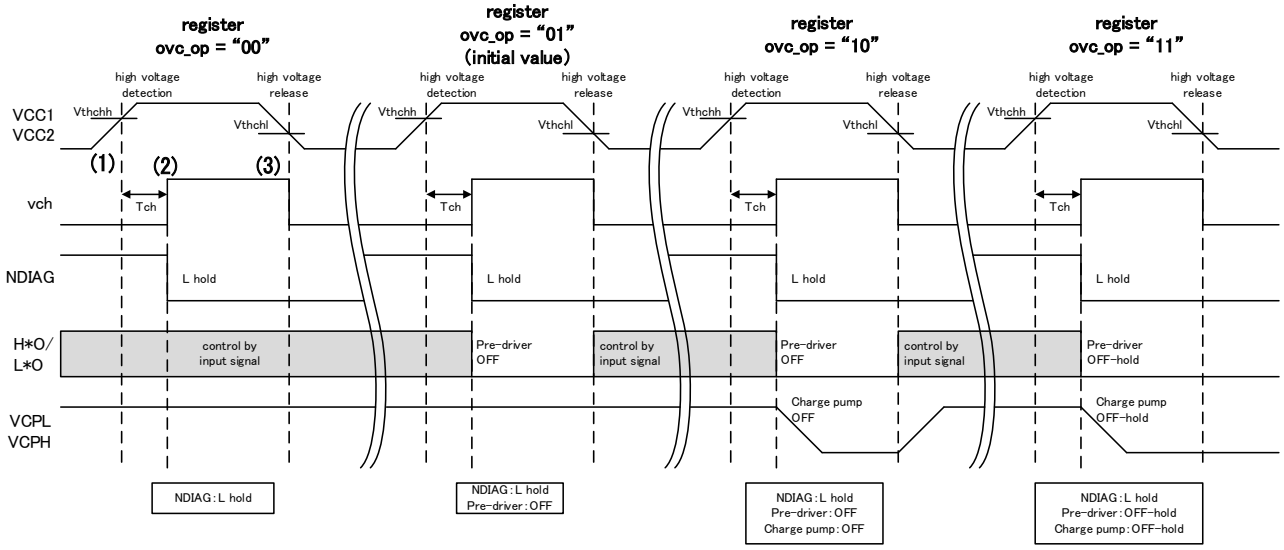


Fig.5-3b Timing chart of VCC1/VCC2 over voltage detection

(5-4) Over temperature detection

Three over temperature detection comparators are built in. Three detection comparators and three filters are built in. If at least one filter outputs high, the over temperature detection becomes effective.

The band gap voltage recognized as the reference of a detection comparator is generated from two band gap circuits (BG1 and BG2).

When chip temperature exceeds 170°C, the comparator switches and the over temperature is detected. The operation after detection can be chosen among 4 modes through SPI communication. When IC internal temperature becomes 160°C or less, the over temperature detection is released.

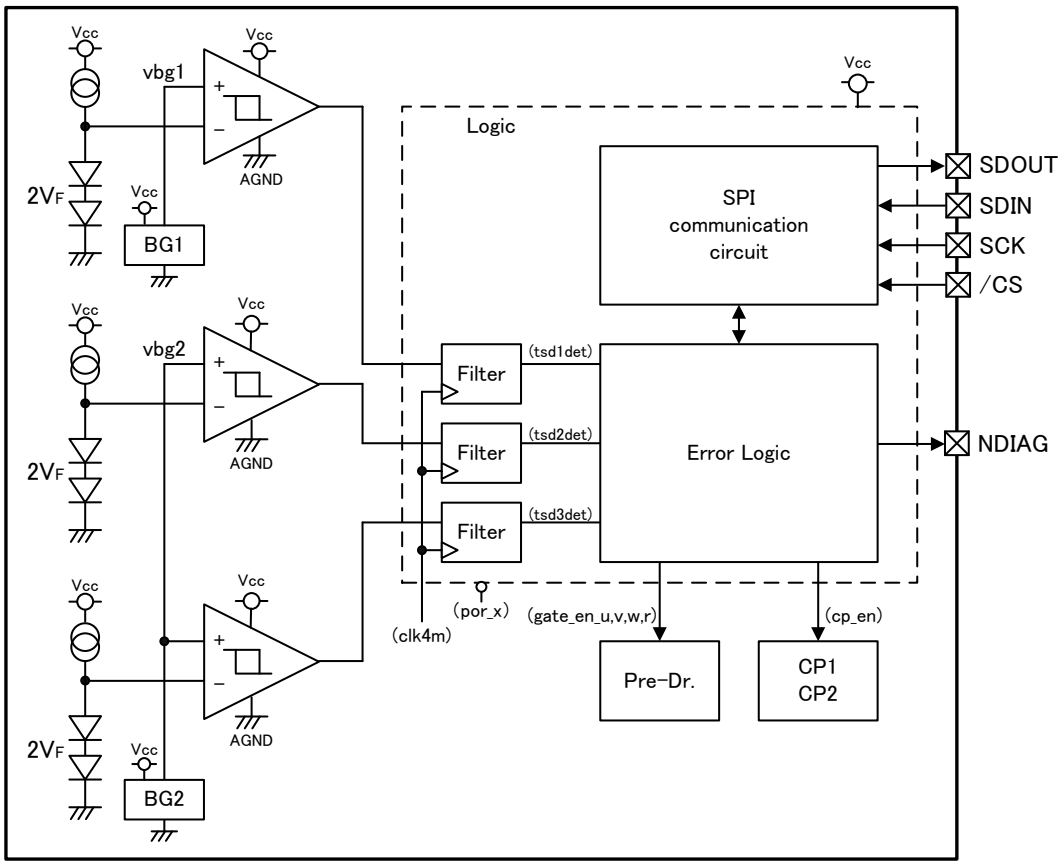


Fig.5-4a Over temperature detection Block Diagram

➢ D-(1) Over temperature detection

If the temperature exceeds Tsdh, after the detection filter time (Ttsd), the over temperature detection signal (tsd1 to 3det) outputs high, and the over temperature is detected.
The operation after detection can be chosen among 4 modes through SPI communication.
A setup does not become effective even if the mode is changed during over temperature state. The setup becomes effective when the over temperature state is released and the register (tsd*det) is cleared.

➢ D-(2) Release of over temperature detection

If temperature is less than Tsdl, the over temperature detection signal (tsd1 to 3det) outputs low, and the over temperature detection is released.
When register (tsd_op) is 11, even if the over temperature detection is released, each circuit continues OFF and NDIAG leeps outputting low. When the register (tsd_op) is 00, 01, and 10, each circuit operates normally. However, NDIAG holds low. When the register (tsd*det) is cleared through SPI communication, each circuit operates normally and NDIAG outputs high.
During over temperature detection, the register (tsd*det) is not cleared and NDIAG outputs low.

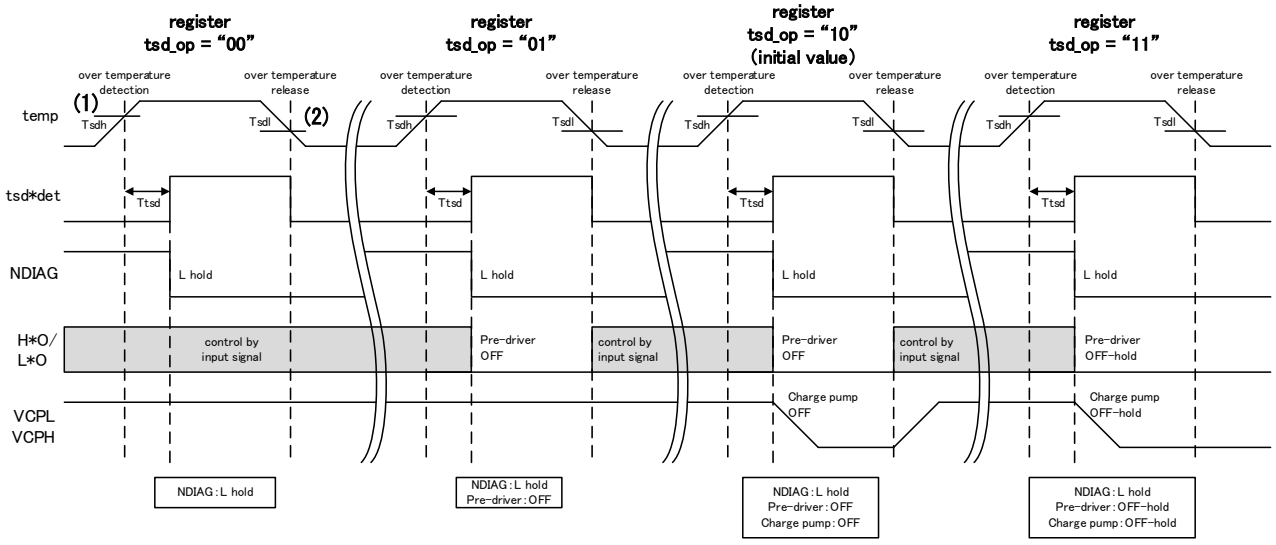


Fig.5-4b Timing chart of over temperature detection

(5-5) Short-circuit detection

Short-circuit of external MOSFET is detected by monitoring the dorain terminal and the source terminal of the external MOSFET.
When short-circuit is detected, the operation after detection can be chosen among 8 modes through SPI communication.
Moreover, detection threshold voltage and detection time can be set from four values through SPI communication.

At the time of short-circuit detection release, in case that the register (sh_op) is 010, 100, and 110, even if short-circuit detection is released, each circuit continues OFF and NDIAG holds L. When the register (tsd_op) is 000, 001, 011, and 101, each circuit operates normally, but NDIAG holds L. When the register (sc**) is cleared through SPI communication, each circuit operates normally and NDIAG outputs high.

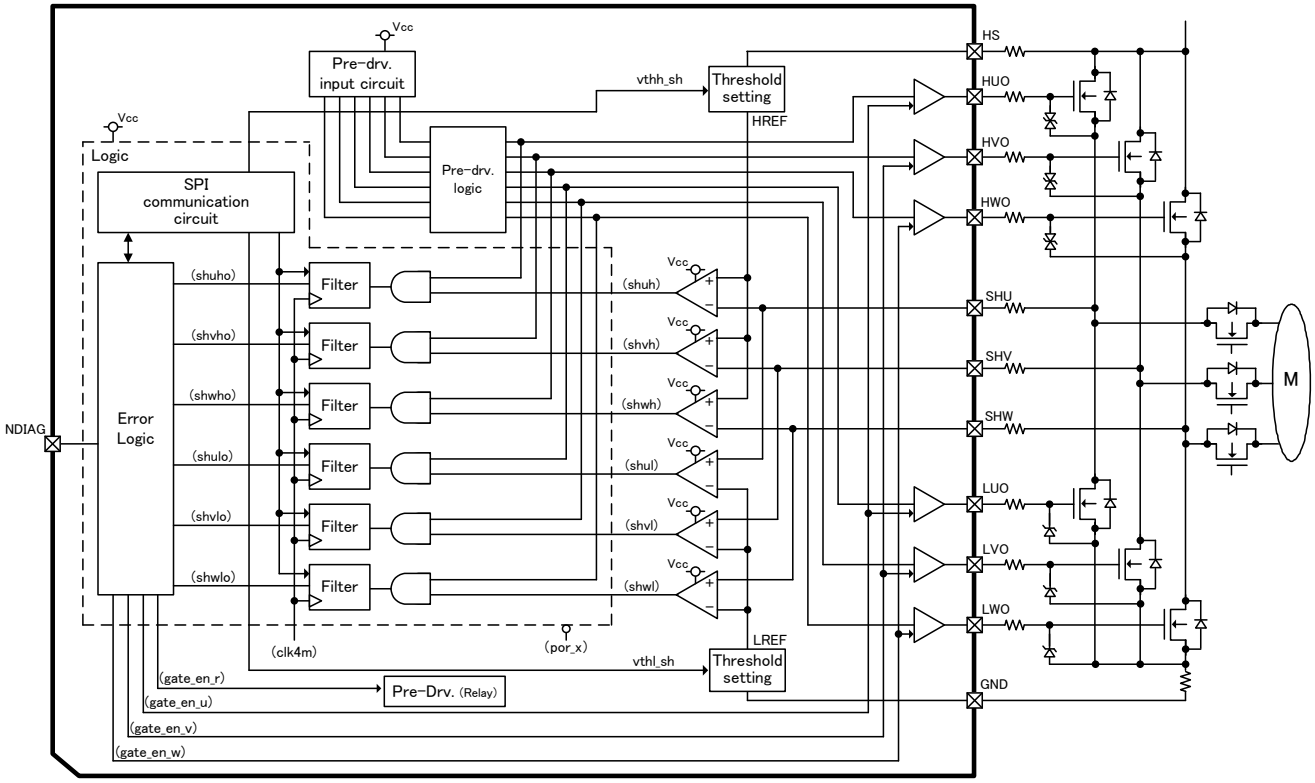


Fig.5-5a Short-circuit detection Block Diagram

●Table5-5a Short-circuit detection state

Comparator input	Comparator output	Input signal	Abnormal condition
SHU > LREF	shul = H	LUI = H	External MOSFET short-circuit of HUO
SHV > LREF	shvl = H	LVI = H	External MOSFET short-circuit of HVO
SHW > LREF	shwl = H	LWI = H	External MOSFET short-circuit of HWO
SHU < HREF	shuh = H	HUI = H	External MOSFET short-circuit of LUO
SHV < HREF	shvh = H	HVI = H	External MOSFET short-circuit of LVO
SHW < HREF	shwh = H	HWI = H	External MOSFET short-circuit of LWO

* HREF = HS- Vthh_sh (detection threshold voltage of the High side), LREF = Vthl_sh (detection threshold voltage of the Low side)
* The detection threshold voltage of the High side is specified between HS and SH* of the IC terminal.
Please set up the threshold value of HREF in consideration of the generating voltage by external resistance of HS terminal and SH* terminal, and the voltage between drain and source of MOSFET of the High side.
* The detection threshold voltage of the Low side is specified between SH* and PGND(s) of the IC terminal.Please set up the threshold value of LREF in consideration of the generating voltage by external resistance of SH* terminal, the generating voltage by the shunt resistance for current detection, and the voltage between drain and source of MOSFET of the Low side.

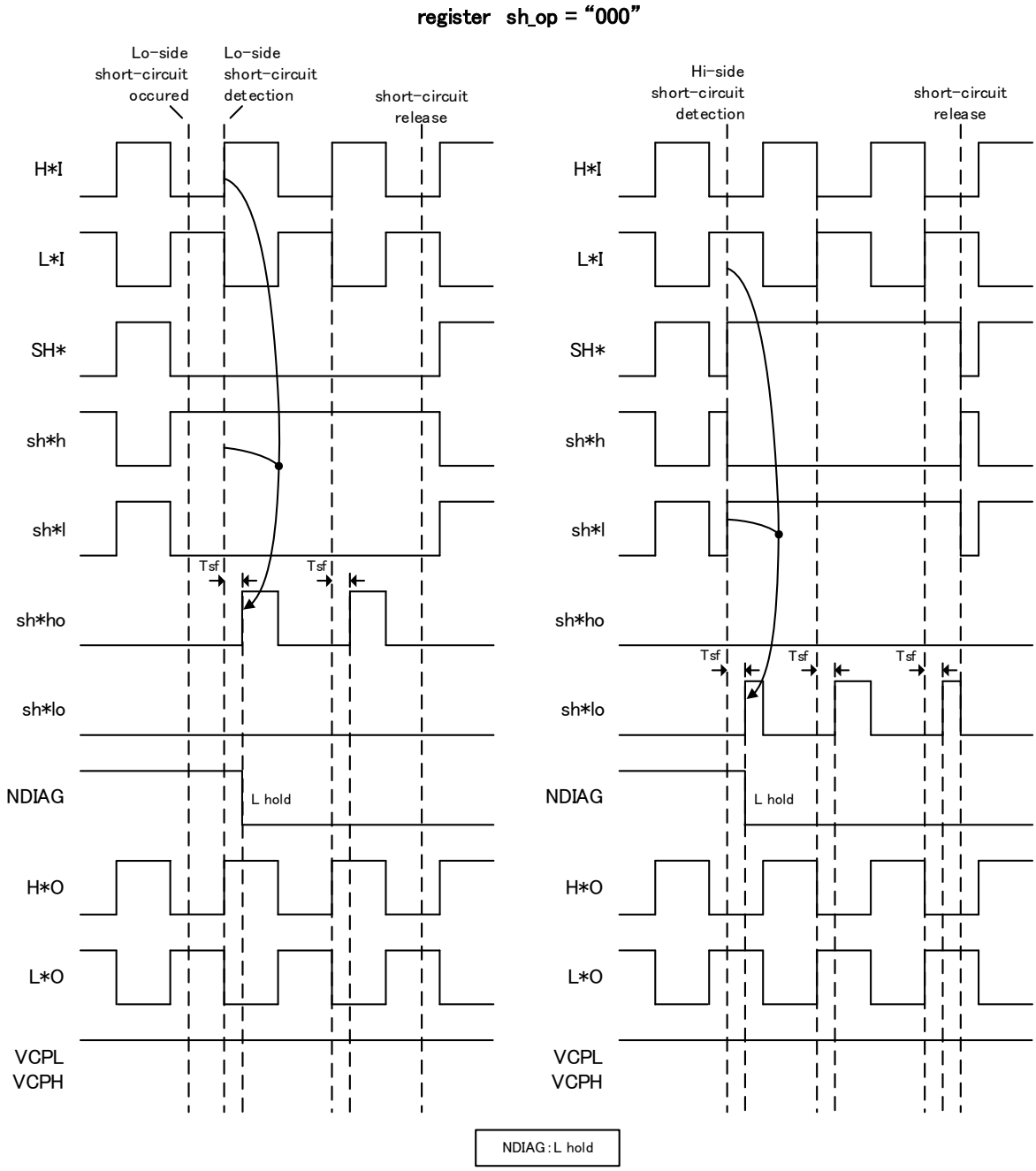


Fig.5-5b Timing chart of short-circuit detection (Register (sh_op) = ”000”)

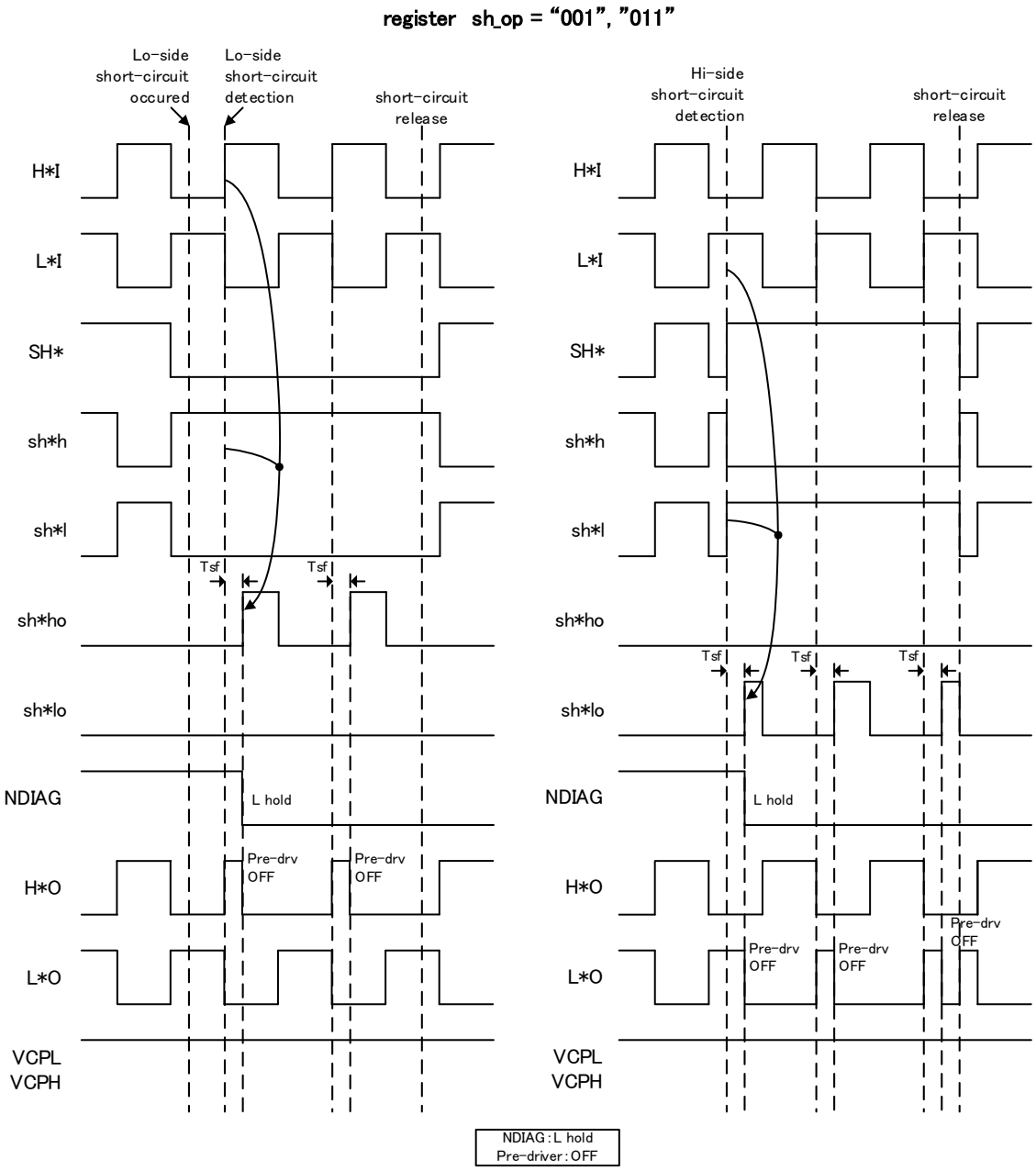


Fig.5-5c Timing chart of short-circuit detection (Register (sh_op) = ”001” and ”011”)

* "001" : Pre-driver OFF in only a detection phase.
"011": Pre-driver OFF in all phase

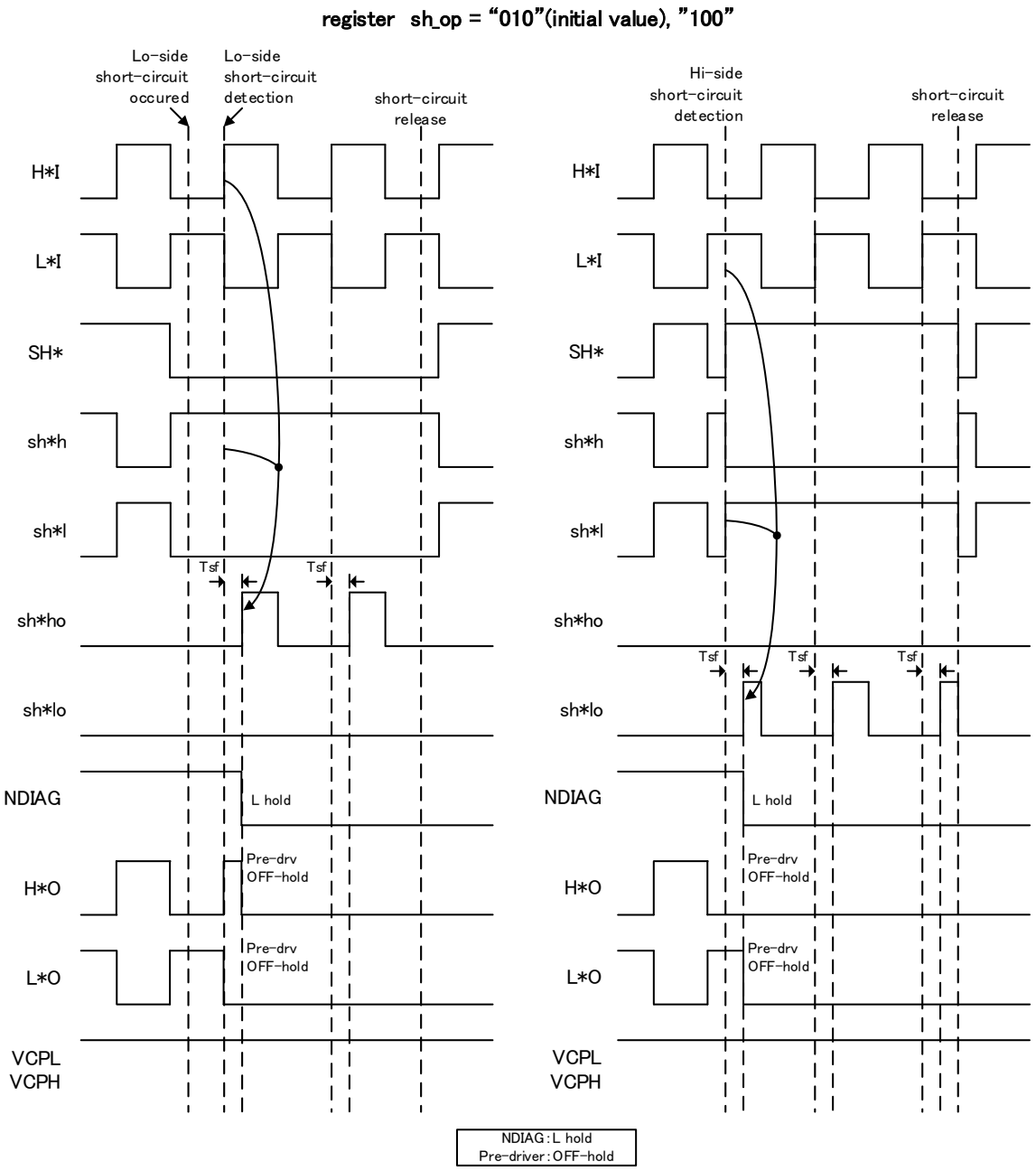


Fig.5-5d Timing chart of short-circuit detection (Register (sh_op) = ”010” and ”100”)

*”010”: Pre-driver OFF in only a detection phase
”100”: Pre-driver OFF in all phase

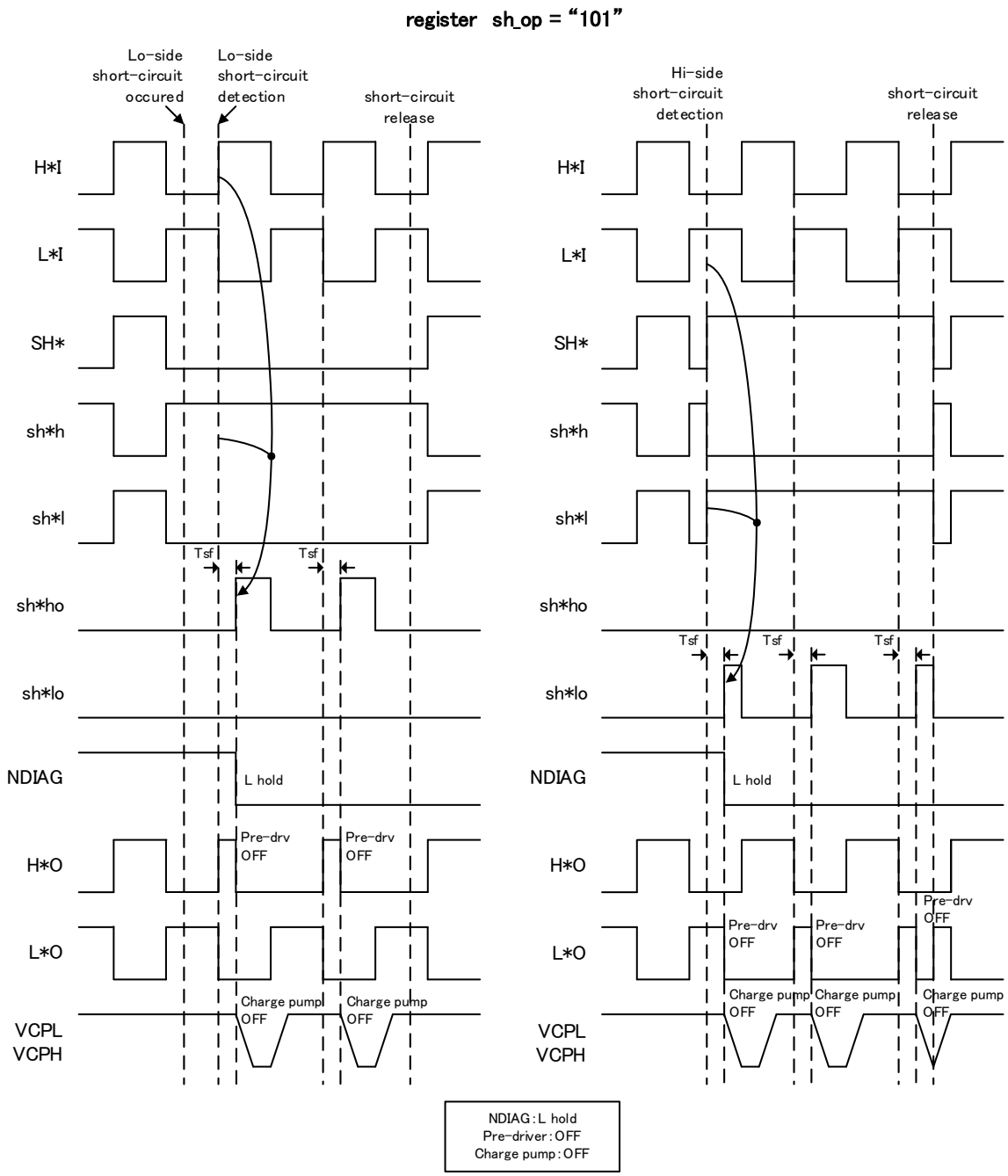


Fig.5-5e Timing chart of short-circuit detection (Register (sh_op) = "101")

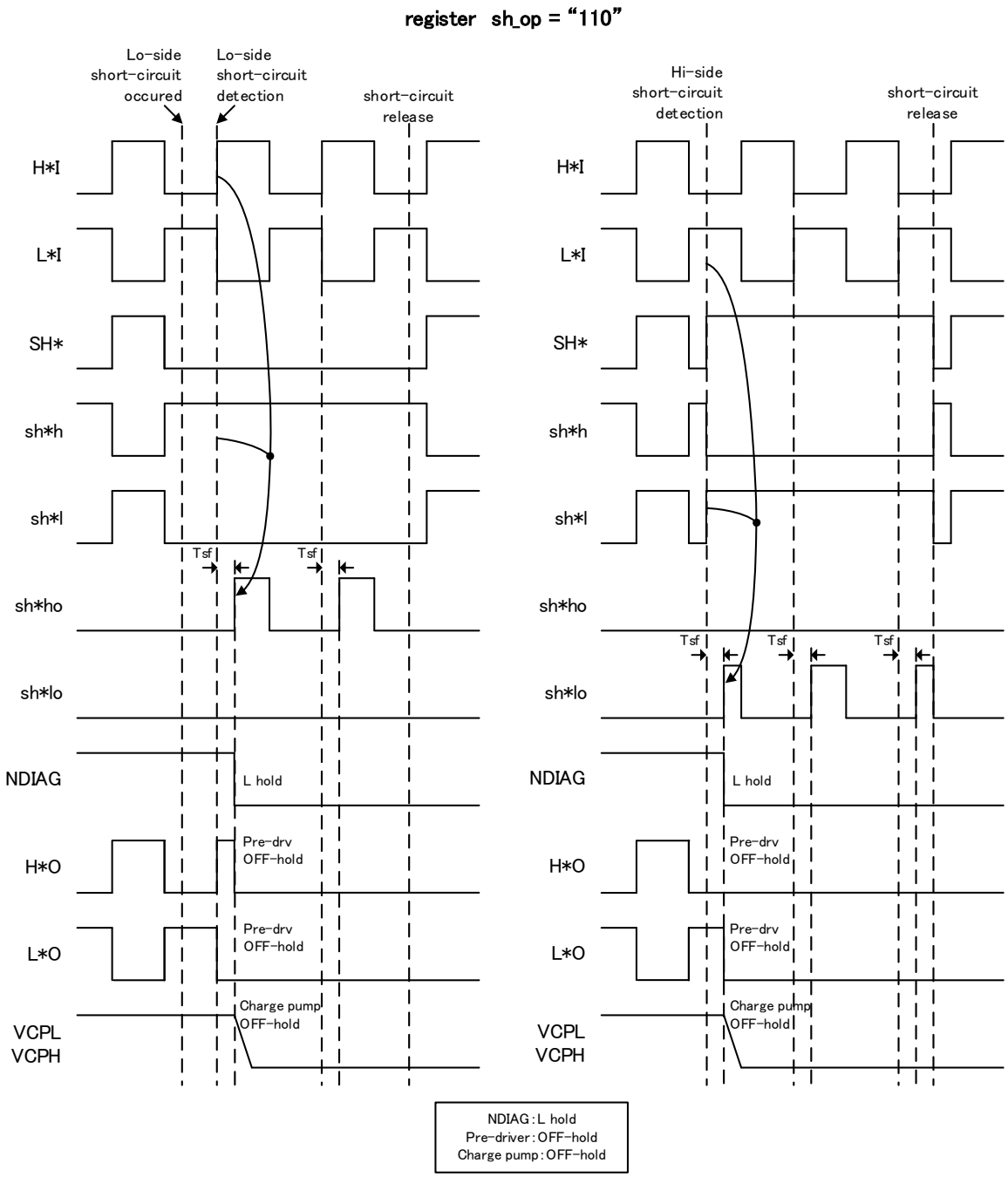


Fig.5-5f Timing chart of short-circuit detection (Register (sh_op) = ”110”)

(5-6) Oscillating frequency monitoring

It detects the abnormality in frequency when oscillating frequency is low and high.
The low frequency detection circuit of oscillating frequency resets the input of a comparator for every clk1m. If the frequency becomes low and reset is overdue, the output of a comparator is reversed and the abnormality in frequency is detected at the rising edge of the following clk1m.
In the high frequency detection circuit of the oscillating frequency, a comparator repeats H/L output for every clk1m. When oscillating frequency becomes high, a detection comparator continues outputting H, and the detection comparator continues outputting H at the falling edge of 1st count of clk1m, the abnormality in high frequency is detected.
The operation in failure detection can be chosen among 5 modes through SPI communication.
A setup does not become effective even if the mode is changed in the frequency failure detection state. The setup becomes effective after the abnormality in frequency are released and the register (err_of and err_uf) is cleared.
Abnormality of frequency is not detected in case that the register (ferr_op) is 1**.
When frequency failure detection is released, in case that the register (ferr_op) is 011, even if frequency failure detection is released, each circuit continues OFF and NDIAG holds L. In case that the register (ferr_op) is 000, 001, and 010, each circuit recovers to the normal operation. However, NDIAG holds L. When the register (err_of and err_uf) is cleared through SPI communication, each circuit recovers to the normal operation and NDIAG outputs high.

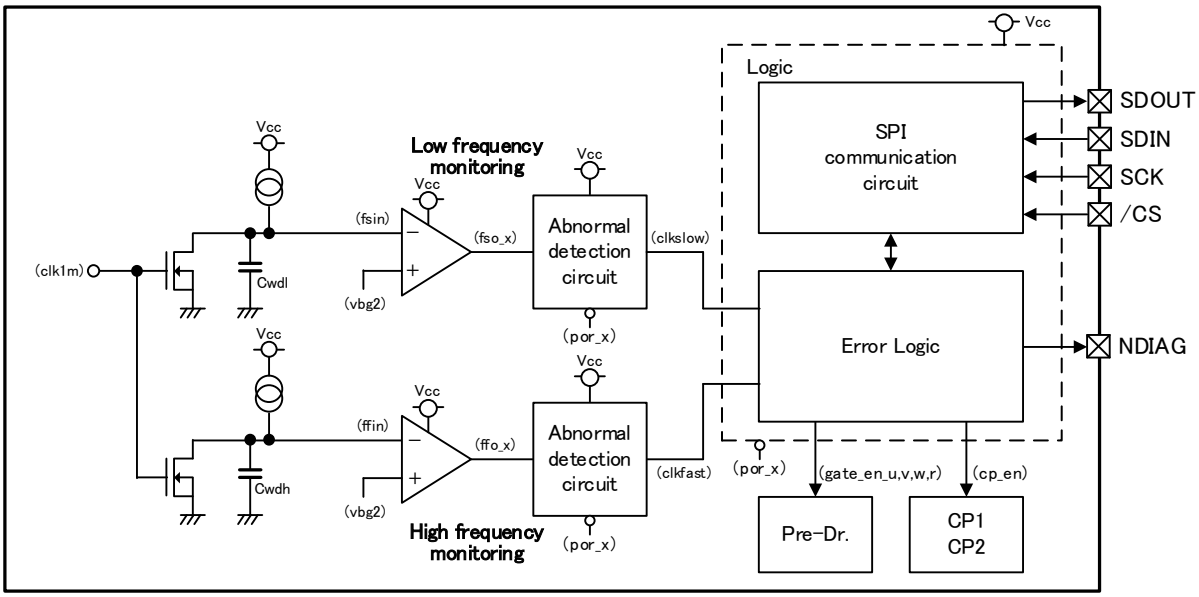


Fig.5-6a Frequency monitoring circuit

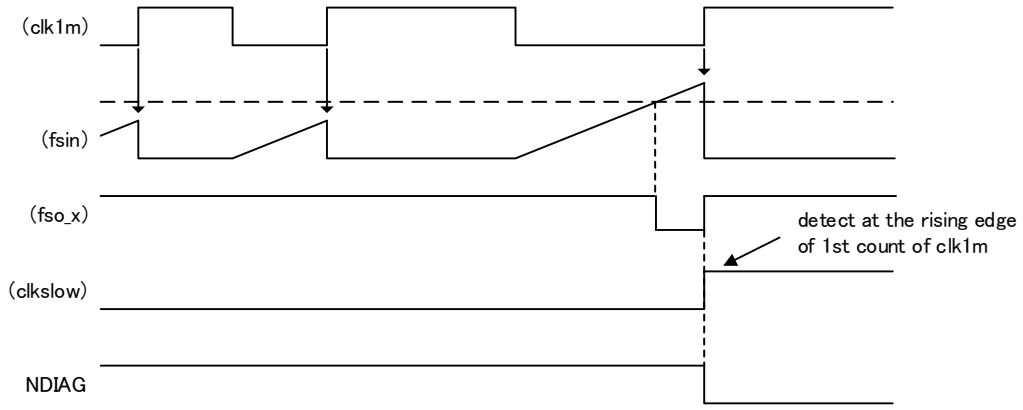


Fig.5-6b Timing chart of frequency monitoring (Low frequency)

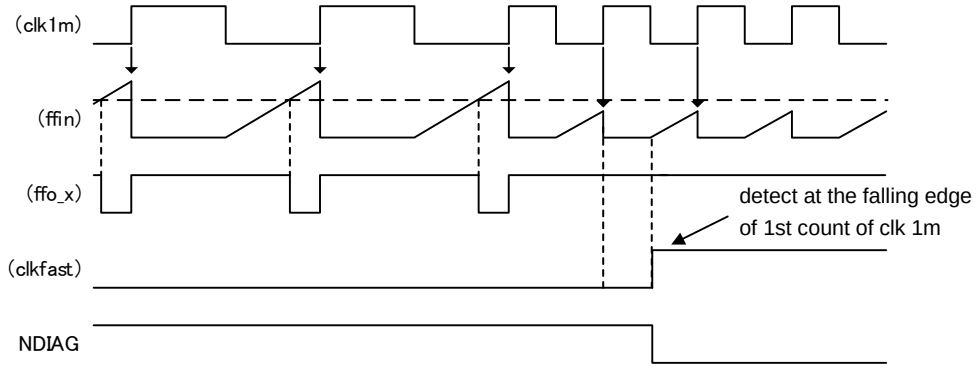


Fig.5-6c Timing chart of frequency monitoring (High frequency)

(6) ALARM input circuit

As an input terminal of an ALARM signal, TB9081FG have two terminals of ALARM1 and ALARM2.
An ALARM signal controls Enable/Disable of the Pre-drivers (a FET drive circuit, a motor relay drive circuit, a power supply relay drive circuit).
In the case of ALARM1= "L" or ALARM2= "L", the Pre-drivers will be Disable. In the case of ALARM1="H" and ALARM2="H", Enable/Disable is decided by the input and internal signal of each Pre-drivers.
Also, the input side of the ALARM1 and ALARM2 terminal has a built-in digital filter (D.F.) for noise removal. Digital filter time can be set through the SPI communication.
If ALARM1="L" or ALARM2="L" is detected, the short-circuit detection function is enabled.

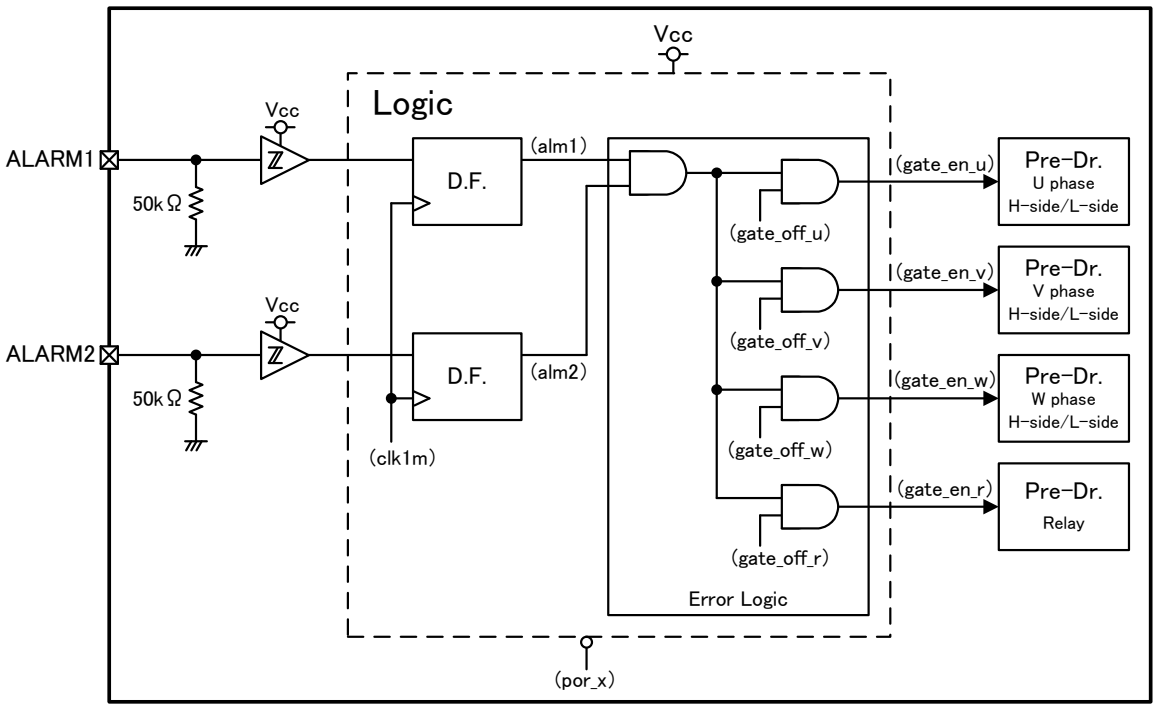


Fig.6-a FET drive circuit control Block Diagram

Table 6-a FET drive circuit control truth table

Input signal		Internal input signal					Internal control signal				FETdrive circuit
ALARM1	ALARM2	(por_x)	(gate_off_u)	(gate_off_v)	(gate_off_w)	(gate_off_r)	(gate_en_u)	(gate_en_v)	(gate_en_w)	(gate_en_r)	
L	*	*	*	*	*	*	L	L	L	L	Disable
*	L	*	*	*	*	*	L	L	L	L	Disable
*	*	L	*	*	*	*	L	L	L	L	Disable
H	H	H	L	-	-	-	L	-	-	-	U phase Disable
H	H	H	H	-	-	-	H	-	-	-	U phase Enable
H	H	H	-	L	-	-	-	L	-	-	V phase Disable
H	H	H	-	H	-	-	-	H	-	-	V phase Enable
H	H	H	-	-	L	-	-	-	L	-	W phase Disable
H	H	H	-	-	H	-	-	-	H	-	W phase Enable
H	H	H	-	-	-	L	-	-	-	L	Relay Disable
H	H	H	-	-	-	H	-	-	-	H	Relay Enable

(Note 1) "*": Don't care
(Note 2) Although "-":gate_off_* and gate_en_* have logic dependence in phase, the logic dependence to other phase is nothing.

(7) EN_CP input circuit

EN_CP signal controls Enable/Disable of a charge pump circuit.
In the case of input signal EN_CP= "L", the charge pump circuit will be Disable. In the case of EN_CP="H", Enable/Disable of the charge pump circuit is decided by an internal signal.
Also, the charge pump SW circuit (CP_SW) will be Disable in case of input signal EN_CP = "L" or the internal signal (por_x) = "L". In the case of EN_CP = (por_x) = "H", it will be Enable.

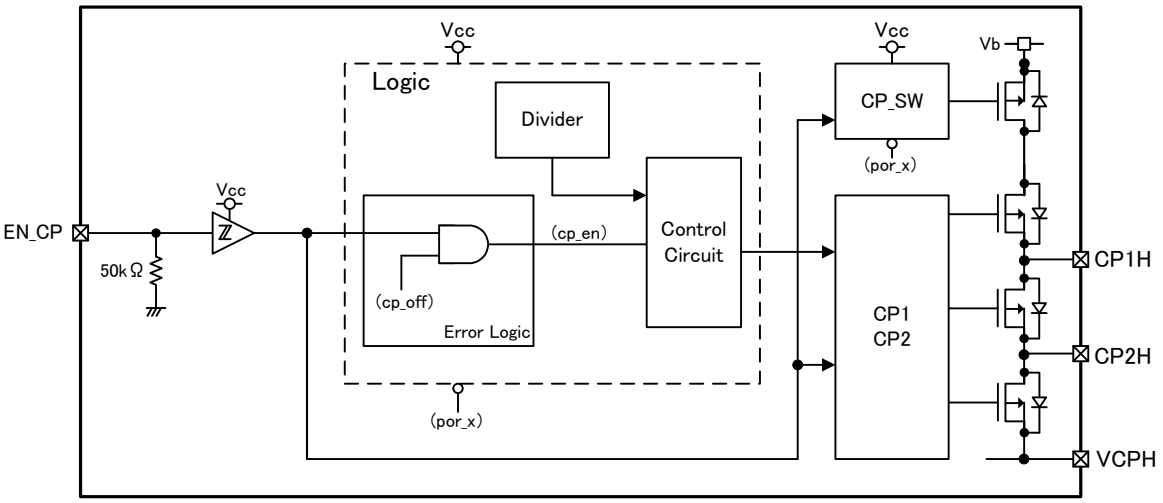


Fig.7-a EN_CP input circuit Block Diagram

Table 7-a Charge-pump-circuit control truth table

Input signal	Internal input signal		Internal control signal	Charge pump circuit	Charge pump SW circuit
EN_CP	(por_x)	(cp_off)	(cp_en)		
L	*	*	L	Disable	Disable
H	L	*	L	Disable	Disable
H	H	L	L	Disable	Enable
H	H	H	H	Enable	Enable

(Note) "*":Don't care

(8) ABIST function

At the time of IC starting, it is diagnosed whether miscellaneous abnormal detection is functioning normally.
At the time of IC starting, a divider starts operation after VCC1/VCC2 under voltage release, and it starts diagnosis of ABIST after LBIST completion. Diagnosis of ABIST is performed even when a judgment of LBIST is NG.
At the time of ABIST starting, the input voltage of the comparator is changed by the switch for diagnosis, and each detection comparator is reversed. Then, the diagnosis is performed. Diagnosis is performed in order synchronizing with a clock (clk16k), and diagnostic information is input to the ABIST judgment circuit. Also, NDIAG=L is kept during the diagnosis.
After completion of all diagnosis, the IC switches to the normal operation. When the abnormal detection is not diagnosed, NDIAG will be H. When the abnormal detection is diagnosed, NDIAG will be L and keep the diagnosis information.
A diagnostic part is as follows.
VCC1/VCC2 over voltage detection, VCPH clamp voltage detection, over temperature detection, and frequency abnormal detection (low frequency side)

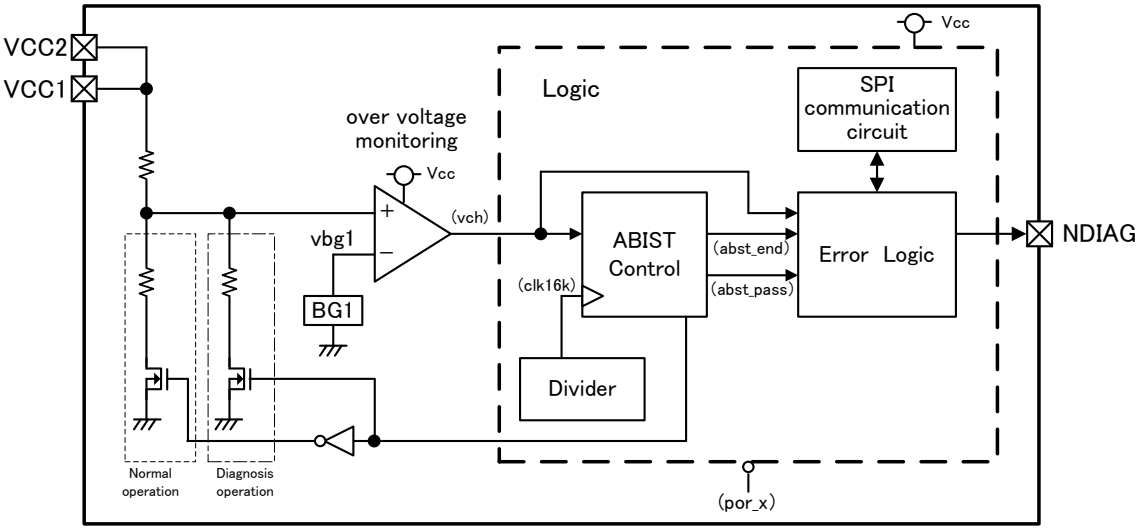


Fig.8-a ABIST Block Diagram (VCC1/VCC2 over voltage detection)

Table 8-a Circuit operation truth table (CP_SW circuit)

Input signal	CP_SW circuit			
EN_CP	Before ABIST	During ABIST	ABIST OK	ABIST NG
L	Disable	**Enable**	Disable	Disable
H	**Enable**	**Enable**	**Enable**	**Enable**

Table 8-b Circuit operation truth table (charge pump circuit)

Input signal	Charge pump circuit			
EN_CP	Before ABIST	During ABIST	ABIST OK	ABIST NG
L	Disable	Disable	Disable	Disable
H	Disable	Disable	**Enable**	Disable

Table 8-c Circuit operation truth table (pre-driver circuit)

Input signal		Pre-diver circuit			
ALARM1	ALARM2	Before ABIST	During ABIST	ABIST OK	ABIST NG
L	*	Disable	Disable	Disable	Disable
*	L	Disable	Disable	Disable	Disable
H	H	Disable	Disable	**Enable**	Disable

(Note)"*": Don't care

<ABIST whole operation / startup operation>

➢ H-(1) IC startup

At the time of IC starting, the divider is started the operation by the release of Vcc under voltage.

➢ H-(2) LBIST running

The divider starts the operation and starts the LBIST.

➢ H-(3) ABIST start up

The ABIST is started after the LBIST.

The detection comparator is changed every 2clk of clk16k, and diagnosed whether the detection comparator is outputting the failure detection signal correctly.

The comparator for an over temperature detection is diagnosed to the beginning.

➢ H-(4) Diagnosis

Each comparator is diagnosed as follows.

VCC1/VCC2 over voltage, VCPH cramp voltage, and a frequency monitoring (low frequency)

➢ H-(5) ABIST completion

When all detection comparator diagnosis is completed, the IC switches to the normal operation mode, and the charge pump circuit starts the operation. Then the pre-driver can be ON.

Also, the diagnosis result is output to the NDIAG.

In the case of the diagnosis NG, the charge pump circuit and the pre-driver circuit are kept OFF.

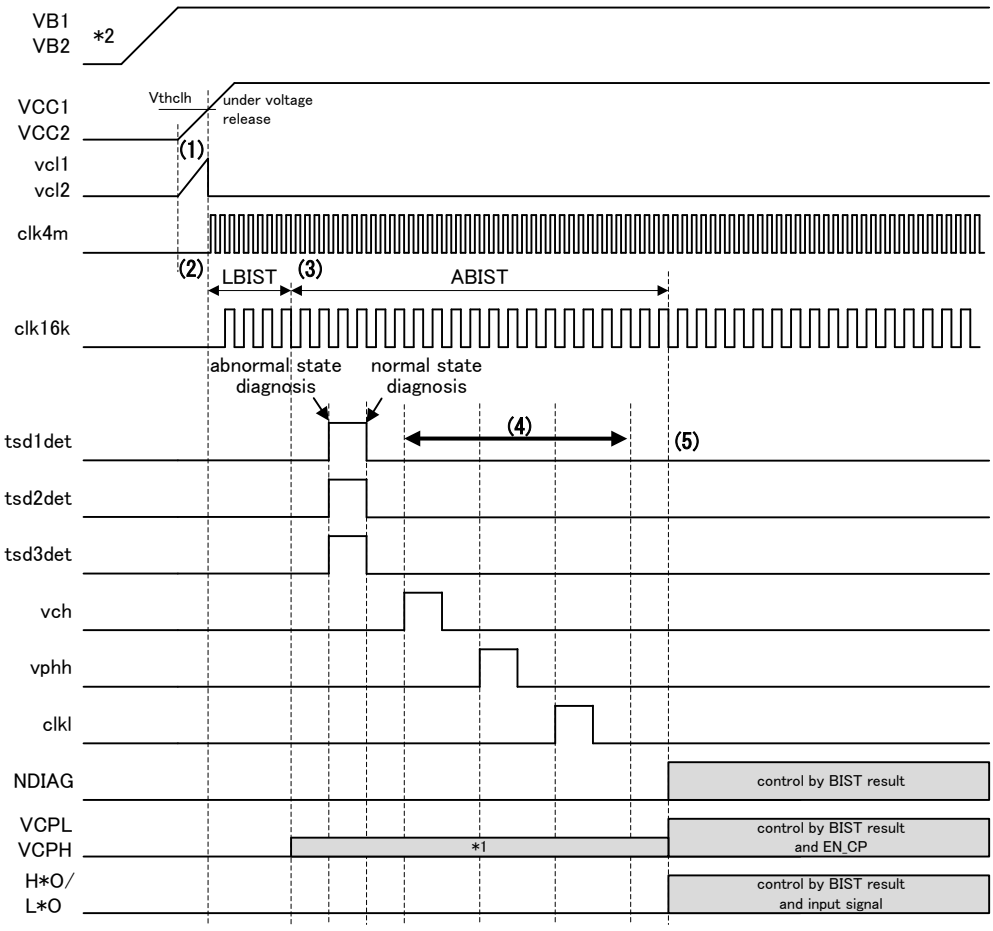


Fig.8-b ABIST timing chart

*1 Regardless of EN_CP input signals, Vcph is equal to Vcpl=Vb-3VF (Vcpl<=16V) during running the ABIST.

*2 There is no start order of VB1/2, and VCC1/2.
The slew rate of Vb and Vcc should be use in the following range.
Less than Vb=8V/μs
Less than Vcc=0.3V/μs

*3 When an abnormal detection of vphh is diagnosed, if Vb is lower than Vcc, maximum 10μA current flows in the cycle of 2clk of clk16k (125μs).

*4 The running time of LBIST and ABIST is about 2.4ms (typ.).

(9) SPI Communication circuit

The SPI communication circuit consists of an SPI core circuit and a register read circuit block.
Only when /CS is L, communication with a microcomputer is attained. A microcomputer writes data in SDIN at the rising edge of a clock, and IC reads data at the following falling edges. Moreover, IC writes data in SDOUT at the rising edge of a clock, and a microcomputer reads data at the following falling edges. SDIN receives the data bit from a microcomputer in order from MSB to LSB. SDOUT transmits a data bit to a microcomputer in order from MSB to LSB. An output is push-pull composition and will be a Hi-Z at the time of /CS="H". Moreover, inside IC, the /CS terminal have pull-up by resistance, and the SDIN and SCK terminal have pull-down by resistance.

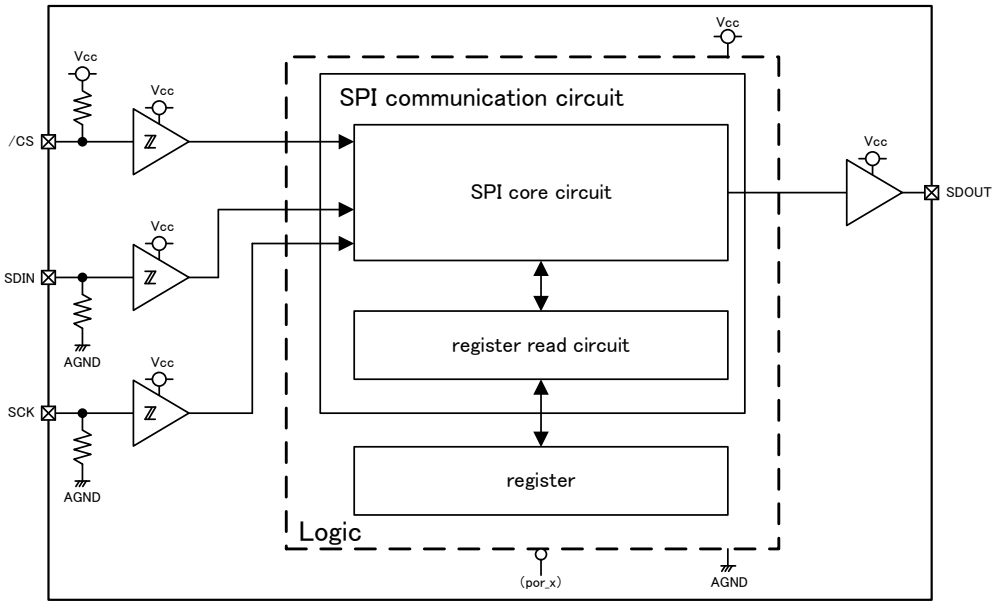


Fig.9-a SPI Communication circuit Block Diagram

(9-1) SPI Communication operation

When /CS is L, the serial data are transmitted or received synchronizing with the SCK. When /CS is H, the SDOUT output will be a high impedance. The data length is 40 bits. As a function, there are two kinds, the read operation and the write operation, and the write / read operation can be selected with "RW" bit. ”Dummy” bit does not influence the operations.

<Write operation>

The data structure of the write operation is shown in Fig.9-b.
SDIN is consist of ”RW” bit, ”Address” bit, ”Dummy” bit (2 bits), ”Data” bit, ”CRC” bit, and ”Dummy” bit (16bits). ”RW” bit is the bit to select the write or the read operation, and when ”RW” bit=’1,’ the write operation is selected. ”Address” bit is the bit to specify the address, and ”Data” bit is the write data bit. Data of ”Data” bit is written to "Address" bit. ”CRC” bit is calculated by the micro controller, according to 16 bits of ”RW” bit, ”Address” bit, ”Dummy” bit (2bits), and “Data” bit.
SDOUT is all ”Dummy” bit.
In addition, perform the read operation after writing and confirm the correct data are written.
Even if data are written to the empty bits, the data are not written.

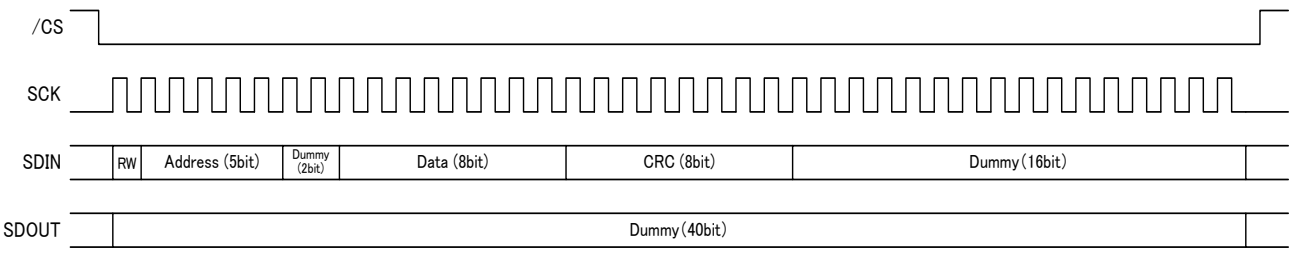


Fig.9-b Data structure of write operation

<Read operation>

The data structure of the read operation is shown in Fig.9-c.
SDIN is consist of ”RW” bit, ”Address” bit, ”Dummy” bit (10 bits), ”CRC” bit and ”Dummy” bit (16 bits). ”RW” bit is the bit to select the write or the read operation, and at when ”RW” bit=’0’, the read operation is selected. ”Address” bit is the bit to specify the address, and the data are read from the address of ”Address” bit. ”CRC” bit is calculated by the micro controller, according to 16 bits of ”RW” bit, ”Address ”bit, and ”Dummy” bit (10 bits).
SDOUT is consist of ”Dummy” bit (8 bits), ”Data” bit, ”Dummy” bit (16 bits), and ”CRC” bit. The data read from the address of ”Address” bit of the SDIN is output to ”Data” bit. "CRC" bit outputs the value which is calculated from 8 bits of "Data" bit by the IC.

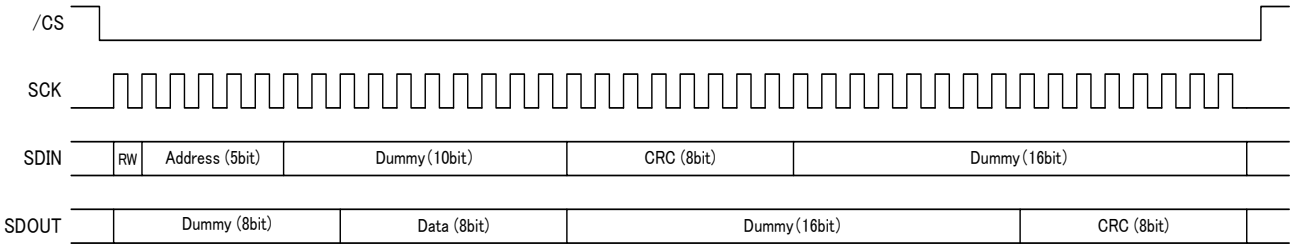


Fig.9-c Data structure of read operation

<CRC error judgment>

An error judgment is performed by the CRC to confirm the data communication correctly.
The generation polynomial used for the calculation is the following.

$$x^8+x^4+x^3+x^2+1$$

In the case of CRC error, the operation is the following.

(1) In the case of write operation

The write data are not written to the IC.

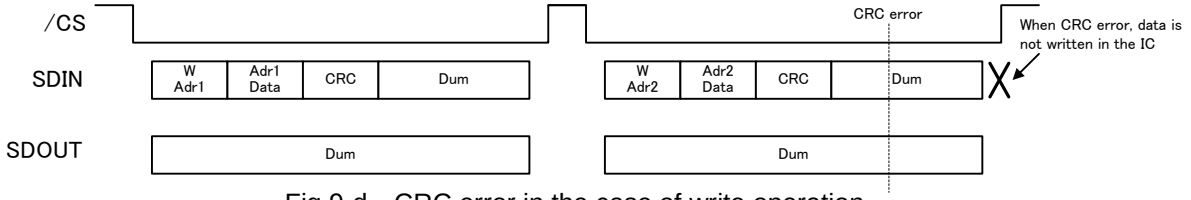


Fig.9-d CRC error in the case of write operation

(2)In the case of read operation

Incorrect data are written to the CRC bit of the SCOUT in the same frame.
Then the micro controller detects a CRC error.

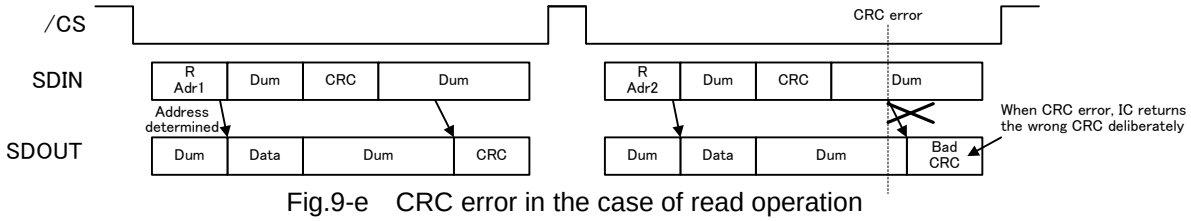


Fig.9-e CRC error in the case of read operation

<In the case of Vcc under voltage detection>

The SPI communication cannot perform when Vcc under voltage is detected.
And then, the SDOUT is fixed to 'L' (at the write and the read operation).

<Fail judgment>

In the following cases at the SPI communication, the IC judges it as a communication error, and 1 is written to err_spi which is the register of the SPI communication error.
(1) Access to the address which has no register
(2) When data length is except 40 bits

(9-2) SPI Register Map

Table 9-2a config 1 (Address : 0x01)

bit	7	6	5	4	3	2	1	0
Symbol	df_alm1		df_alm2		sh_op			-
DEFAULT	1	1	1	1	0	1	0	0

bit	Symbol	R/W	Function
7:6	df_alm1	R/W	setting of ALARM1 Digital Filtering Time (H-side/L-side) (Fc=4MHz typ.) "00" = (16x2^2/Fc) + (1/Fc) "01" = (1000x2^2/Fc) + (1/Fc) "10" = (2000x2^2/Fc) + (1/Fc) "11" = (4000x2^2/Fc) + (1/Fc)
5:4	df_alm2	R/W	setting of ALARM2 Digital Filtering Time (H-side/L-side) (Fc=4MHz(typ.) "00" = (16x2^2/Fc) + (1/Fc) "01" = (1000x2^2/Fc) + (1/Fc) "10" = (2000x2^2/Fc) + (1/Fc) "11" = (4000x2^2/Fc) + (1/Fc)
3:1	sh_op	R/W	Response of Short circuit Detection "000" = NDIAG:L (Hold) "001" = NDIAG:L (Hold), Detected Phase Pre-Driver OFF (During detection) "010" = NDIAG:L (Hold), Detected Phase Pre-Driver OFF(Hold) "011" = NDIAG:L (hold), All (eleven) Pre-Driver OFF (During detection) "100" = NDIAG:L (Hold), All (eleven) Pre-Driver OFF (Hold) "101" = NDIAG:L (Hold), All (eleven) Pre-Driver and Charge Pump OFF (During detection) "110" = NDIAG:L (Hold), All (eleven) Pre-Driver and Charge Pump OFF (Hold) "111" = Detection disable

Table 9-2b config2 (Address : 0x02)

bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	ovc_op		tsd_op		pl_op
DEFAULT	0	0	0	0	1	1	0	0

bit	Symbol	R/W	Function
4:3	ovc_op	R/W	Response of VCC1/VCC2 Over Voltage Detection "00" = NDIAG:output "L" (Hold) "01" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver OFF "10" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF (During detection) "11" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF (Hold)
2:1	tsd_op	R/W	Response of Over Temperature Detection "00" = NDIAG:output "L" (Hold) "01" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver OFF (During detection) "10" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF (During detection) "11" = NDIAG:output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF (Hold)
0	pl_op	R/W	Response of Prohibit Pre-Driver Output setting Detection "0" = NDAIG:no outpu , During Prohibit input, Detected Phase Pre-Driver OFF "1" = NDIAG:output "L" (Hold), During Prohibit input, Detected Phase Pre-Driver OFF

Prohibit Pre-Driver Output Setting

: In case that High-side and Low-side Input of the same Phase are “H”, the both High-side and Low-side Output are forced to be “L”

(Input) HUI=LUI=”H” → HUO=LUO=”L”
HVI=LVI=”H” → HVO=LVO=”L”
HWI=LWI=”H” → HWO=LWO=“L”

Table 9-2c config3 (Address : 0x03)

bit	7	6	5	4	3	2	1	0
Symbol	uvb_op		co_sel		ferr_op			-
DEFAULT	0	1	0	0	1	0	0	0

bit	Symbol	R/W	Function
7:6	uvb_op	R/W	Response of VB1/VB2 Low Voltage Detection "00" = NDIAG: output "L" (Hold), All (eleven) Pre-Driver OFF (During detection) "01" = NDIAG: output "L", All (eleven) Pre-Driver OFF (During detection) "1*" = NDIAG: output "H", All (eleven) Pre-Driver OFF (During detection)
5:4	co_sel	R/W	setting Monitoring Output Signal of "CLKOUT" "00" = output "L" "01" = clk4m 4MHz (typ.) "10" = clk500k 500kHz(typ.) "11" = clk16k 16kHz(typ.)
3:1	ferr_op	R/W	Response of Internal OSC Over/Low Frequency Detectioin 000 = NDIAG: output "L" (Hold) 001 = NDIAG: output "L" (Hold), All (eleven) Pre-Driver OFF (During detection) 010 = NDIAG: output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF(During detection) 011 = NDIAG: output "L" (Hold), All (eleven) Pre-Driver and Charge Pump OFF (Hold) 1** = nop

* : don't care

Table 9-2d config4 (Address : 0x04)

bit	7	6	5	4	3	2	1	0
Symbol	-	df_sh			vthh_sh		vthl_sh	
DEFAULT	0	0	0	1	0	0	0	1

bit	Symbol	R/W	Function
6:4	df_sh	R/W	setting Digital Filtering Time of Short Circuit Detection (typ. at 4MHz) "000" = 6µs "001" = 8µs "010" = 10µs "011" = 12µs "1**" = no Filtering
3:2	vthh_sh	R/W	setting Threshold Voltage of Short Circuit Detection (Hi-side) "00" = 0.5V "01" = 0.75V "10" = 1.0V "11" = 1.25V
1:0	vthl_sh	R/W	setting Threshold Voltage of Short Circuit Detection (Lo-side) "00" = 0.5V "01" = 0.75V "10" = 1.0V "11" = 1.25V

* : don't care

Table 9-2e config5 (Address : 0x05)

bit	7	6	5	4	3	2	1	0
Symbol	rebst	diag_dg	shuh_dg	shul_dg	shvh_dg	shvl_dg	shwh_dg	shwl_dg
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
7	rebst	R/W	BIST restart request by SPI Command "0": nop "1": restart BIST
6	diag_dg	R/W	NDIAG Diagnosis Check by SPI Command "0": nop (NDIAG normal Operation) "1": Forced output "L" from PIN"NDIAG"
5	shuh_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（U-Phase Lo-side） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")
4	shul_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（U-Phase Hi-side） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")
3	shvh_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（V-Phase Lo-side)） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")
2	shvl_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（V-Phase Hi-side） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")
1	shwh_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（W-Phase Lo-side） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")
0	shwl_dg	R/W	Short Circuit Detection Diagnosis Check by SPI Command（W-Phase Hi-side)） "0": nop (Short Detection Norma Operation) "1": Forced Short Circuit Detection (output "L" from PIN"NDIAG")

- BIST restart by SPI Reg. “rebst” is enable when LBIST or ABIST is failure. In normal operation and LBIST/ABIST passed, the Write ”rebst”=1 is ignored and do not restart BIST.
- Forced Short Circuit Detection:
  - Output “L” from PIN ”NDIAG”
  - each detected Phase Pre-Driver OFF according to the setting by SPI Reg. “sh_op”(address 0x01 bit1-3)
  - Charge Pump OFF according to the setting by SPI Reg. “sh_op”(config1)
- To write “0” into the SPI Reg. ”sh**_dg”, the above detection response are reset and return to normal operation.
- In case of SPI Reg. “sh_op”=”111”(config1), the above Short Circuit Detection Diagnosis does not performed, even write “1” into the above each Short Circuit Detection Diagnosis register.

Table 9-2f config6 (Address : 0x06)

bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	t_ilim	
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
1:0	t_ilim	R/W	seting time of Current Limit disable after Turn On/Off (typ. at 4MHz) "00" = 8µs "01" = 16µs "10" = 32µs "11" = Always Current Limit enable

The Current Limit is available for each Output of Pre-driver (HUO,HVO,HWO,LUO,LVO,LWO) (refer “Electrical characteristics”). These Current Limit are disabled the above period which is set by SPI Reg. “t_ilim”. For example, when ”t_ilim” is set “00”, during 8µs(typ.) after Turn On/Turn Off, there is no Current Limit and after 8µs(typ.) passed, the Current Limit which is shown in the spec. is enable.

Current Limit of Turn On : Io_lmth = 1mA (typ.)
Current Limit of Turn Off : Io_lmtl = 10mA (typ.)

Table 9-2g status1 (Address : 0x07)

bit	7	6	5	4	3	2	1	0
NAME	uvb	–	ovc	–	–	–	–	–
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
7	uvb	R/W	VB1/VB2 Low Voltage Detection Flag "0" = Normal "1" = Detected Low Volateg of VB1/VB2
5	ovc	R/W	VCC1/VCC2 Over Volatge Detection Flage "0" = Normal "1" = Detected Over Volateg of VB1/VB2

- When the above each SPI Reg. is written “1” after return to normal condition, each detection Flag is reset and the SPI Reg. are "0" (Default). In this case, Output NDAIG=High, return to normal operation. “0” write into these SPI Reg. is ignored.
  When abnormal condition is kept, the write “1” is ignored and keep detection response.

Table 9-2h status2 (Address : 0x08)

bit	7	6	5	4	3	2	1	0
Symbol	-	-	tsd1det	tsd2det	tsd3det	-	-	-
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
5	tsd1det	R/W	Over Temperature Detection1 "0" = Mormal "1" = detected Over Temperature1
4	tsd2det	R/W	Over Temperature Detection2 "0" = Normal ″1″ = detected Over Temperature2
3	tsd3det	R/W	Over Temperature Detection3 "0" = Normal "1" = Over Temperature Detection3

- When the above each SPI Reg. is written “1” after return to normal condition, each detection Flag is reset and the SPI Reg. are "0" (Default). In this case, Output NDAIG=High, return to normal operation. “0” write into these SPI Reg. is ignored.
  When abnormal condition is kept, the write “1” is ignored and keep detection response.

Table 9-2i status3 (Address : 0x09)

bit	7	6	5	4	3	2	1	0
Symbol	-	-	scuh	scvh	scwh	scul	scvl	scwl
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
5	scuh	R/W	Short Detection of external MOSFET（UPhase, GND Short） "0" = Normal "1" = Detected Short Circuit
4	scvh	R/W	Short Detection of external MOSFET（VPhase, GND Short） "0" = Normal "1" = Detected Short Circuit
3	scwh	R/W	Short Detection of external MOSFET（WPhase, GND Short） "0" = Normal "1" = Detected Short Circuit
2	scul	R/W	Short Detection of external MOSFET（UPhase, VB Short） "0" = Normal "1" = Detected Short Circuit
1	scvl	R/W	Short Detection of external MOSFET（VPhase, VB Short） "0" = Normal "1" = Detected Short Circuit
0	scwl	R/W	Short Detection of external MOSFET（WPhase, VB Short） "0" = Normal "1" = Detected Short Circuit

- When the above each SPI Reg. is written “1” after return to normal condition, each detection Flag is reset and the SPI Reg. are "0" (Default). In this case, Output NDAIG=High, return to normal operation. “0” write into these SPI Reg. is ignored.
  When abnormal condition is kept, the write “1” is ignored and keep detection response.

Table 9-2j status4 (Address : 0x0A)

bit	7	6	5	4	3	2	1	0
Symbol	err_of	err_uf	err_plu	err_plv	err_plw	err_spi	-	-
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	FUNCTION
7	err_of	R/W	setting of Internal OSC Over Frequency Detection "0" = Normal "1" = Detected Over Frequency of internal OSC
6	err_uf	R/W	setting of Internal OSC low Frequency Detection "0" = Normal "1" = Detected Low Frequency of internal OSC
5	err_plu	R/W	setting of Prohibit U-Phase Pre-Driver Output setting Detection "0" = Normal "1" = Detected Prohibit setting of U-Phase
4	err_plv	R/W	setting of Prohibit V-Phase Pre-Driver Output setting Detection "0" = Normal "1" = Deteced Prohibit setting of V-Phase
3	err_plw	R/W	setting of Prohibit W-Phase Pre-Driver Output setting Detection "0" = Normal "1" = Detected Prohibit setting of W-Phase
2	err_spi	R/W	setting of SPI Transmission Failure Detection "0" = Normal "1" = Detected SPI Transmission Failure

- When the above each SPI Reg. is written “1” after return to normal condition, each detection Flag is reset and the SPI Reg. are "0" (Default). In this case, Output NDAIG=High, return to normal operation. “0” write into these SPI Reg. is ignored.
  When abnormal condition is kept, the write “1” is ignored and keep detection response.

Table 9-2k status5 (Address : 0x0B)

bit	7	6	5	4	3	2	1	0
Symbol	abst_judge				abst_pass	lbst_pass	abst_end	lbst_end
DEFAULT	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
7:4	abst_judge	R	ABIST counter value "0***" = ABIST error "11**" = ABIST error "101*" = ABIST error "1001" = ABIST error "1000" = No error
3	abst_pass	R	ABIST Result Flag "0" = Result ”Failure” "1" = Result”PASS”
2	lbst_pass	R	LBIST Result Flag "0" = Result "Failure" "1" = Result”PASS”
1	abst_end	R	ABIST Finish Flag "0" =Irregular ABIST stop "1" = Finish
0	lbst_end	R	LBIST Finish Flag "0" = Irregular LBIST stop "1" = Finish

When ABIST/LBIST is finished, SPI Reg.”abst_end” / ”lbst_end” is “1”. When ABIST/LBIST cannot be finished abnormally, SPI Reg. ”abst_end” / ”lbst_end” is “0”.
After finish ABIST/LBIST normally and that result is passed, SPI Reg. ”abst_pass” / ”lbst_pass” is “1”. When ABIST/LBIST result is failure, SPI Reg. ”abst_pass” / ”lbst_pass” is “0”.

Absolute maximum ratings (Ta = 25°C)

Unless otherwise specified, all voltage is the AGND standard voltage

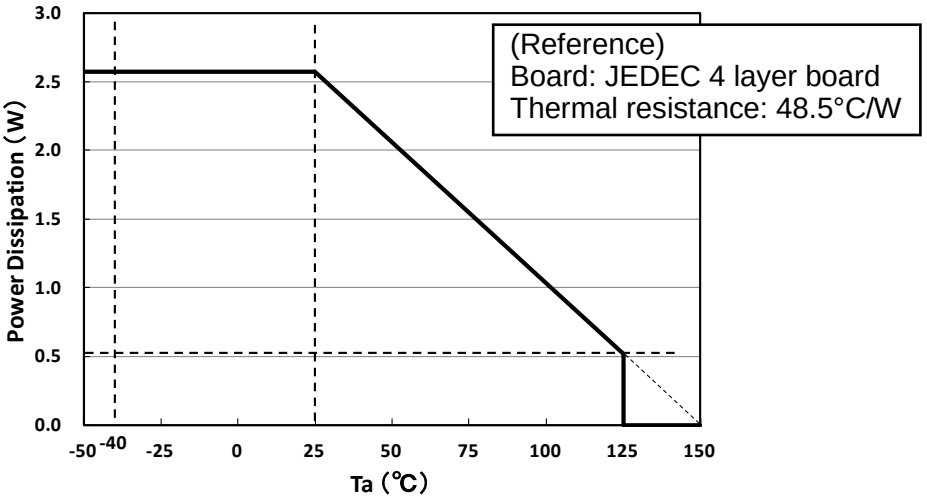
Item	Symbol	Pin	Rate	Unit	Condition
Supply voltage	Vb	VB1,VB2	-0.3 to +28(DC) +28 to +40(≤1s)	V	-
	Vcpl	VCPL	-0.3 to +20	V	-
	Vcph	VCPH	-0.3 to +40	V	-
	Vcc	VCC1,VCC2	-0.3 to +6	V	-
	Vccop	VCC_OP	-0.3 to +6	V	-
Voltage between AGND and PGND terminals	Vgnd	AGND1,AGND2, PGND1,PGND2,PGND3	-0.3 to +0.3	V	AGND: AGND1,2 PGND: PGND1,2,3
Input voltage	Vin1	LUI, LVI, LWI, HUI, HVI, HWI, BR1I, BR2I, RUI, RVI, RWI, SCK, /CS, SDIN, ALARM1, ALARM2, EN_CP, TEST AMP1P, AMP1N, AMP2P, AMP2N, AMP3P, AMP3N,VRI	-0.3 to Vcc +0.3	V	Vin1≤6V
	Vin2	HS, SHU, SHV, SHW	-0.3 to Vcph +0.3	V	Vin2≤40V
	Vin3	BR1O, BR2O	-18 to 0	V	AGND1,2=PGND1,2,3=0V Terminals other than the above are open.
Output voltage	Vout1	CP1H, CP2H, HUO, HVO,HWO, BR1O, BR2O, RUO, RVO, RWO	-0.3 to Vcph +0.3	V	Vout1≤40V
	Vout2	CP1L, CP2L	-0.3 to Vb +0.3	V	Vout2≤28V(DC) Vout2≤40V(≤1s)
	Vout3	LUO, LVO, LWO	-0.3 to Vcpl +0.3	V	Vout3≤20V
	Vout4	AMP1O, AMP2O, AMP3O, VRO	-0.3 to Vccop +0.3	V	Vout4≤6V
	Vout5	NDIAG, CLKOUT, SDOUT	-0.3 to Vcc +0.3	V	Vout5≤6V
Input current	Iin1	SHU, SHV, SHW,	(-10)	mA	External resistance :1kΩ Time ≤ 5μs The numerical value in a parenthesis means a design value.
	Iin2	AMP1P, AMP1N, AMP2P, AMP2N, AMP3P, AMP3N	±5	mA	-
Output current	Iout1	HUO, HVO,HWO, LUO, LVO, LWO	-5 to 20	mA	-
	Iout2		±1	A	Time shorter than output current switching time(Tsw) PWM period: 50μs
	Iout3	AMP1O, AMP2O, AMP3O,VRO	±5	mA	-
	Iout4	NDIAG, CLKOUT, SDOUT	±10	mA	-
Operating ambient temperature	Ta	-	-40 to 125	°C	-
Storage temperature	Tstg	-	-55 to 150	°C	-

Power dissipation	PD	-	515	mW	JEDEC 4 layer board, Ta=125°C, Thermal resistance 48.5°C/W

* The numerical value in a parenthesis means a design value. The shipment test is not performed.

<<User notes>>

*Absolute maximum ratings represent the values which cannot be exceeded for any length of time.
*The sink current to this IC is shown with '+', the sink current from this IC is shown with "-."
*The value of absolute maximum ratings is limited by the range of condition column.
*The symbols (Vb, Vcpl, Vcph, Vcc, and Vccop) shown in the above maximum ratings table mean the supply voltage and output voltage in each terminal (VB1/2, VCPL, VCPH, VCC1/2, and VCC_OP).
*Use the through rate of Vb and Vcc in the following range.
less than Vb=8V/μs, less than Vcc=0.3V/μs
*This product is intended for use with a 12 V battery.



Power dissipation curve

Electrical characteristics

Operating voltage range

Item	Applied terminal	Symbol	Rating	Unit	Condition
Input voltage	VB1,VB2	Vb	4.5 to 28	V	DC
	VCC1,VCC2	Vcc	3.0 to 5.5	V	DC
	VCC_OP	Vccop	3.0 to 5.5	V	DC

* This product is intended for use with a 12 V battery.

Current consumption

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Vccop=3 to 5.5V, Ta=-40 to 125°C

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit
stand-by current (Vb)	VB1,VB2	Ib1	Vb=12V ,Vcc=Vccop=0V	-	0.01	2.0	μA
Current consumption (Vb)	VB1,VB2	Ib2	Vb=13.5V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Cload=10000pF, Rload=33Ω	-	100	200	mA
		Ib3	Vb=17V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Cload=10000pF, Rload=33Ω	-	120	250	mA
		Ib4	Vb=28V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Cload=10000pF, Rload=33Ω	-	200	300	mA
Current consumption (Vcc)	VCC1,VCC2	Icc1	Vcc=5V	4.0	6.5	10.0	mA
		Icc2	Vcc=3.3V	3.0	5.5	9.0	mA
Current consumption (Vccop)	VCC_OP	Iccop1	Vccop=5V	3.0	6.5	11.0	mA
		Iccop2	Vccop=3.3V	3.0	5.5	9.0	mA

* Ib1, Ib2, Ib3, Ib4 is the current obtained by summing the current of VB1 and VB2.
* Icc1, Icc2 is the current obtained by summing the current of VCC1 and VCC2.
* When Vcc is lowered, IC will be the stand-by state. Current in the stand-by state has been defined by the Ib1.
* The external constant of charge pump in Ib2, Ib3, Ib4 is the constant of the reference circuit example.

Charge pump circuit

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Output voltage	VCPL	Vcpl	Vb=4.5 to 5.5V (Output load=1.5kΩ)	Vb+4	-	-	V	-
			Vb=5.5 to 7V (Output load=1.5kΩ)	Vb+6	-	-	V	-
			Vb=7 to 28V (Output load=1.5kΩ)	Vb+8 (Vcplcl)	-	-	V	-
	VCPH	Vcph	Vb=4.5 to 5.5V (Output load=1.5kΩ)	Vb+4	-	-	V	-
			Vb=5.5 to 7V (Output load=1.5kΩ)	Vb+6	-	-	V	-
			Vb=7 to 8V (Output load=1.5kΩ)	Vb+8	-	-	V	-
			Vb=8 to 28V (Output load=1.5kΩ)	Vb+10 (Vcphcll)	Vb+12	Vb+14 (Vcphclh)	V	-
Clamp voltage	VCPL	Vcplcl	-	14	16	18	V	-
	VCPH	Vcphclh	-	34.5	37	40	V	-
		Vcphcll	-	34	36.5	39.5	V	-

* The following shows the reference values of the external capacitors and resistance of CP1H, CP1L, CP2H, CP2L, VCPH, and VCPL terminal;

Ccp = 0.1 [μF], Rcp = 15 [Ω], Cvcph1 = 10 [μF], Cvcph2 = 0.1 [μF], Cvcpl1 = 4.7 [μF], Cvcpl2 = 0.1 [μF]

The external circuit should be decided after certainly evaluating and confirming on the unit board supposing the usage environment.

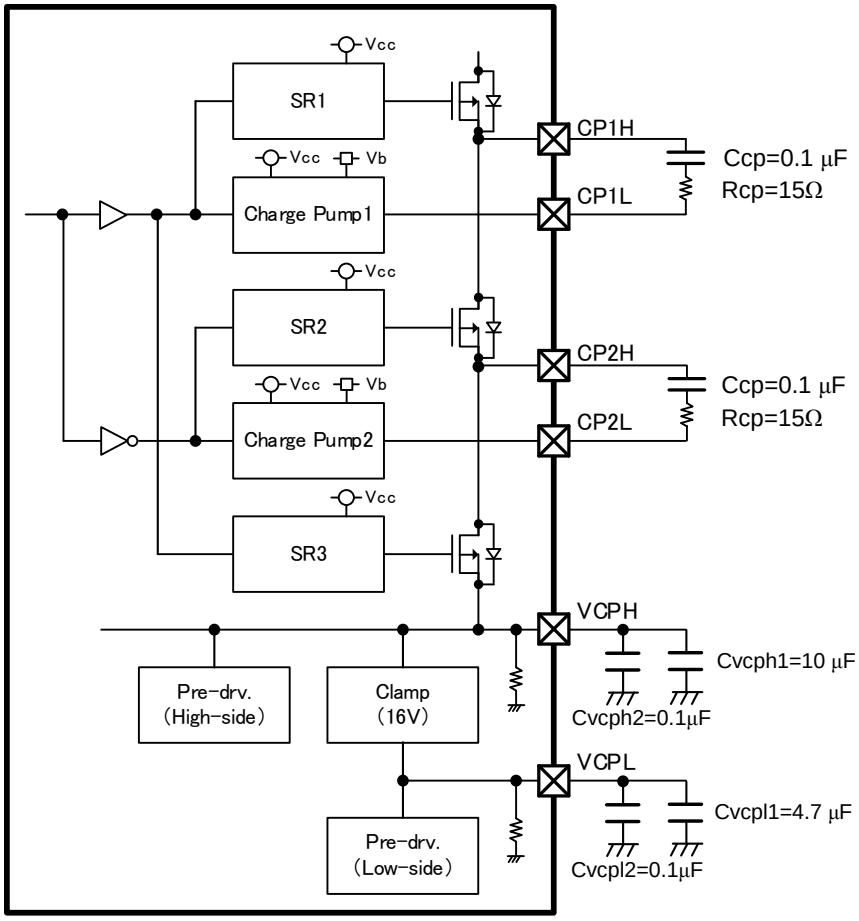


Fig.1-c Charge pump application circuit diagram

Pre-diver circuit

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
High level input current	HUI, HVI, HWI, LUI, LVI, LWI, RUI, RVI, RWI, BR1I, BR2I	Iih	Vcc= 5.0V, Vin = 5.0V	50	100	200	μA	-
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	μA	-
High level input detection voltage	HUI, HVI, HWI, LUI, LVI, LWI, RUI, RVI, RWI, BR1I, BR2I	Vih	-	0.75× Vcc	-	-	V	-
Low level input detection voltage		Vil		-	-	0.25× Vcc	V	-
Output voltage 1	HUO,HVO,HWO	Voh1	Iload=-100μA	Vcph-0.1	-	Vcph	V	-
		Vol1	Iload=100μA	-	-	0.5	V	-
Output voltage 2	LUO,LVO,LWO	Voh2	Iload=-100μA	Vcpl-0.1	-	Vcpl	V	-
		Vol2	Iload=100μA	-	-	0.5	V	-
Output voltage 3	BR1O,BR2O	Voh3	Iload=-100μA	Vcph-0.2	-	Vcph	V	-
		Vol3	Iload=10μA	-	-	0.9	V	-
Output voltage 4	RUO,RVO,RWO	Voh4	Iload=-100μA	Vcph-0.2	-	Vcph	V	-
		Vol4	Iload=100μA	-	-	0.5	V	-
Output resistance1	HUO,HVO,HWO	Rohh	HUI,HVI,HWI = 5.0V Iload=-50mA	1.0	2.5	6.0	Ω	Before passing Tsw
		Rohl	HUI,HVI,HWI = 0V Iload=50mA	0.3	1.0	3.0	Ω	Before passing Tsw
Output resistance2	LUO,LVO,LWO	Rolh	LUI,LVI,LWI = 5.0V Iload=-50mA	1.0	2.5	6.0	Ω	Before passing Tsw
		Roll	LUI,LVI,LWI = 0V Iload=50mA	0.3	1.0	3.0	Ω	Before passing Tsw
Output resistance3	RUO,RVO,RWO	Rorh	RUI,RVI,RWI = 5.0V Iload=-5mA	0.8	1	1.2	kΩ	-
		Rorl	RUI,RVI,RWI = 0V Iload=5mA	0.8	1	1.2	kΩ	-
Output resistance4	BR1O,BR2O	Robh	BR1I,BR2I = 5.0V Iload=-5mA	0.8	1	1.2	kΩ	-
		Robl	BR1I,BR2I = 0V Robl=Vd/4mA	0.8	1	1.2	kΩ	Refer to Fig.2-e.
Leakage current at the time of VB reverse connection	BR1O,BR2O	Iol	BR1O,BR2O =-18V, PGND1,2,3=0V	0	0.01	1.0	μA	-

* For the motor relay output, RUO, RVO, and RWO, connect the external series resistance more than 10 kΩ.

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Output limit current	HUO,HVO,HWO LUO,LVO,LWO	Io_lmth	When turning on After passing Tsw	-1.4	-1	-0.6	mA	Refer to Fig.2-d.
		Io_lmtl	When turning off After passing Tsw	6	10	14	mA	Refer to Fig.2-d.
Output current switching time	HUO,HVO,HWO LUO,LVO,LWO	Tsw	-	5	8	14	μs	t_ilim = "00" Refer to Fig.2-d
			-	10	16	28	μs	t_ilim = "01" Refer to Fig.2-d
			-	20	32	56	μs	t_ilim = "10" Refer to Fig.2-d
Turn on input propagation delay time	HUI,HVI,HWI, HUO,HVO,HWO	Tdonh1	Ta=-40°C, VCC=3.0 to 3.5V, Rload=33Ω, Cload=10000pF	50	120	1200	ns	Refer to Fig.2-d.
		Tdonh2	Ta=25/125°C, VCC=3.0 to 3.5V, Rload=33Ω, Cload=10000pF	50	120	250	ns	Refer to Fig.2-d.
		Tdonh3	VCC=3.5 to 5.5V, Rload=33Ω, Cload=10000pF	50	120	250	ns	Refer to Fig.2-d.
	LUI,LVI,LWI, LUO,LVO,LWO	Tdonl1	Ta=-40°C, VCC=3.0 to 3.5V, Rload=33Ω, Cload=10000pF	50	120	1200	ns	Refer to Fig.2-d.
		Tdonl2	Ta=25/125°C, VCC=3.0 to 3.5V, Rload=33Ω, Cload=10000pF	50	120	250	ns	Refer to Fig.2-d.
		Tdonl3	VCC=3.5 to 5.5V, Rload=33Ω, Cload=10000pF	50	120	250	ns	Refer to Fig.2-d.
Turn off input propagation delay time	HUI,HVI,HWI, HUO,HVO,HWO	Tdoffh	Rload=33Ω, Cload=10000pF	100	180	300	ns	Refer to Fig.2-d.
	LUI,LVI,LWI, LUO,LVO,LWO	Tdoffl	Rload=33Ω, Cload=10000pF	100	180	300	ns	Refer to Fig.2-d.
Difference of input propagation delay time	HUI,HVI,HWI, LUI,LVI,LWI, HUO,HVO,HWO LUO,LVO,LWO	dTd1	Ta=-40°C, VCC=3.0 to 3.5V, Tdonh-Tdoffl, Tdonl-Tdoffh	-125	-	1150	ns	Difference between H or L side of the same phrases, U,V, and W
		dTd2	Ta=25/125°C, VCC=3.0 to 3.5V, Tdonh-Tdoffl, Tdonl-Tdoffh	-125	-	125	ns	Difference between H or L side of the same phrases, U,V, and W
		dTd3	VCC=3.5 to 5.5V, Tdonh-Tdoffl, Tdonl-Tdoffh	-125	-	125	ns	Difference between H or L side of the same phrases, U,V, and W

* For the measurement circuit, refer to Fig.2-b and Fig.2-c.

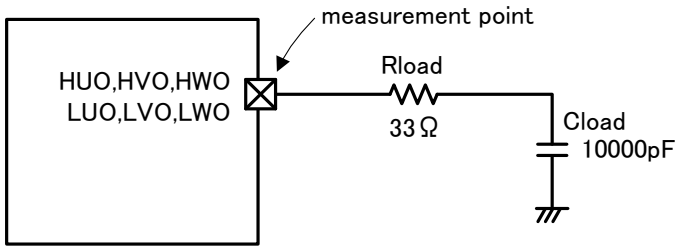


Fig.2-b Measurement circuit diagram (High side/Low side)

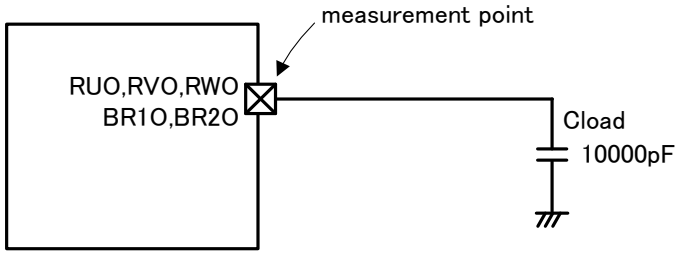


Fig.2-c Measurement circuit diagram (power supply relay/motor relay)

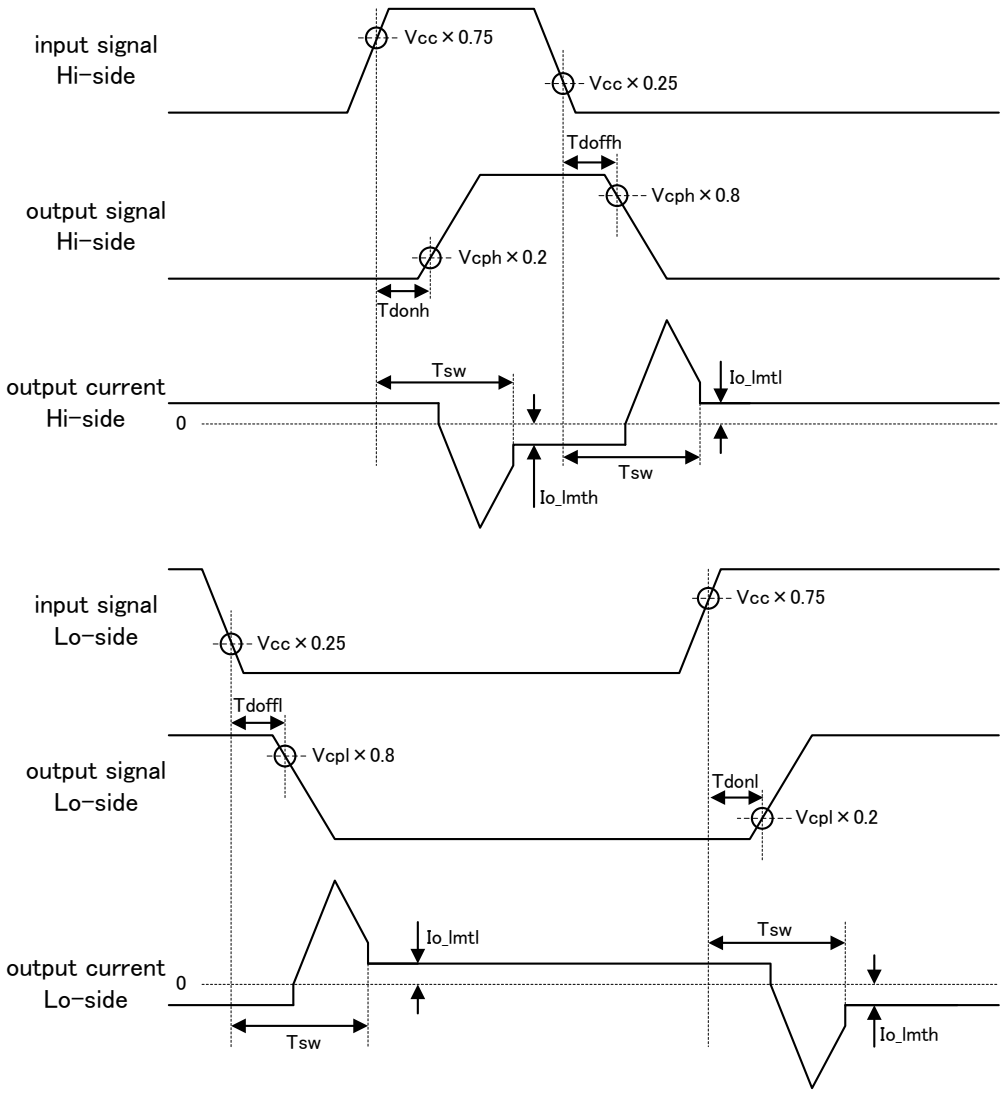


Fig.2-d Timing chart of output current switching time and input propagation delay time

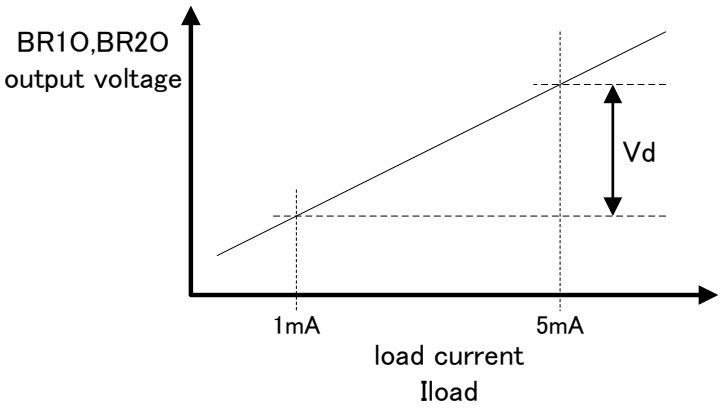


Fig.2-e Measurement method of BR1O and BR2O output resistance

Current detection circuit

Unless otherwise specified, Vb=4.5 to 28V, Vccop=3 to 5.5V, Ta=-40 to 125°C

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Input voltage range	VRI	Vin1	-	0.5	-	Vccop -1.4	V	-
Input offset voltage	VRI	Voff1	Vin1=0.5 to Vccop-1.4V	-7	-	7	mV	-
	AMP*P, AMP*M	Voff2	Gain=5, Vinr =-0.5V to 0.5V, VRO=Vccop/2, Iload = 0, and 1mA	-7	-	7	mV	-
Input offset voltage Temperature characteristic	AMP*P, AMP*M	VoffdT	Gain=5, Vinr =-0.5V to 0.5V, VRO=Vccop/2, Iload = 0, and 1mA	(-15)	-	(15)	μV/°C	The numerical value in a parenthesis means a design value.
Input bias current	VRI AMP*P, AMP*M	Iin	-	-1	-	1	μA	-
Output voltage	VRO	Vo	Iload = -2mA	0.5	-	Vccop -1.4	V	-
	AMP*O	Voh	Gain=5, Vinr=-0.1×Vccop, VRO=Vccop/2, Iload = -1mA	Vccop -0.3	-	Vccop	V	-
		Vol	Gain=5, Vinr=0.1×Vccop, VRO=Vccop/2, Iload = 1mA	0	-	0.3	V	-
Slew rate	AMP*O	SR1	Gain=5 Rload=1kΩ, Cload=100pF	10	20	40	V/μs	Refer to Fig.3-d.
		SR2		-40	-20	-10	V/μs	Refer to Fig.3-d.

* shows from 1 to 3

*The input resistance, R1 and R2 should be used in the range from 1.5 kΩ to 20kΩ, R3 should be used at 100 kΩ or less.

*The Gain should be used in the range from 5 to 30 times.

*The amplifier configuration should be used with the configuration shown in Fig.3-c.

* The numerical value in a parenthesis means a design value. The shipment test is not performed.

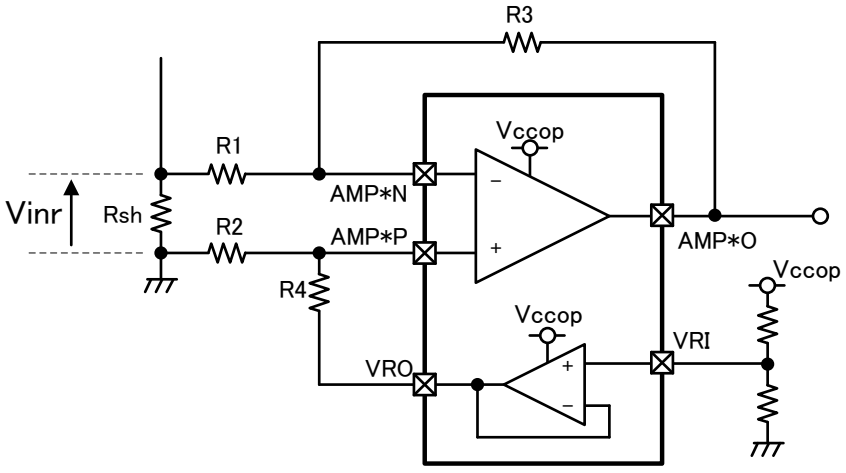


Fig.3-c Measurement circuit diagram

※SR1 = 0.6x(Vccop−0.3)/ΔTr
※SR2 = −0.6x(Vccop−0.3)/ΔTf

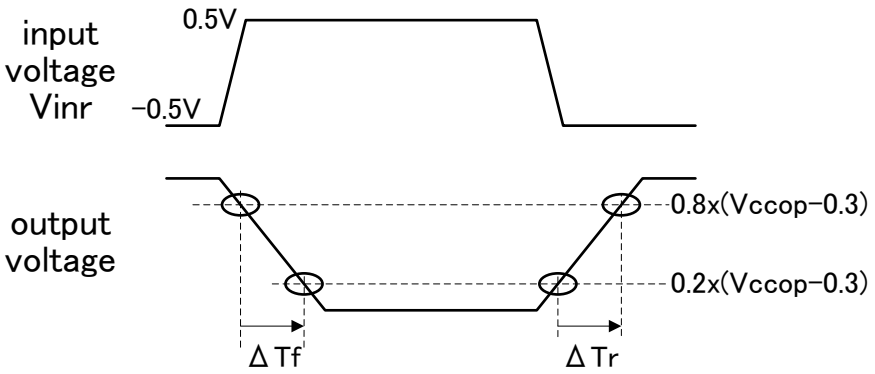


Fig.3-d Slew rate timing chart

Oscillator / Divider

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4 MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Internal oscillation frequency	-	Fc	-	2.6	4	5.4	MHz	-
Output voltage	CLKOUT	Voh	Ioh=-2mA	0.85×Vcc	-	-	V	-
		Vol	Iol=2mA	-	-	0.15×Vcc	V	-
Division output	CLKOUT	Fco	-	-	Fc	-	Hz	co_sel = “01” (clk4m)
				-	$Fc/2^3$	-		co_sel = “10” (clk500k)
				-	Fc/250	-		co_sel = “11” (clk16k)

* CLKOUT pin is connected to the internal resistance 100Ω (typ.).

Failure detection circuit

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4 MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Detection voltage of Vb under voltage	VB1,VB2	Vthblh	-	4.2	4.35	4.5	V	-
		Vthbll	-	3.9	4.05	4.2	V	-
		Vthblhys	-	0.2	0.3	0.4	V	-
Filtering time of Vb under voltage detection	VB1,VB2	Tbl	-	13	20	34	µs	-
Detection voltage of Vcc under voltage	VCC1,VCC2	Vthclh	-	2.7	2.85	3.0	V	-
		Vthcll	-	2.55	2.70	2.85	V	-
		Vthclhys	-	0.10	0.15	0.20	V	-
Replying time of Vcc under voltage detection	VCC1,VCC2	Tcl	-	10	20	40	µs	-
Detection voltage of Vcc over voltage	VCC1,VCC2	Vthchh	-	5.6	5.75	5.9	V	-
		Vthchl	-	5.5	5.65	5.8	V	-
		Vthchhys	-	0.05	0.10	0.15	V	-
Filtering time of Vcc over voltage detection	VCC1,VCC2	Tch	-	13	20	34	µs	-
Detection temperature of over temperature	-	Tsdh	-	(155)	(170)	(185)	°C	The numerical value in a parenthesis means a design value.
Release temperature of over temperature detection	-	Tsdl	-	(145)	(160)	(175)	°C	The numerical value in a parenthesis means a design value.
Filtering time of over temperature detection	-	Ttsd	-	(13)	(20)	(34)	µs	The numerical value in a parenthesis means a design value.

* The numerical value in a parenthesis means a design value. The shipment test is not performed.
* When Vcc is lower than the detection voltage of Vcc under voltage further, IC will be the stand-by state.

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4 MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
Filtering time of short-circuit detection	-	Tsf	-	3.9	6	10.2	µs	df_sh=000
				5.2	8	13.6		df_sh=001
				6.5	10	17.0		df_sh=010
				7.8	12	20.4		df_sh=011
Short-circuit detection threshold voltage (High-side)	-	Vthh_sh	-	0.4	0.5	0.6	V	vthh_sh=00
				0.6	0.75	0.9		vthh_sh=01
				0.8	1	1.2		vthh_sh=10
				1.0	1.25	1.5		vthh_sh=11
Short-detection threshold voltage (Low-side)	-	Vthl_sh	-	0.4	0.5	0.6	V	vthl_sh=00
				0.6	0.75	0.9		vthl_sh=01
				0.8	1	1.2		vthl_sh=10
				1.0	1.25	1.5		vthl_sh=11
NDIAG output voltage	NDIAG	Voh	Ioh = -5mA	0.9×Vcc	-	-	V	-
		Vol	Iol = 5mA	-	-	0.1×Vcc	V	-
L hold voltage	NDIAG	Vlk	Vcc=1.1V to Vthcll Iol = 100µA	0	-	0.3	V	Refer to Fig.5-2c.
Frequency of high frequency detection	-	Fh	-	6.4	8	9.6	MHz	-
Frequency of low frequency detection	-	Fl	-	1.6	2	2.4	MHz	-

The voltage between HS and SH of the IC terminals has prescribed the short-circuit detection threshold voltage (High-side).
The voltage between SH and PGND of the IC terminals has prescribed the short-circuit detection threshold voltage (Low-side).
* Since current flows into HS terminal and SH* terminal, the short-detection threshold value is decided by the external resistance of a register, HS, and SH*.

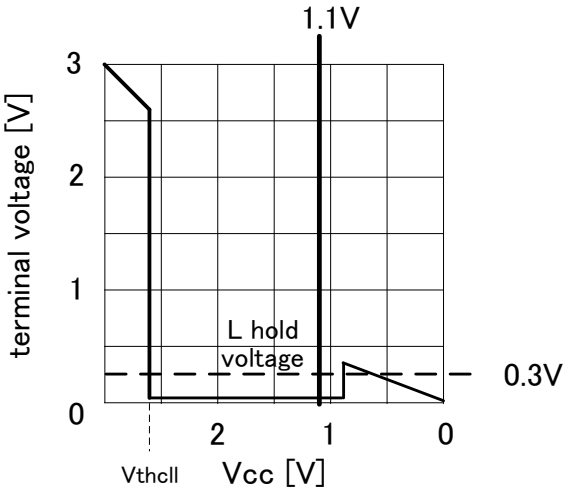


Fig.5-2c L hold voltage

ALARM input circuit

Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4 MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
High level input current	ALARM1 ALARM2	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	μA	-
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	μA	-
High level input detection voltage	ALARM1 ALARM2	Vih	-	0.75× Vcc	-	-	V	-
Low level input detection voltage		Vil		-	-	0.25× Vcc	V	-
Pulse width of input detection	ALARM1 ALARM2	Twmin	H,L detection	16x2²/Fc +1/Fc	-	-	s	df_alm1 = ”00” df_alm2 = ”00”
				1000x2²/Fc +1/Fc	-	-	s	df_alm1 = ”01” df_alm2 = ”01”
				2000x2²/Fc +1/Fc	-	-	s	df_alm1 = ”10” df_alm2 = ”10”
				4000x2²/Fc +1/Fc	-	-	s	df_alm1 = ”11” df_alm2 = ”11”
Pulse width of input removal	ALARM1 ALARM2	Twmax	H,L detection	-	-	15x2²/Fc -1/Fc	s	df_alm1 = ”00” df_alm2 = ”00”
				-	-	999x2²/Fc -1/Fc	s	df_alm1 = ”01” df_alm2 = ”01”
				-	-	1999x2²/Fc -1/Fc	s	df_alm1 = ”10” df_alm2 = ”10”
				-	-	3999x2²/Fc -1/Fc	s	df_alm1 = ”11” df_alm2 = ”11”

<<User note>>

*The pulse width of the input detection (Twmin) means the pulse width which passes through a digital filter and appears to an output. The pulse width of the input removal (Twmax) means the pulse width which is removed by the digital filter (Fig.6-b).

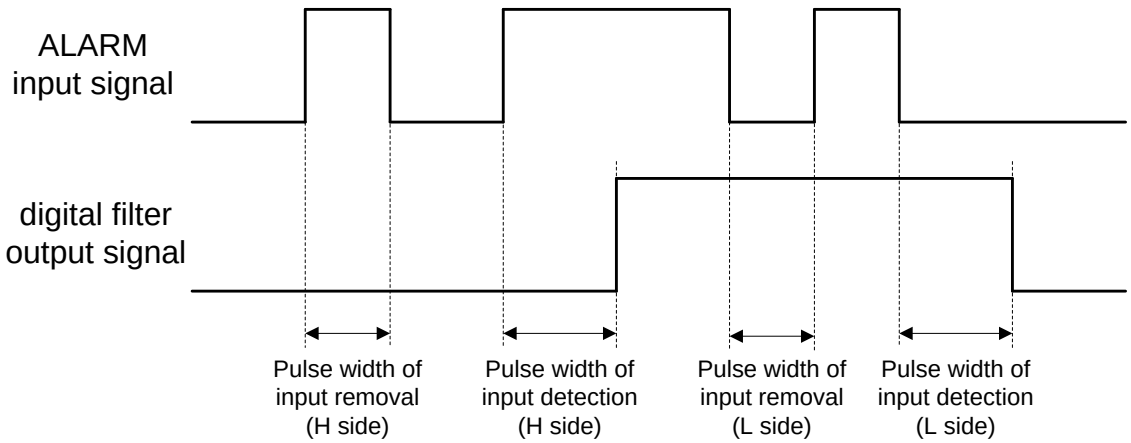


Fig.6-b Pulse width of input removal (with filter) and pulse width of input detection (with filter)

EN_CP Input circuit

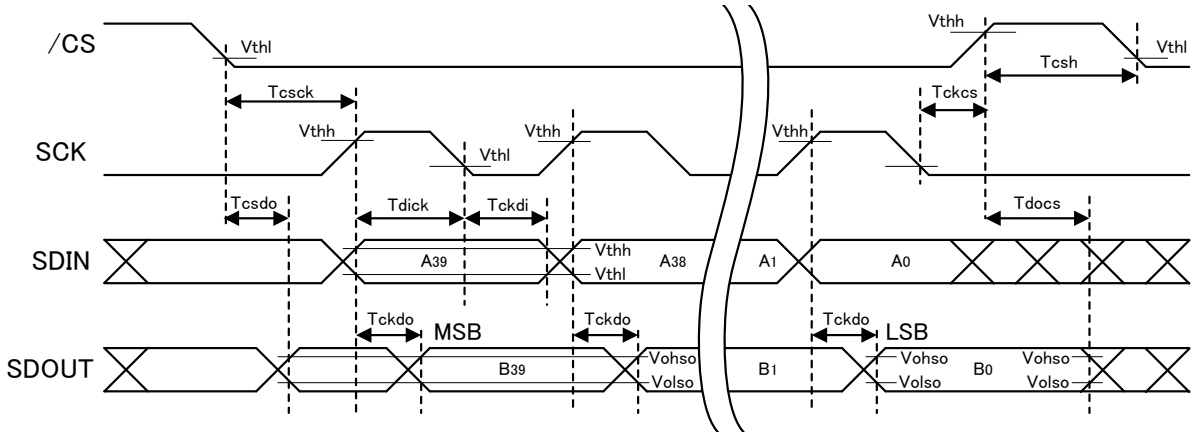
Unless otherwise specified, Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
High level input current	EN_CP	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	μA	-
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	μA	-
High level input detection voltage	EN_CP	Vih	-	0.75× Vcc	-	-	V	-
Low level input detection voltage		Vil		-	-	0.25× Vcc	V	-

SPI Communication circuit

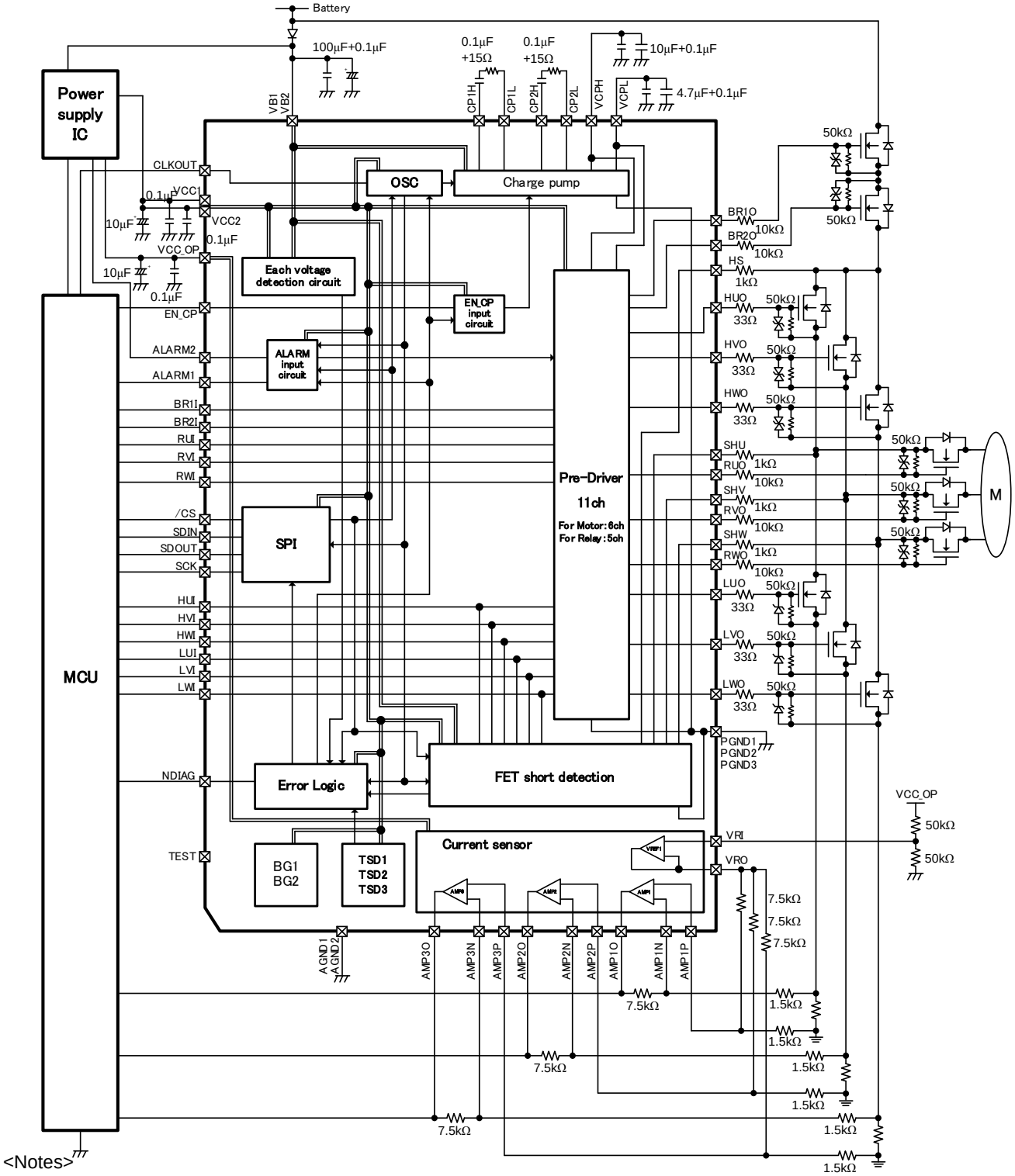
Unless otherwise specified,Vb=4.5 to 28V, Vcc=3 to 5.5V, Ta=-40 to 125°C, Fc=4 MHz

Item	Applied terminal	Symbol	Measurement condition	Min	Typ.	Max	Unit	Note
High level input current	/CS	Iih	Vcc = 5.0V, Vin = 5.0V	-5	-	5	μA	-
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-200	-100	-50	μA	-
High level input current	SCK, SDIN	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	μA	-
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	-	5	μA	-
High level input detection voltage	/CS, SCK, SDIN	Vthh	-	0.75×Vcc	-	-	V	-
Low level input detection voltage		Vthl		-	-	0.25×Vcc	V	-
Output voltage	SDOUT	Vohso	Iohso = -5mA	0.9×Vcc	-	-	V	-
		Volso	Iolso = 5mA	-	-	0.1×Vcc	V	-
Valid standby time	/CS SCK	Tcsck	fop = 2MHz	250	-	-	ns	Time from /CS falling edge to SCK rising edge.
Invalid standby time		Tckcs	-	250	-	-	ns	Time from the last SCK falling edge to /CS rising edge
Delay time from /CS falling to SDOUT	/CS SDOUT	Tcsdo	Cload=100pF	-	-	340	ns	Time until SDOUT stops being the Tri State from /CS falling edge
Delay time from SDOUT to /CS rising		Tdocs	Cload=100pF	-	-	100	ns	Time until SDOUT becomes the Tri State from /CS rising edge
SDIN setup time	SCK SDIN	Tdick	-	120	-	-	ns	Time when SDIN is valid before SCK falling edge
SDIN hold time		Tckdi	-	120	-	-	ns	Time when SDIN is valid after SCK falling edge
SDOUT valid time	SCK SDOUT	Tckdo	Cload=100pF	-	-	100	ns	Time from SCK rising edge to valid output data
/CS invalid time	/CS	Tcsh	-	5	-	-	μs	Invalid time between continuous /CS
Operation frequency	SCK	fop	-	-	-	2	MHz	-



SPI Timing chart

Reference circuit diagram



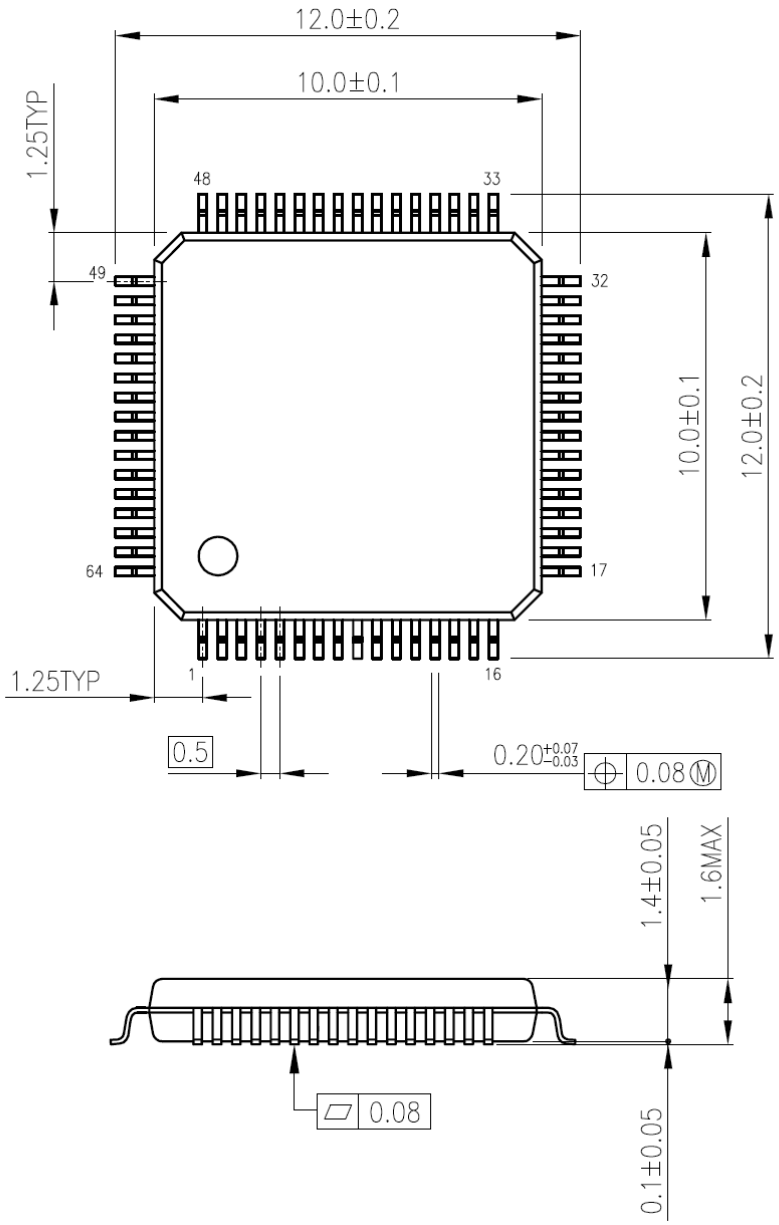
<Notes>

* These circuit constants are reference circuit examples, and are not guaranteed.
The external circuit should be decided after certainly evaluating and confirming on the unit board supposing the usage environment.
* The smoothing capacitor connected externally to the power supply terminals (VB1, VB2, VCC1, VCC2 and VCC_OP) should be the layout on the IC as close as possible.
*The power supply of the resistance partial pressure connected to the VRI terminal should be used as the same power supply as VCC_OP.
* AGND1, 2 and PGND1, 2, and 3 should be the solid GND (potential ±0.3V) on the unit board.
*Consider notes of each block at the time of a unit design.
* Do not implement incorrectly. The destruction of the ICs or the damage to the devices may occur.

PACKAGE

LQFP64-P-1010-0.50E

Unit: mm



Weight: 0.35 g (typ.)

Revision history

Version	Item	Contents (Changes)	Modification date
1.0	-	New release	2016-03-28
2.0	All chapter	Modify the specification by corresponding to the ES2.	2017-04-28
	Pre-driver circuit	Modify the block diagram and review the explanation.	
	Abnormal detection circuit	Review the explanation of operation. Add Note4 / Note5 Change the word `Latch` to `Hold` in each timing chart of the abnormal detection.	
	SPI Register Map	Review the explanation. Modify the status5 [7:4] register.	
	Reference circuit diagram	Modify the reference circuit diagram	
2.1	Abnormal detection circuit	Explanation of operation of oscillation frequency monitoring function, revision of timing chart of oscillation frequency monitoring function.	2017-08-07
	Absolute maximum ratings	Change of absolute maximum ratings.	
2.2	SPI Register Map	Modify the config 1 [3:1], 2[4:0], 3[7:6] [3:1] register.	2018-04-02
2.3	Absolute maximum ratings Operating voltage range	Delete time regulation of VB = 28 V.	2018-04-18
2.4	-	Modify the text.	2018-05-07
2.5	-	Add supplementary explanation	2019-02-27

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