

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC05P, TC74AC05F

Hex Inverter (open drain)

The TC74AC05 is an advanced high speed CMOS INVERTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74AC04, but the TC74AC05 has high performance MOS N-channel transistor (open-drain) outputs.

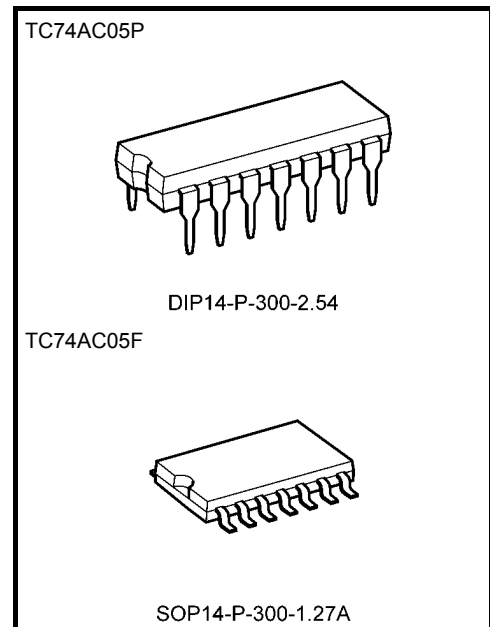
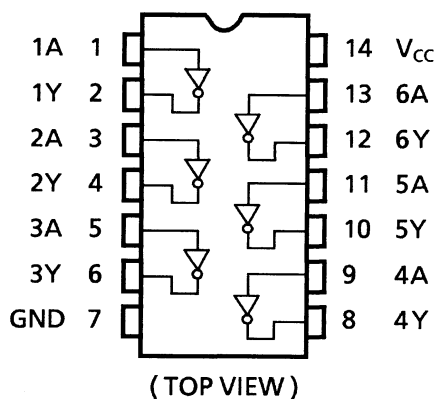
This device can, therefore, with a suitable pull-up resistor, be used in wired-OR, LED drive and other applications.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $t_{pZ} = 3.4 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Symmetrical output impedance: $I_{OL} = 24 \text{ mA (min)}$
Capability of driving 50Ω transmission lines.
- Wide operating voltage range: $V_{CC} \text{ (opr)} = 2 \text{ to } 5.5 \text{ V}$
- Open drain structure.
- Pin and function compatible with 74F05

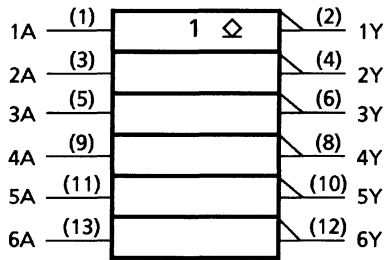
Pin Assignment



| | |
|-------------------|-----------------|
| Weight | |
| DIP14-P-300-2.54 | : 0.96 g (typ.) |
| SOP14-P-300-1.27A | : 0.18 g (typ.) |

Start of commercial production
1989-11

IEC Logic Symbol

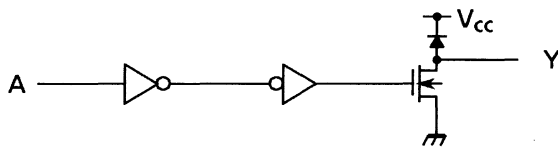


Truth Table

| | |
|---|---|
| A | Y |
| L | Z |
| H | L |

Z: High impedance

System Diagram (per gate)



Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|------------------------------|------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to $V_{CC} + 0.5$ | V |
| DC output voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | ±20 | mA |
| Output diode current | I_{OK} | ±50 | mA |
| DC output current | I_{OUT} | +50 | mA |
| DC V_{CC} /ground current | I_{CC} | ±150 | mA |
| Power dissipation | P_D | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | T_{stg} | -65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---|------|
| Supply voltage | V_{CC} | 2.0 to 5.5 | V |
| Input voltage | V_{IN} | 0 to V_{CC} | V |
| Output voltage | V_{OUT} | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | -40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition | | $T_a = 25^\circ\text{C}$ | | | $T_a = -40$ to 85°C | | Unit | |
|----------------------------------|----------|---|---------------------------------|--------------------------|------|------|-----------------------------------|------|-----------|---------------|
| | | | | V_{CC} (V) | Min | Typ. | Max | Min | | Max |
| High-level input voltage | V_{IH} | — | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | 3.0 | 2.10 | — | — | 2.10 | — | |
| | | | | 5.5 | 3.85 | — | — | 3.85 | — | |
| Low-level input voltage | V_{IL} | — | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | 3.0 | — | — | 0.90 | — | 0.90 | |
| | | | | 5.5 | — | — | 1.65 | — | 1.65 | |
| Low-level output voltage | V_{OL} | $V_{IN} = V_{IH}$ | $I_{OL} = 50 \mu\text{A}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL} = 12 \text{ mA}$ | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | | 4.5 | — | — | 0.36 | — | 0.44 | |
| $I_{OL} = 24 \text{ mA}$ | 3.0 | — | — | 0.36 | — | 0.44 | | | | |
| | 4.5 | — | — | 0.36 | — | 0.44 | | | | |
| Low-level output voltage | V_{OL} | $V_{IN} = V_{IH}$ | $I_{OL} = 75 \text{ mA (Note)}$ | 5.5 | — | — | — | — | 1.65 | |
| | | | | 5.5 | — | — | — | — | 1.65 | |
| 3-state output off-state current | I_{OZ} | $V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ | | 5.5 | — | — | ± 0.5 | — | ± 5.0 | μA |
| Input leakage current | I_{IN} | $V_{IN} = V_{CC}$ or GND | | 5.5 | — | — | ± 0.1 | — | ± 1.0 | μA |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.
One output should be tested at a time for a 10 ms maximum duration.

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \text{ } \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C | | Unit | |
|-------------------------------|--------------------|----------------|-----------|-----|------|------------------|-----|------|-----|
| | | | VCC (V) | Min | Typ. | Max | Min | | Max |
| Propagation delay time | t_{pLZ} | — | 3.3 ± 0.3 | — | 4.1 | 7.0 | 1.0 | 8.0 | ns |
| | | | 5.0 ± 0.5 | — | 3.5 | 5.3 | 1.0 | 6.0 | |
| Propagation delay time | t_{pZL} | — | 3.3 ± 0.3 | — | 5.9 | 9.1 | 1.0 | 10.4 | ns |
| | | | 5.0 ± 0.5 | — | 4.1 | 6.6 | 1.0 | 7.5 | |
| Input capacitance | C_{IN} | — | — | 5 | 10 | — | 10 | pF | |
| Output capacitance | C_{OUT} | — | — | 10 | — | — | — | pF | |
| Power dissipation capacitance | C_{PD} (Note) | — | — | 8 | — | — | — | pF | |

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per gate)}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm



Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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