

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74AC161P, TC74AC161F, TC74AC161FT TC74AC163P, TC74AC163F, TC74AC163FT

Synchronous Presettable 4-Bit Binary Counter

TC74AC161P/F/FT Asynchronous Clear

TC74AC163P/F/FT Synchronous Clear

The TC74AC161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both  $\overline{LOAD}$  and  $\overline{CLR}$  inputs are active on low logic level.

Presetting of these IC's is synchronous to the rising edge of CK.

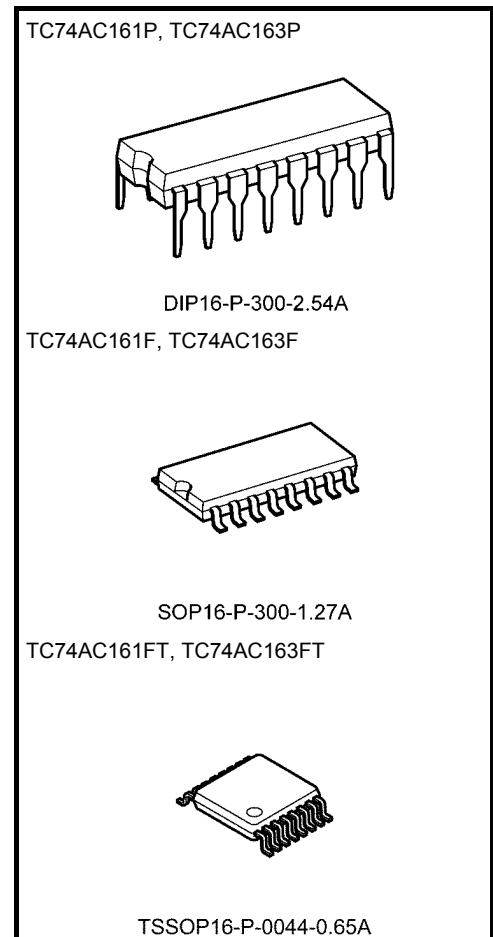
The clear function of the TC74AC163 is synchronous to CK, while the TC74AC161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{max} = 170$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 8$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24$  mA (min)  
Capability of driving 50  $\Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (opr) = 2$  to 5.5 V
- Pin and function compatible with 74F161/163

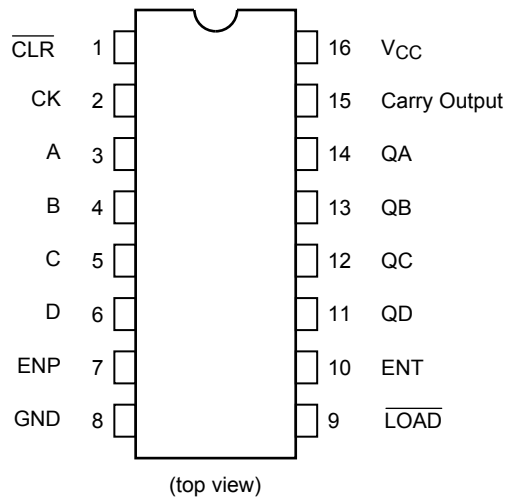


### Weight

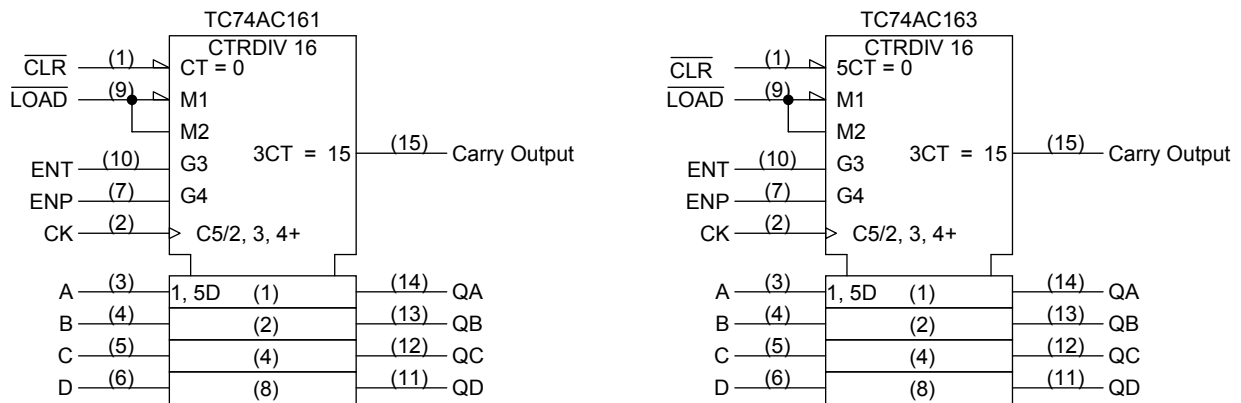
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)

Start of commercial production  
1987-05

## Pin Assignment



## IEC Logic Symbol



## Truth Table (Note)

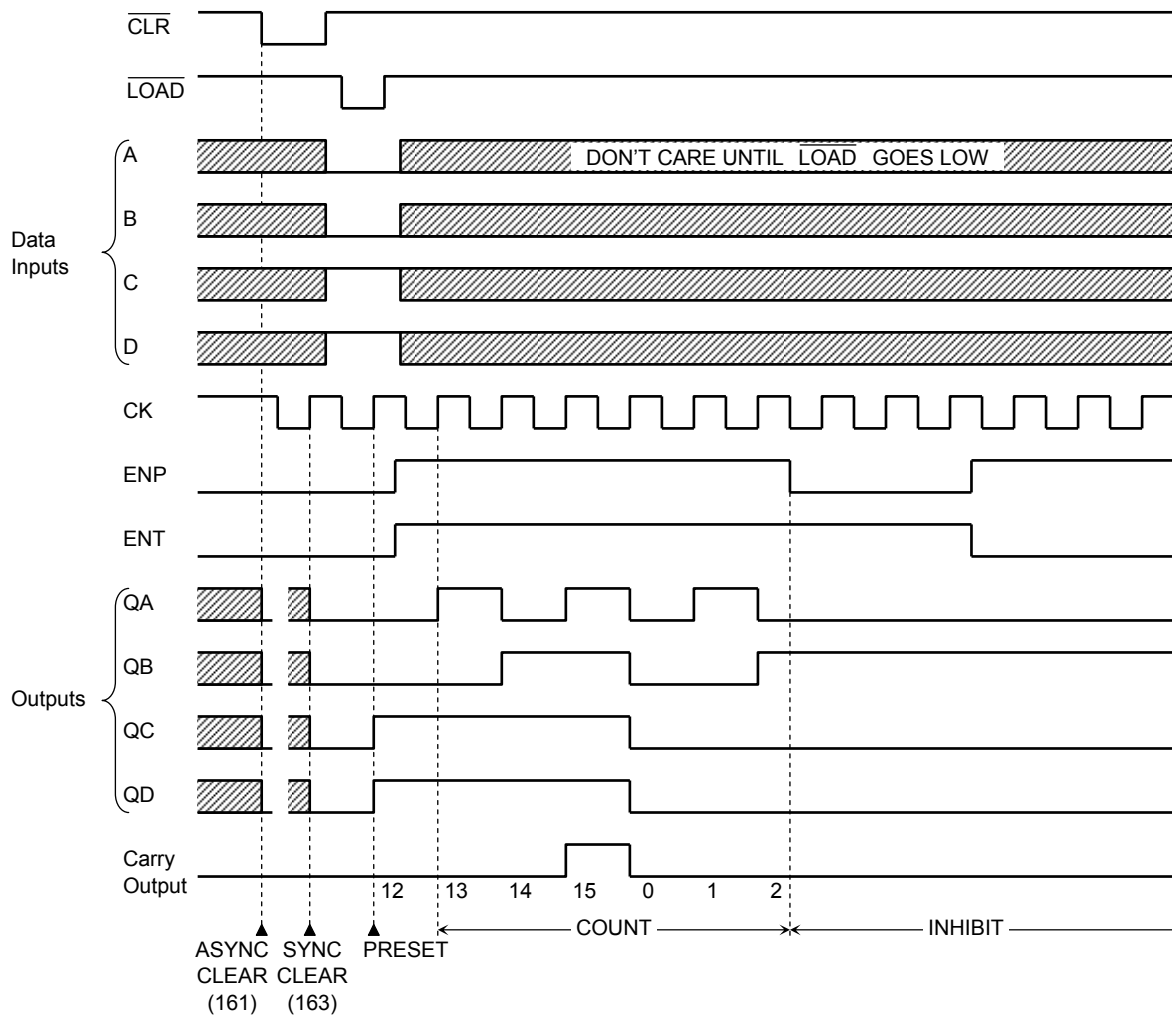
Inputs							Outputs				Function
$\overline{\text{CLR}}$ (161)	$\overline{\text{CLR}}$ (163)	$\overline{\text{LOAD}}$	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X	$\uparrow$	L	L	L	L	Reset to "0"
H	H	L	X	X	$\uparrow$	$\uparrow$	A	B	C	D	Preset Data
H	H	H	X	L	$\uparrow$	$\uparrow$	No Change				No Count
H	H	H	L	X	$\uparrow$	$\uparrow$	No Change				No Count
H	H	H	H	H	$\uparrow$	$\uparrow$	Count Up				Count
H	X	X	X	X	$\downarrow$	$\downarrow$	No Change				No Count

Note: X: Don't care

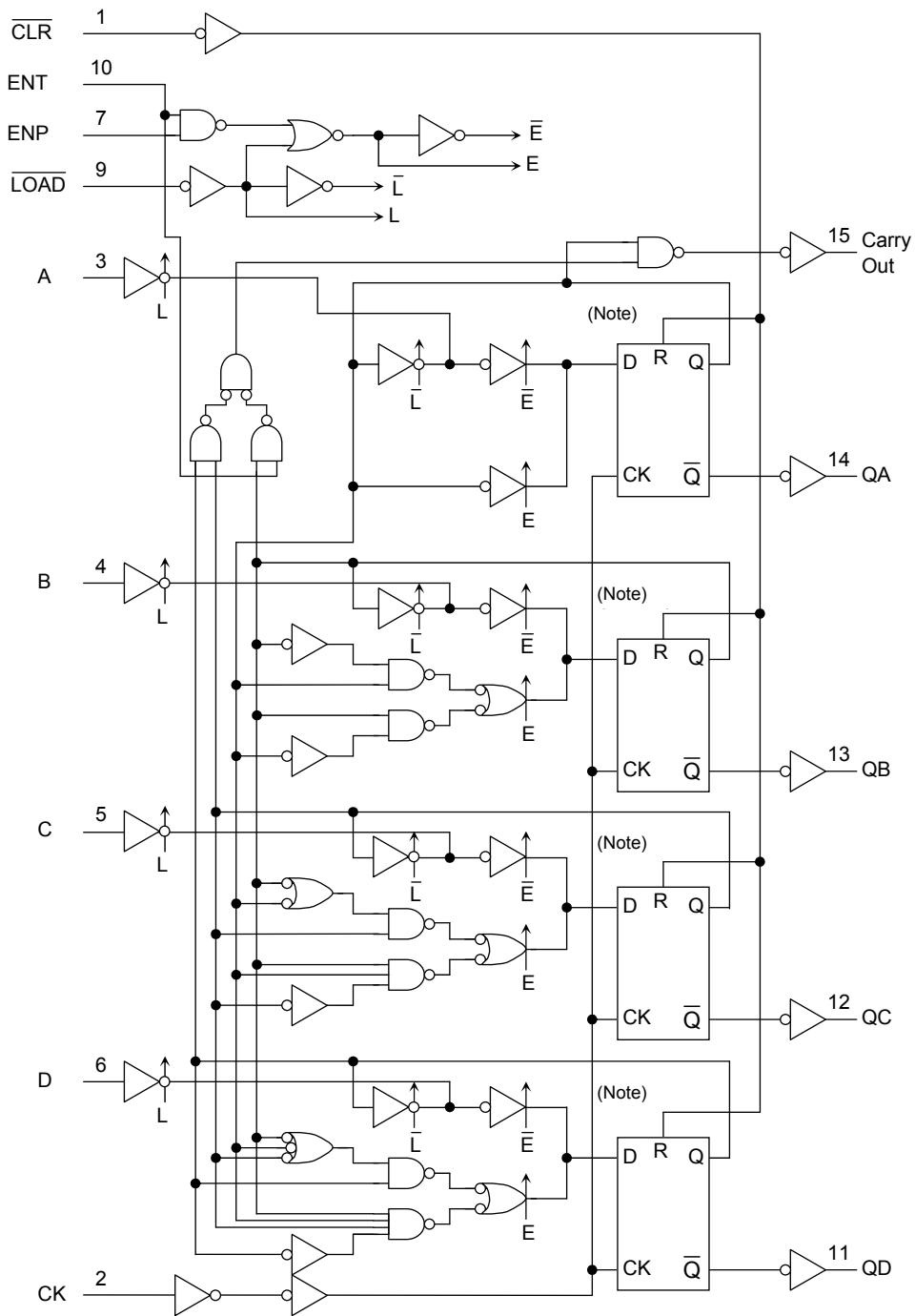
A, B, C, D: Logic level of data inputs

Carry: Carry = ENT · QA · QB · QC · QD

**Timing Chart**



## System Diagram



Note: Truth table of internal F/F

TC74AC161					TC74AC163				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	H	L	H	X	$\uparrow$	H	L	H
L	$\uparrow$	L	L	H	L	$\uparrow$	L	L	H
H	$\uparrow$	L	H	L	H	$\uparrow$	L	H	L
X	$\downarrow$	L	No Change		X	$\downarrow$	L	No Change	

X: Don't care

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 125$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10$  mW/°C should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dV$	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	V <sub>IH</sub>	—	2.0	1.50	—	—	1.50	—	V	
			3.0	2.10	—	—	2.10	—		
			5.5	3.85	—	—	3.85	—		
Low-level input voltage	V <sub>IL</sub>	—	2.0	—	—	0.50	—	0.50	V	
			3.0	—	—	0.90	—	0.90		
			5.5	—	—	1.65	—	1.65		
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—	
		I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—		
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 12 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44	
		I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65		
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	8.0	—	80.0	μA	

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

**Timing Requirements (input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			VCC (V)	Limit	Limit	Limit	
Minimum pulse width (CK)	$t_w(L)$ $t_w(H)$	Figure 1	3.3 ± 0.3	7.0	7.0	ns	
			5.0 ± 0.5	5.0	5.0		
Minimum pulse width ( $\overline{CLR}$ ) (Note 1)	$t_w(L)$	Figure 4	3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns	
Minimum set-up time ( $\overline{LOAD}$ , ENP, ENT)	$t_s$	Figure 2, Figure 3	3.3 ± 0.3	11.0	13.0	ns	
			5.0 ± 0.5	7.0	7.0		
Minimum set-up time (A, B, C, D)	$t_s$	Figure 2	3.3 ± 0.3	8.0	8.0	ns	
			5.0 ± 0.5	4.0	4.0		
Minimum set-up time ( $\overline{CLR}$ ) (Note 2)	$t_s$	Figure 5	3.3 ± 0.3	6.0	6.0	ns	
			5.0 ± 0.5	4.0	4.0		
Minimum hold time	$t_h$	Figure 2, Figure 3, Figure 5	3.3 ± 0.3	1.0	1.0	ns	
			5.0 ± 0.5	1.0	1.0		
Minimum removal time ( $\overline{CLR}$ ) (Note 1)	$t_{rem}$	Figure 4	3.3 ± 0.3	6.0	6.0	ns	
			5.0 ± 0.5	4.0	4.0		

Note 1: For TC74AC161 only

Note 2: For TC74AC163 only

## AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	$t_{pLH}$	Figure 1	$3.3 \pm 0.3$	—	8.8	15.8	1.0	18.0	ns
	$t_{pHL}$		$5.0 \pm 0.5$	—	6.5	9.6	1.0	11.0	
Propagation delay time (CK-carry, count mode)	$t_{pLH}$	Figure 1	$3.3 \pm 0.3$	—	10.4	18.4	1.0	21.6	ns
	$t_{pHL}$		$5.0 \pm 0.5$	—	8.1	11.8	1.0	13.5	
Propagation delay time (CK-carry, preset mode)	$t_{pLH}$	Figure 2	$3.3 \pm 0.3$	—	12.9	22.4	1.0	25.5	ns
	$t_{pHL}$		$5.0 \pm 0.5$	—	9.1	13.2	1.0	15.0	
Propagation delay time (ENT-carry)	$t_{pLH}$	Figure 6	$3.3 \pm 0.3$	—	7.5	13.2	1.0	15.0	ns
	$t_{pHL}$		$5.0 \pm 0.5$	—	5.8	8.3	1.0	9.5	
Propagation delay time ( $\overline{\text{CLR}}$ -Q) (Note 1)	$t_{pHL}$	Figure 4	$3.3 \pm 0.3$	—	10.6	18.4	1.0	21.0	ns
			$5.0 \pm 0.5$	—	7.7	11.4	1.0	13.0	
Propagation delay time ( $\overline{\text{CLR}}$ -carry) (Note 1)	$t_{pHL}$	Figure 4	$3.3 \pm 0.3$	—	12.0	21.0	1.0	24.0	ns
			$5.0 \pm 0.5$	—	8.6	12.7	1.0	14.5	
Maximum clock frequency	$f_{max}$	—	$3.3 \pm 0.3$	50	110	—	50	—	MHz
			$5.0 \pm 0.5$	90	140	—	90	—	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{PD}$	(Note 2)	—	85	—	—	—	pF	

Note 1: For TC74AC161 only

Note 2:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of  $C_{PD}$ , and  $\Delta I_{CC}$  which is obtained from the following formula:

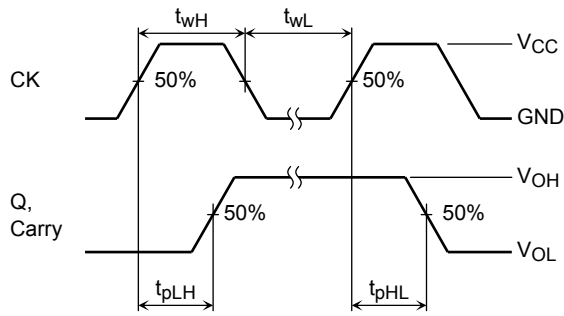
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

$C_{QA}$  to  $C_{QD}$  and  $C_{CO}$  are the capacitances at QA to QD and CARRY OUT, respectively.

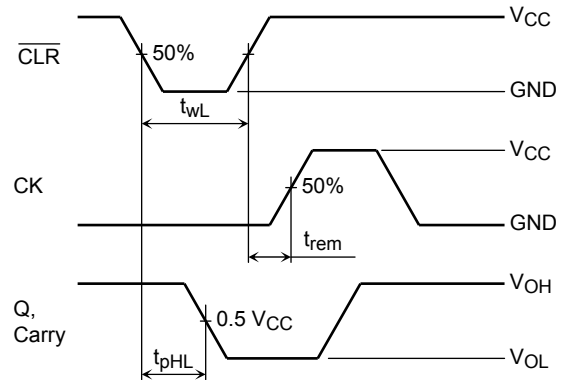
$f_{CK}$  is the input frequency of the CK.



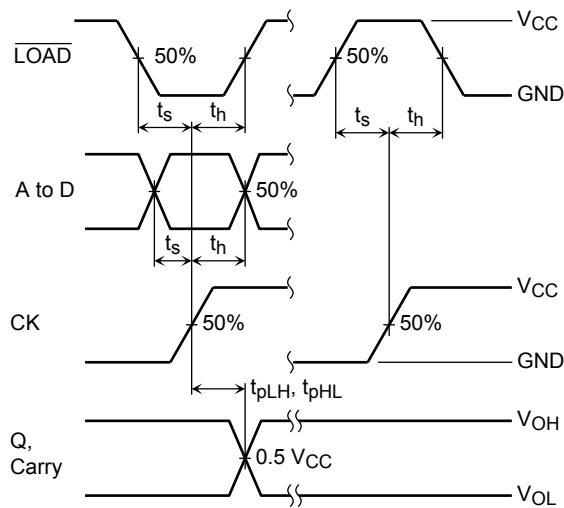
**Switching Characteristics Test Waveform**



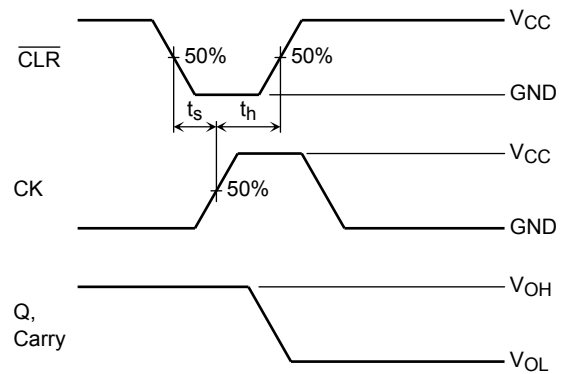
**Figure 1 Count Mode**



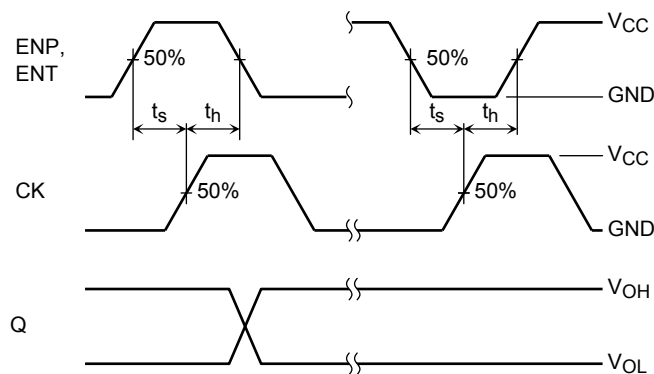
**Figure 4 Clear Mode (TC74AC161)**



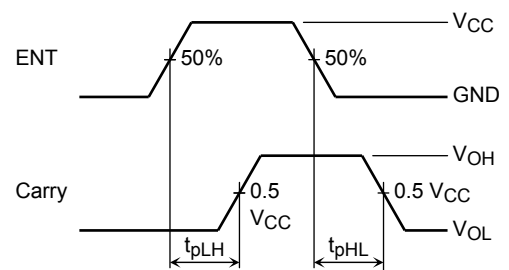
**Figure 2 Preset Mode**



**Figure 5 Clear Mode (TC74AC163)**



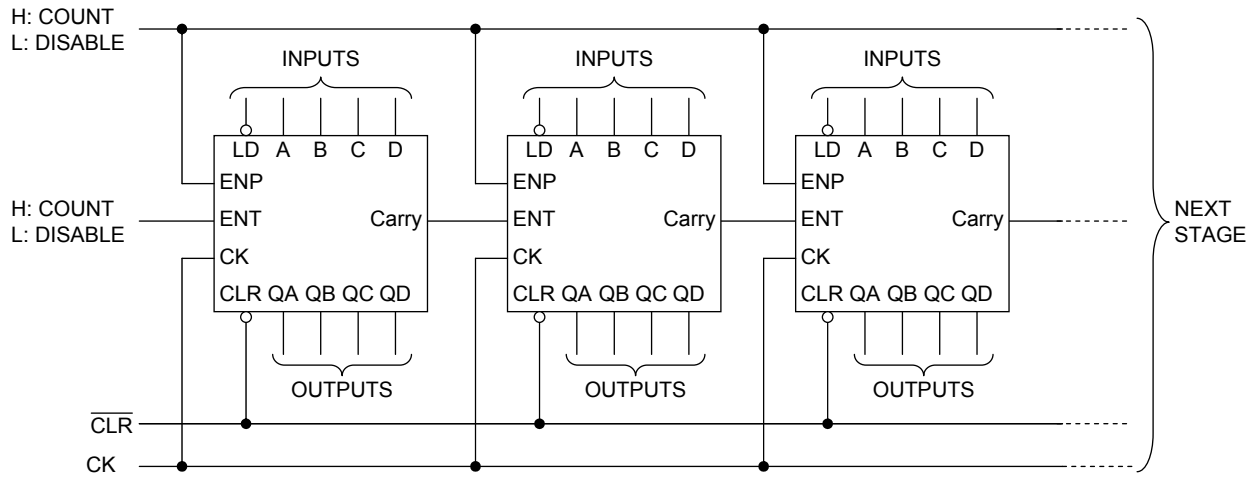
**Figure 3 Count Enable Mode**



**Figure 6 Cascade Mode (fix maximum count)**

**Typical Application**

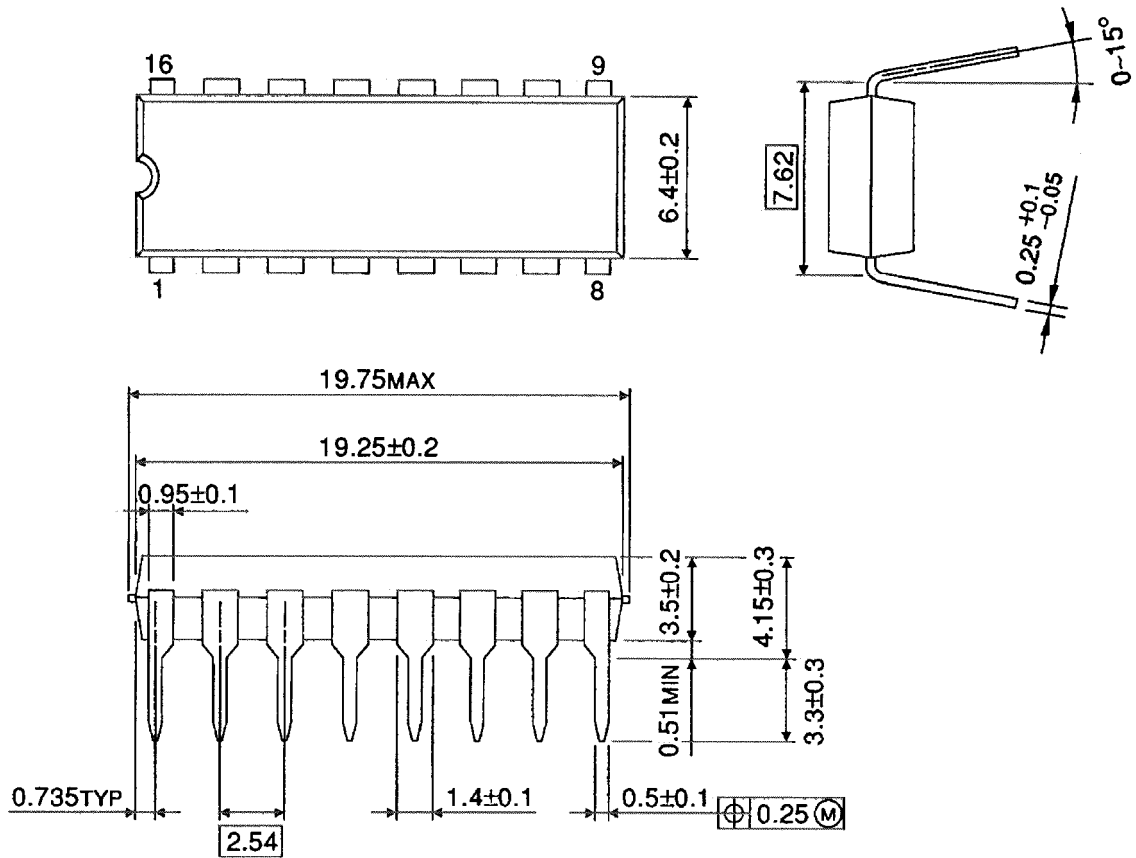
**Parallel Carry N-Bit Counter**



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

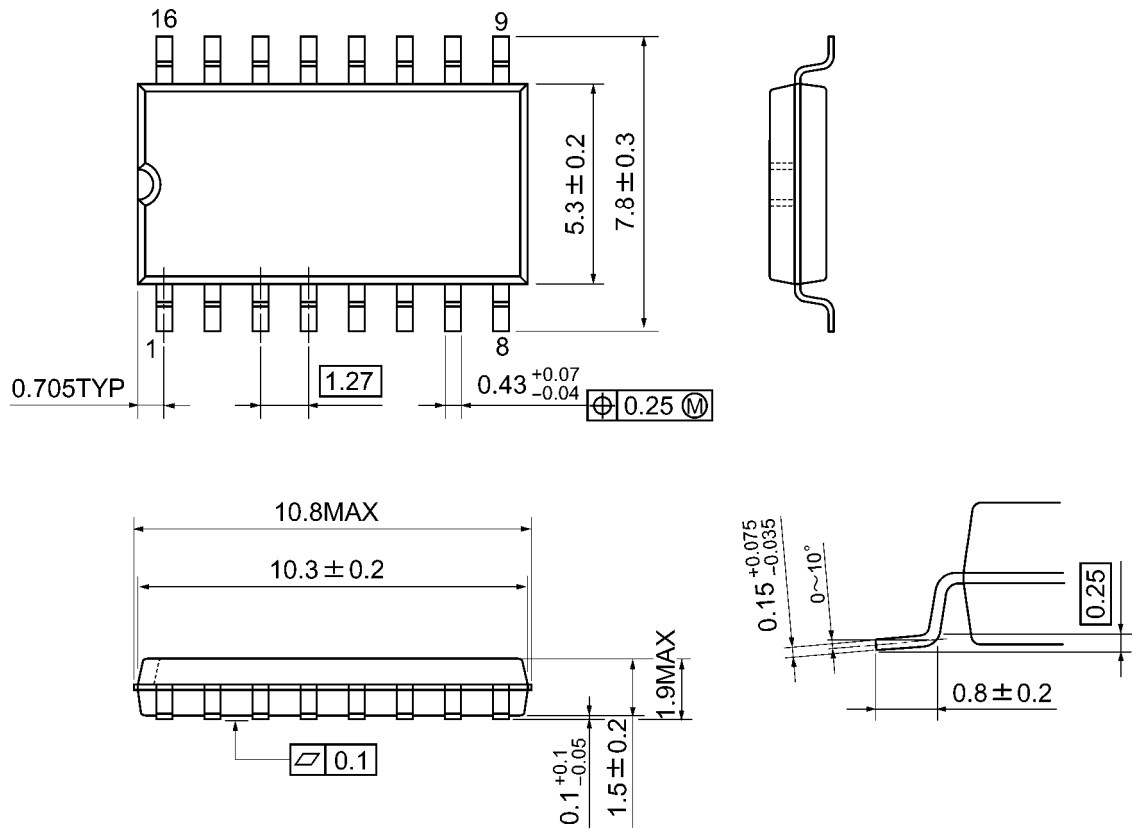


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm

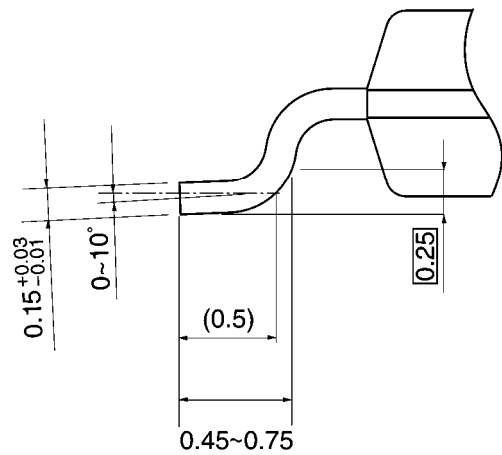
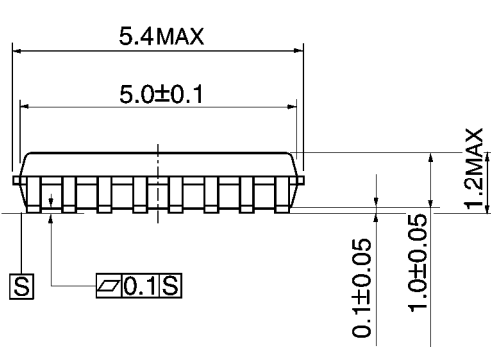
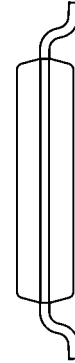
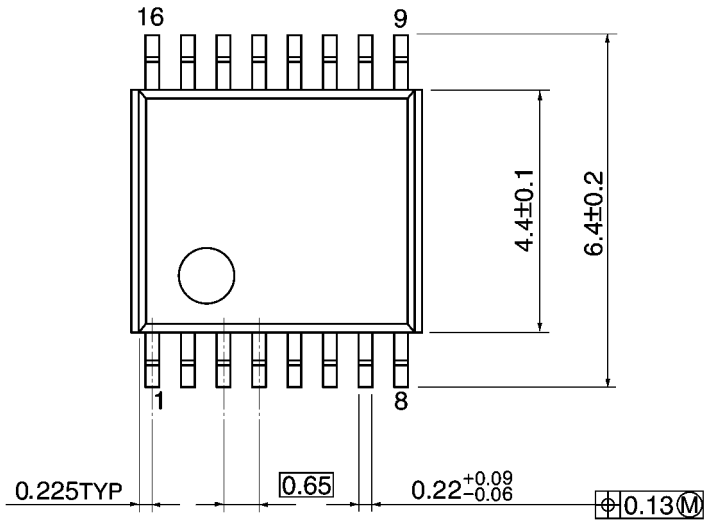


Weight: 0.18 g (typ.)

**Package Dimensions**

TSSOP16-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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