

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74ACT540P, TC74ACT540F, TC74ACT540FT TC74ACT541P, TC74ACT541F, TC74ACT541FT

Octal Bus Buffer

| | |
|------------------|--------------------------------|
| TC74ACT540P/F/FT | Inverting, 3-State Outputs |
| TC74ACT541P/F/FT | Non-Inverting, 3-State Outputs |

The TC74ACT540/TC74ACT541 are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

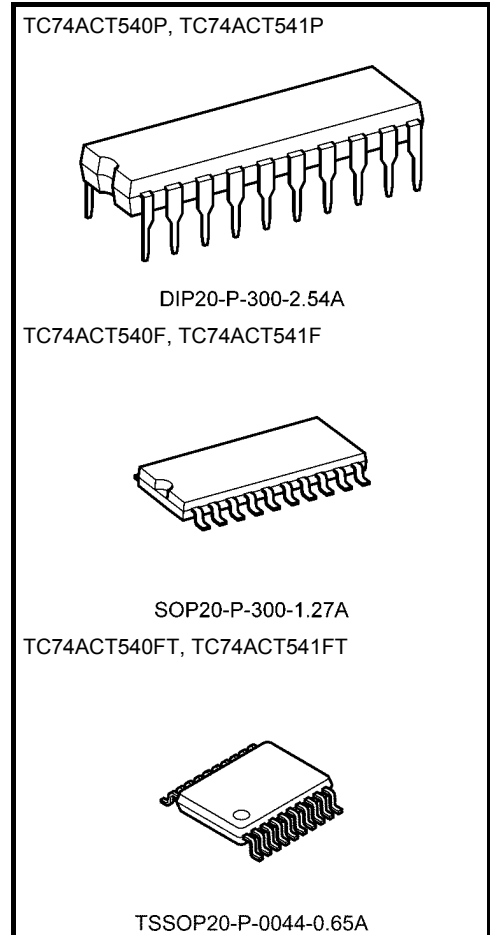
The TC74ACT540 is an inverting type, and the TC74ACT541 is a non-inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $t_{pd} = 4.3 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs
: $V_{IL} = 0.8 \text{ V (max)}$ $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance
: $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$
Capability of driving 50Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F540/541

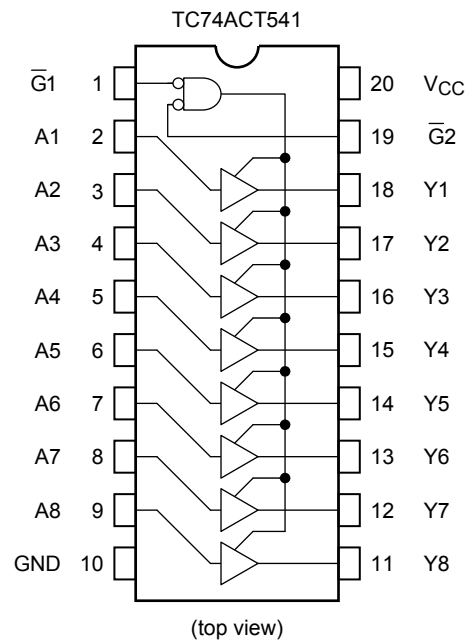
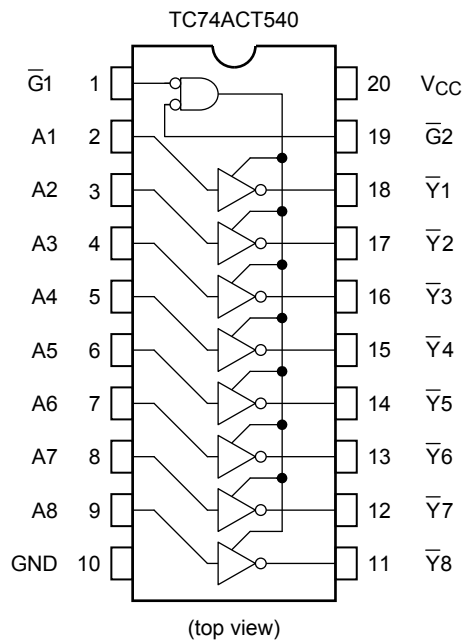


Weight

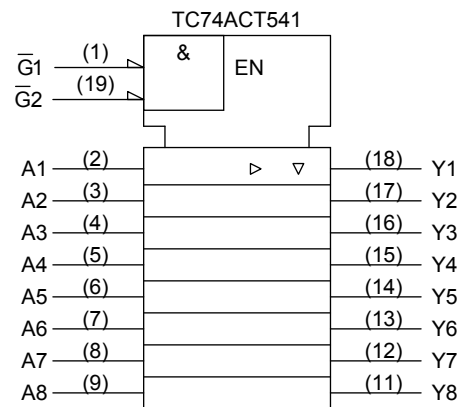
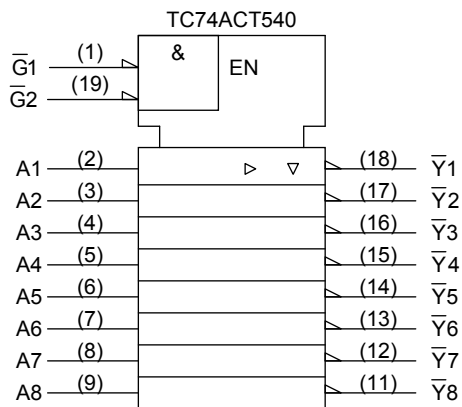
| | |
|----------------------|-----------------|
| DIP20-P-300-2.54A | : 1.30 g (typ.) |
| SOP20-P-300-1.27A | : 0.22 g (typ.) |
| TSSOP20-P-0044-0.65A | : 0.08 g (typ.) |

Start of commercial production
1988-10

Pin Assignment



IEC Logic Symbol



Truth Table

| Inputs | | | Outputs | |
|------------|------------|-------|---------|-------------|
| $\bar{G}1$ | $\bar{G}2$ | A_n | Y_n | \bar{Y}_n |
| H | X | X | Z | Z |
| X | H | X | Z | Z |
| L | L | H | H | L |
| L | L | L | L | H |

X: Don't care

Z: High impedance

Y_n : ACT541

\bar{Y}_n : ACT540

Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|------------------------------------|-------------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to $V_{CC} + 0.5$ | V |
| DC output voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | ± 20 | mA |
| Output diode current | I_{OK} | ± 50 | mA |
| DC output current | I_{OUT} | ± 50 | mA |
| DC V_{CC} /ground current | I_{CC} | ± 200 | mA |
| Power dissipation | P_D | 500 (DIP) (Note 2)/180 (SOP/TSSOP) | mW |
| Storage temperature | T_{stg} | -65 to 150 | $^{\circ}C$ |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to $65^{\circ}C$. From $T_a = 65$ to $85^{\circ}C$ a derating factor of -10 mW/ $^{\circ}C$ should be applied up to 300 mW.

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---------------|-------------|
| Supply voltage | V_{CC} | 4.5 to 5.5 | V |
| Input voltage | V_{IN} | 0 to V_{CC} | V |
| Output voltage | V_{OUT} | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | -40 to 85 | $^{\circ}C$ |
| Input rise and fall time | dt/dV | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = -40 to 85°C | | Unit | |
|----------------------------------|-----------------|---|---------------------------------|---------------------|------|------|------------------|------|------|-----|
| | | | | V _{CC} (V) | Min | Typ. | Max | Min | | Max |
| High-level input voltage | V _{IH} | — | | 4.5 to 5.5 | 2.0 | — | — | 2.0 | — | V |
| Low-level input voltage | V _{IL} | — | | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | V |
| High-level output voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50 μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | I _{OH} = -24 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | | | I _{OH} = -75 mA (Note) | 5.5 | — | — | — | 3.85 | — | |
| Low-level output voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50 μA | 4.5 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | I _{OL} = 24 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| | | | I _{OL} = 75 mA (Note) | 5.5 | — | — | — | — | 1.65 | |
| 3-state output off-state current | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | | 5.5 | — | — | ±0.5 | — | ±5.0 | μA |
| Input leakage current | I _{IN} | V _{IN} = V _{CC} or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | I _{CC} | V _{IN} = V _{CC} or GND | | 5.5 | — | — | 8.0 | — | 80.0 | μA |
| | I _C | Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND | | 5.5 | — | — | 1.35 | — | 1.5 | mA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: t_r = t_f = 3 ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C | | Unit | |
|---|------------------|----------------|---------------------|-----|------|------------------|-----|------|-----|
| | | | V _{CC} (V) | Min | Typ. | Max | Min | | Max |
| Propagation delay time (Note 2) | t _{pLH} | — | 5.0 ± 0.5 | — | 5.0 | 8.3 | 1.0 | 9.5 | ns |
| | t _{pHL} | — | 5.0 ± 0.5 | — | 5.0 | 8.3 | 1.0 | 9.5 | |
| Propagation delay time (Note 3) | t _{pLH} | — | 5.0 ± 0.5 | — | 5.0 | 8.3 | 1.0 | 9.5 | ns |
| | t _{pHL} | — | 5.0 ± 0.5 | — | 5.0 | 8.3 | 1.0 | 9.5 | |
| Output enable time | t _{pZL} | — | 5.0 ± 0.5 | — | 7.3 | 11.4 | 1.0 | 13.0 | ns |
| | t _{pZH} | — | 5.0 ± 0.5 | — | 7.3 | 11.4 | 1.0 | 13.0 | |
| Output disable time | t _{pLZ} | — | 5.0 ± 0.5 | — | 5.9 | 9.2 | 1.0 | 10.5 | ns |
| | t _{pHZ} | — | 5.0 ± 0.5 | — | 5.9 | 9.2 | 1.0 | 10.5 | |
| Input capacitance | C _{IN} | — | — | 5 | 10 | — | 10 | pF | |
| Output capacitance | C _{OUT} | — | — | 10 | — | — | — | pF | |
| Power dissipation capacitance (Note 1) | C _{PD} | TC74ACT540 | — | 24 | — | — | — | pF | |
| | | TC74ACT541 | — | 27 | — | — | — | | |

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Note 2: For TC74ACT540 only

Note 3: For TC74ACT541 only

Package Dimensions

DIP20-P-300-2.54A

Unit : mm



Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

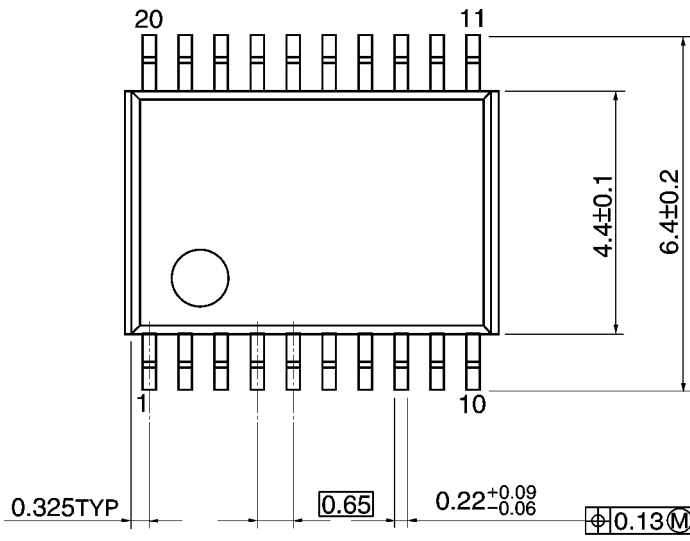


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

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