

# TC74HCT273AP, TC74HCT273AF

## Octal D-Type Flip Flop with Clear

The TC74HCT273A is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

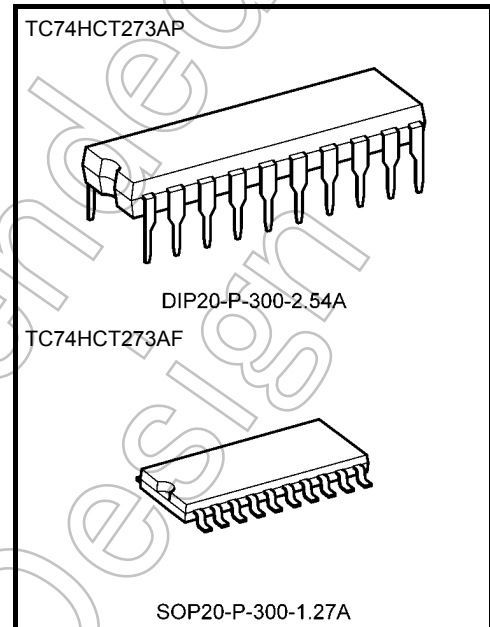
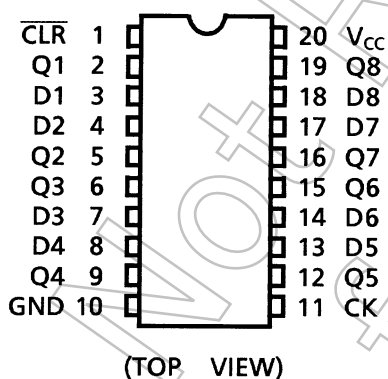
When the CLR input is held "L", the Q outputs are at a low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{max} = 90$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- Compatible with TTL outputs:  $V_{IH} = 2.0$  V (min)  
 $V_{IL} = 0.8$  V (max)
- Wide interfacing ability: LSTTL, NMOS, CMOS
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| \approx I_{OL} = 4$  mA (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74LS273

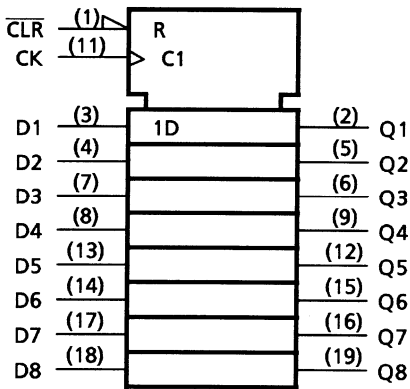
### Pin Assignment



Weight		
DIP20-P-300-2.54A	:	1.30 g (typ.)
SOP20-P-300-1.27A	:	0.22 g (typ.)

Start of commercial production  
1989-05

**IEC Logic Symbol**

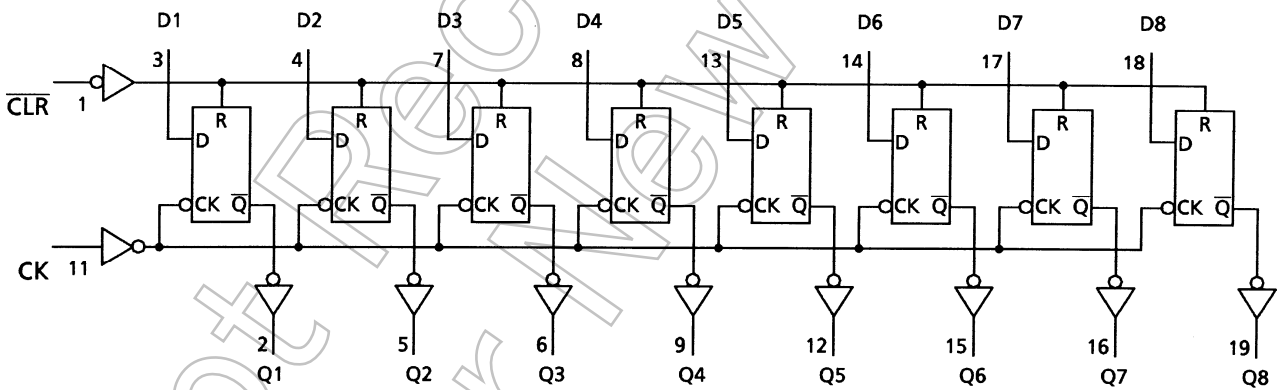


**Truth Table**

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Qn	No Change

X: Don't care

**System Diagram**



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	±20	mA
Output diode current	$I_{OK}$	±20	mA
DC output current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /ground current	$I_{CC}$	±50	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10$  mW/°C shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics**

**DC Characteristics**

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit		
			$V_{CC}$ (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	$V_{IH}$	—	4.5 to 5.5	2.0	—	—	2.0	—	V	
Low-level input voltage	$V_{IL}$	—	4.5 to 5.5	—	—	0.8	—	0.8	V	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	V
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	V
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA	
	$I_C$	Per input: $V_{IN} = 0.5 \text{ V}$ or $2.4 \text{ V}$ Other input: $V_{CC}$ or GND	5.5	—	—	2.0	—	2.9	mA	

**Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (CK)	$t_W (L)$	—	4.5	—	15	ns
	$t_W (H)$		5.5	—	14	
Minimum pulse width ( $\overline{\text{CLR}}$ )	$t_W (L)$	—	4.5	—	15	ns
			5.5	—	14	
Minimum set-up time	$t_s$	—	4.5	—	10	ns
			5.5	—	10	
Minimum hold time	$t_h$	—	4.5	—	5	ns
			5.5	—	10	
Minimum removal time ( $\overline{\text{CLR}}$ )	$t_{rem}$	—	4.5	—	10	ns
			5.5	—	9	
Clock frequency	f	—	4.5	—	30	MHz
			5.5	—	35	

**AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	4	8	ns
	$t_{THL}$					
Propagation delay time (CK-Q)	$t_{pLH}$	—	—	15	25	ns
	$t_{pHL}$					
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	$t_{pHL}$	—	—	18	28	ns
	$t_{pHL}$					
Maximum clock frequency	$f_{max}$	—	40	90	—	MHz

Not Recommended for New Design

**AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)**

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			VCC (V)	Min	Typ.	Max	Min		Max
Output transition time	t <sub>TLH</sub>	—	4.5	—	9	15	—	19	ns
	t <sub>THL</sub>		5.5	—	8	14	—	18	
Propagation delay time (CK-Q)	t <sub>pLH</sub>	—	4.5	—	19	30	—	38	ns
	t <sub>pHL</sub>		5.5	—	17	27	—	34	
Propagation delay time (CLR-Q)	t <sub>pLH</sub>	—	4.5	—	22	32	—	40	ns
	t <sub>pHL</sub>		5.5	—	18	29	—	36	
Maximum clock frequency	f <sub>max</sub>	—	4.5	30	71	—	24	—	MHz
			5.5	35	81	—	28	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	29	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per flip flop)}$$

And the total C<sub>PD</sub> when n pcs. of flip flop operate can be gained by the following equation:

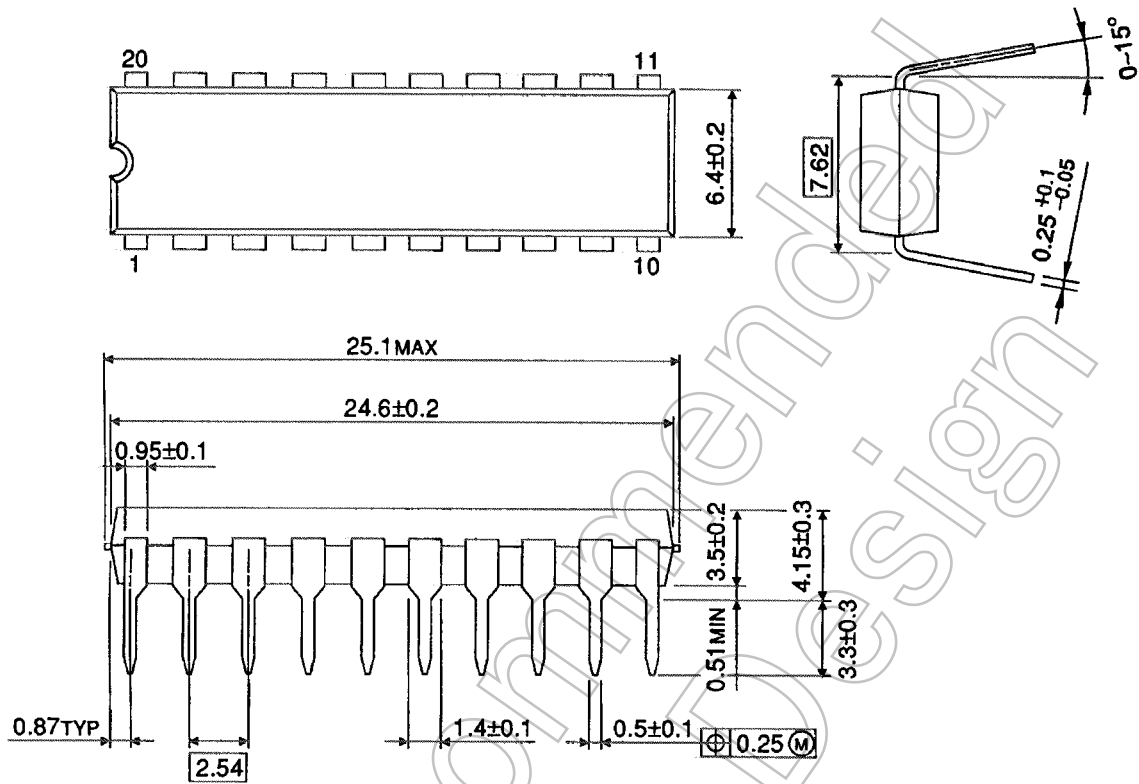
$$C_{PD} (total) = 18 + 11 \cdot n$$

Not Recommended for New Design

## Package Dimensions

DIP20-P-300-2.54A

Unit : mm



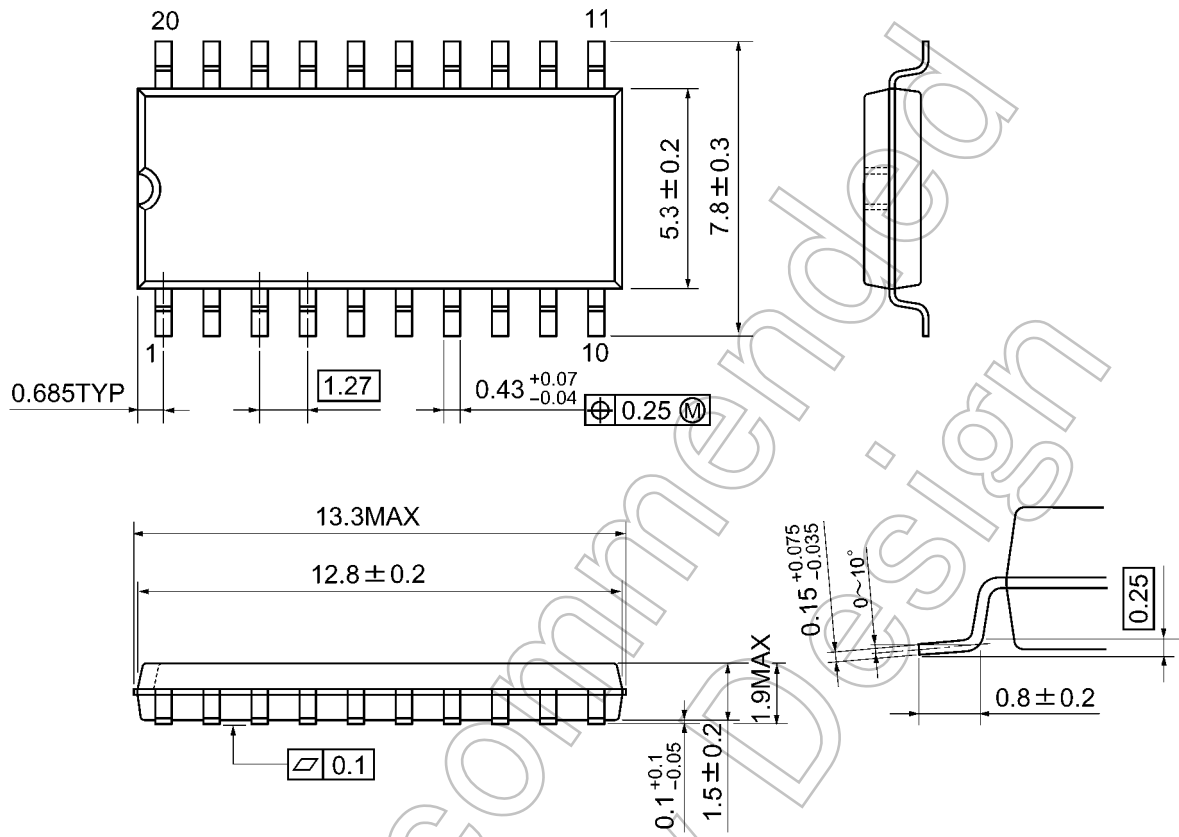
Weight: 1.30 g (typ.)

Not Recommended for New Design

**Package Dimensions**

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

Not Recommended for New Design

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