TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

TC74LVXC3245FS

## Dual Supply Octal Configurable Voltage Interface Bus Transceiver

The TC74LVXC3245FS is a dual supply, advanced high-speed CMOS octal configurable voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 3.3 V bus and a 3.3V to 5 V bus in mixed 3.3 V/5 V supply systems' it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses.

The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. The A-port interfaces with the 3.3-V bus, the B-port with the 3.3V to 5V bus. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when $\overline{G}$ is "H".

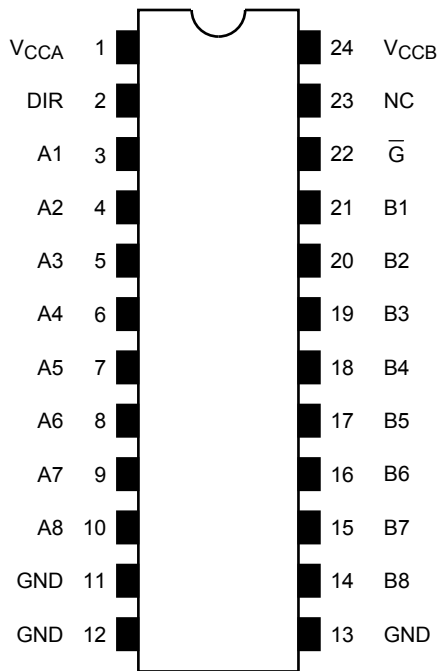All inputs are equipped with protection circuits against static discharge or transient excess voltage.

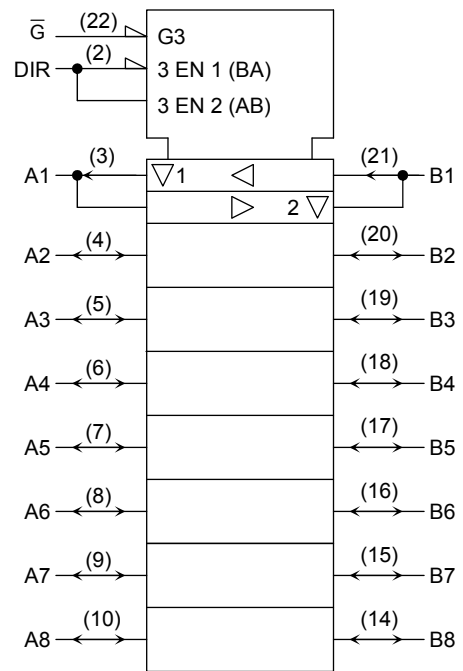SSOP24-P-300-0.65D
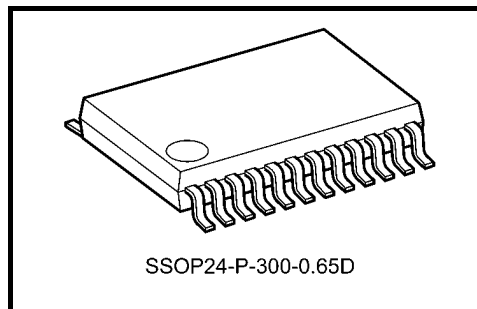
Weight: 0.14 g (typ.)

Features

- Bi-directional interface between 3 V and 5 V buses
- High-speed: t_{pd} = 8.5 ns (max)
  (V_{CCA} = 3.3 V, V_{CCB} = 5.0 V)
- Low power dissipation: I_{CC} = 8 μA (max) (Ta = 25°C)
- Symmetrical output impedance: I_{OUTA} = ±24 mA (min)
  I_{OUTB} = ±24 mA (min)
  (V_{CCA} = V_{CCB} = 3.0 V)
- Low noise: V_{OLP} = 1.5 V (max)
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{G}$ is "H"
- Package: SSOP (shrink small outline package)

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pin must have their input levels fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)

```
VCCA   1  ┌───┐ 24  VCCB
DIR    2  │   │ 23  NC
A1     3  │   │ 22  G̅
A2     4  │   │ 21  B1
A3     5  │   │ 20  B2
A4     6  │   │ 19  B3
A5     7  │   │ 18  B4
A6     8  │   │ 17  B5
A7     9  │   │ 16  B6
A8    10  │   │ 15  B7
GND   11  │   │ 14  B8
GND   12  └───┘ 13  GND
```

IEC Logic Symbol

```
G̅    (22) ──▷  G3
DIR  (2)  ──▷  3 EN 1 (BA)
              3 EN 2 (AB)

A1 (3) ──▽1    ◁──  (21) B1
              ▷  2 ▽
A2 (4) ──              (20) B2
A3 (5) ──              (19) B3
A4 (6) ──              (18) B4
A5 (7) ──              (17) B5
A6 (8) ──              (16) B6
A7 (9) ──              (15) B7
A8 (10) ──             (14) B8
```

Truth Table

Inputs		Outputs	Function	
G̅	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High impedance	

X: Don't care

Z: High impedance

Block Diagram
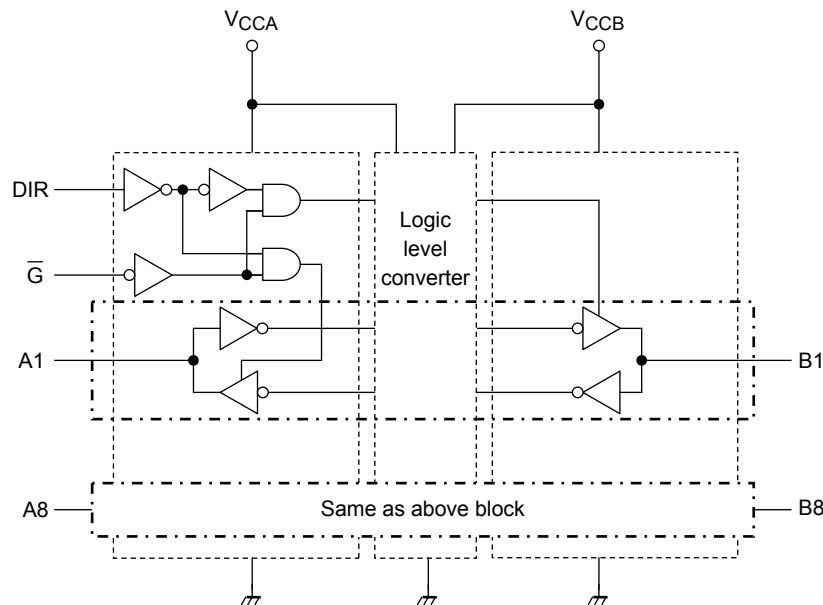
Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Supply voltage range		V_{CCA}	-0.5 to 7.0	V
	(Note 2)	V_{CCB}	-0.5 to 7.0	
DC input voltage	(DIR, $\overline{G}$)	V_{IN}	-0.5 to $V_{CCA} + 0.5$	V
DC bus I/O voltage		$V_{I/OA}$	-0.5 to $V_{CCA} + 0.5$	V
		$V_{I/OB}$	-0.5 to $V_{CCB} + 0.5$	
Input diode current		I_{IK}	±20	mA
Output diode current		$I_{I/OK}$	±50	mA
DC output current		I_{OUTA}	±50	mA
		I_{OUTB}	±50	
DC V_{CC}/ground current		I_{CCA}	±200	mA
		I_{CCB}	±200	
Power dissipation		P_D	180	mW
Storage temperature		T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don't supply a voltage to V_{CCB} terminal when V_{CCA} is in the OFF state.

Operating Ranges (Note 1)

Characteristics		Symbol	Rating	Unit
Supply voltage range		V_{CCA}	2.7 to 3.6	V
	(Note 2)	V_{CCB}	3.0 to 5.5	
Input voltage	(DIR, $\overline{G}$)	V_{IN}	0 to V_{CCA}	V
Bus I/O voltage		$V_{I/OA}$	0 to V_{CCA}	V
		$V_{I/OB}$	0 to V_{CCB}	
Operating temperature		T_{opr}	−40 to 85	°C
Input rise and fall time		dt/dv	0 to 8 (V_{CCA} = 2.7 to 3.6 V)	ns/V
			0 to 8 (V_{CCB} = 3.0 to 5.5 V)	

Note1: The operating ranges are required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note2: Don't use in V_{CCA} > V_{CCB}.

Electrical Characteristics

DC Characteristics

Characteristics		Sym-bol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
							Min	Typ.	Max	Min	Max	
Input voltage (V_{CCA})	H-level	V_{IHA}	DIR, $\overline{G}$, An		2.7	3.0	2.0	—	—	2.0	—	V
					3.0	3.6	2.0	—	—	2.0	—	
					3.6	5.5	2.0	—	—	2.0	—	
	L-level	V_{ILA}	DIR, $\overline{G}$, An		2.7	3.0	—	—	0.8	—	0.8	
					3.0	3.6	—	—	0.8	—	0.8	
					3.6	5.5	—	—	0.8	—	0.8	
Input voltage (V_{CCB})	H-level	V_{IHB}	Bn		2.7	3.0	2.0	—	—	2.0	—	V
					3.0	3.6	2.0	—	—	2.0	—	
					3.6	5.5	3.85	—	—	3.85	—	
	L-level	V_{ILB}	Bn		2.7	3.0	—	—	0.8	—	0.8	
					3.0	3.6	—	—	0.8	—	0.8	
					3.6	5.5	—	—	1.65	—	1.65	
Output voltage (V_{CCA})	H-level	V_{OHA}	$V_{INA} = V_{IHA}$ or V_{ILA} $V_{INB} = V_{IHB}$ or V_{ILB}	$I_{OH} = -100\ \mu A$	3.0	3.0	2.9	3.0	—	2.9	—	V
				$I_{OH} = -12\ mA$	3.0	3.0	2.56	—	—	2.46	—	
				$I_{OH} = -24\ mA$	3.0	3.0	2.35	—	—	2.25	—	
				$I_{OH} = -12\ mA$	2.7	3.0	2.3	—	—	2.2	—	
				$I_{OH} = -24\ mA$	2.7	4.5	2.1	—	—	2.0	—	
	L-level	V_{OLA}		$I_{OL} = 100\ \mu A$	3.0	3.0	—	0	0.1	—	0.1	
				$I_{OL} = 24\ mA$	3.0	3.0	—	—	0.36	—	0.44	
				$I_{OL} = 12\ mA$	2.7	3.0	—	—	0.36	—	0.44	
				$I_{OL} = 24\ mA$	2.7	4.5	—	—	0.42	—	0.5	

DC Characteristics (continued)

Characteristics		Sym-bol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
							Min	Typ.	Max	Min	Max	
Output voltage (V_{CCB})	H-level	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OH} = −100 µA	3.0	3.0	2.9	3.0	—	2.9	—	V
				I_{OH} = −12 mA	3.0	3.0	2.56	—	—	2.46	—	
				I_{OH} = −24 mA	3.0	3.0	2.35	—	—	2.25	—	
				I_{OH} = −24 mA	3.0	4.5	3.86	—	—	3.76	—	
	L-level	V_{OLB}		I_{OL} = 100 µA	3.0	3.0	—	0	0.1	—	0.1	
				I_{OL} = 24 mA	3.0	3.0	—	—	0.36	—	0.44	
				I_{OL} = 24 mA	3.0	4.5	—	—	0.36	—	0.44	
3-state output Off-state current		I_{OZA}	V_{INA} = V_{IHA} or V_{ILA}		3.6	3.6	—	—	±0.5	—	±5.0	µA
			V_{INB} = V_{IHB} or V_{ILB}		3.6	5.5	—	—	±0.5	—	±5.0	
		I_{OZB}	VI/OA = V_{CCA} or GND		3.6	3.6	—	—	±0.5	—	±5.0	
			VI/OB = V_{CCB} or GND		3.6	5.5	—	—	±0.5	—	±5.0	
Input leakage current		I_{IN}	V_{IN} (DIR, $\overline{G}$) = V_{CCA} or GND		3.6	3.6	—	—	±0.1	—	±1.0	µA
					3.6	5.5	—	—	±0.1	—	±1.0	
Quiescent supply current		I_{CCT}	PER INPUT: V_{IN} = 3.0 V		3.6	3.6	—	—	0.35	—	0.5	mA
		I_{CCA1}	An = V_{CCA} or GND Bn = Open, $\overline{G}$ = V_{CCA} DIR = V_{CCA}, V_{CCB} = Open		3.6	Open	—	—	5	—	50	µA
		I_{CCA2}	V_{INA} = V_{IHA} or V_{ILA}		3.6	3.6	—	—	5	—	50	
			V_{INB} = V_{IHB} or V_{ILB}		3.6	5.5	—	—	5	—	50	
		I_{CCB}	V_{INA} = V_{IHA} or V_{ILA}		3.6	3.6	—	—	5	—	50	
			V_{INB} = V_{IHB} or V_{ILB}		3.6	5.5	—	—	8	—	80	

AC Characteristics (input: $t_r = t_f = 3$ ns, $C_L = 50$ pF, $R_L = 500 \ \Omega$, V_{CCA}=2.7 to 3.6 V)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
Propagation delay time	t_{pLH}	Input: An Output: Bn (DIR = "H")		5.0 ± 0.5	—	5.7	8.0	1.0	8.5	ns
(An → Bn)	t_{pHL}			3.3 ± 0.3	—	6.2	8.5	1.0	9.0	
3-state output enable time	t_{pZL}			5.0 ± 0.5	—	6.5	9.5	1.0	10.0	ns
($\overline{G}$ → Bn)	t_{pZH}			3.3 ± 0.3	—	7.4	10.5	1.0	11.5	
3-state output disable time	t_{pLZ}			5.0 ± 0.5	—	7.3	9.5	1.0	10.0	ns
($\overline{G}$ → Bn)	t_{pHZ}			3.3 ± 0.3	—	6.6	9.5	1.0	10.0	
Propagation delay time	t_{pLH}	Input: Bn Output: An (DIR = "L")		5.0 ± 0.5	—	4.6	7.5	1.0	8.0	ns
(Bn → An)	t_{pHL}			3.3 ± 0.3	—	5.2	7.5	1.0	8.0	
3-state output enable time	t_{pZL}			5.0 ± 0.5	—	7.0	10.5	1.0	11.5	ns
($\overline{G}$ → An)	t_{pZH}			3.3 ± 0.3	—	7.0	10.5	1.0	11.5	
3-state output disable time	t_{pLZ}			5.0 ± 0.5	—	6.1	9.5	1.0	10.0	ns
($\overline{G}$ → An)	t_{pHZ}			3.3 ± 0.3	—	6.0	9.5	1.0	10.0	
Output to output skew	t_{osLH}	(Note 1)		5.0 ± 0.5	—	—	1.5	—	1.5	ns
	t_{osHL}			3.3 ± 0.3	—	—	1.5	—	1.5	
Input capacitance	C_{INA}	DIR, $\overline{G}$		5.0 ± 0.5	—	5	10	—	10	pF
Bus input capacitance	$C_{I/O}$	An, Bn			—	8	—	—	—	
Power dissipation capacitance	C_{PDA}	A → B (DIR = "H")		5.0 ± 0.5	—	4	—	—	—	pF
		B → A (DIR = "L")			—	38	—	—	—	
(Note 2)	C_{PDB}	A → B (DIR = "H")		5.0 ± 0.5	—	88	—	—	—	
		B → A(DIR = "L")			—	7	—	—	—	

Note 1: Parameter guaranteed by design.
  ($t_{osLH} = |t_{pLHm} − t_{pLHn}|$, $t_{osHL} = |t_{pHLm} − t_{pHLn}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
  Average operating current can be obtained by the equation:
  $I_{CC \ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

Noise Characteristics (Ta = 25°C, input: t_r = t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω)

Characteristics		Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic	V_{OL} (A)	V_{OLPA}	Input: Bn Output: An (DIR = "L")	3.3	3.3	—	0.9	V
				3.3	5.0	—	0.9	
Quiet output mimimum dynamic	V_{OL} (A)	V_{OLVA}		3.3	3.3	—	−0.9	
				3.3	5.0	—	−0.9	
Quiet output maximum dynamic	V_{OL} (B)	V_{OLPB}	Input: An Output: Bn (DIR = "H")	3.3	3.3	—	0.8	
				3.3	5.0	—	1.5	
Quiet output mimimum dynamic	V_{OL} (B)	V_{OLVB}		3.3	3.3	—	−0.8	
				3.3	5.0	—	−1.2	
Minimum high level dynamic input voltage	V_{IH} (A)	V_{IHDA}	Input: An	3.3	3.3	—	2.0	V
				3.3	5.0	—	2.0	
Maximum low level dynamic input Voltage	V_{IL} (A)	V_{ILDA}	Input: An	3.3	3.3	—	0.8	V
				3.3	5.0	—	0.8	
Minimum high level dynamic input voltage	V_{IH} (B)	V_{IHDB}	Input: Bn	3.3	3.3	2.0	—	V
				3.3	5.0	3.5	—	
Maximum low level dynamic input voltage	V_{IL} (B)	V_{ILDB}	Input: Bn	3.3	3.3	0.8	—	V
				3.3	5.0	1.5	—	

Package Dimensions

SSOP24-P-300-0.65D   Unit: mm
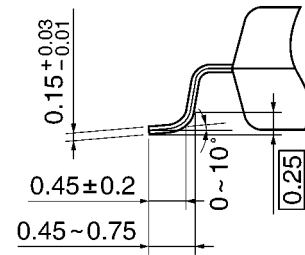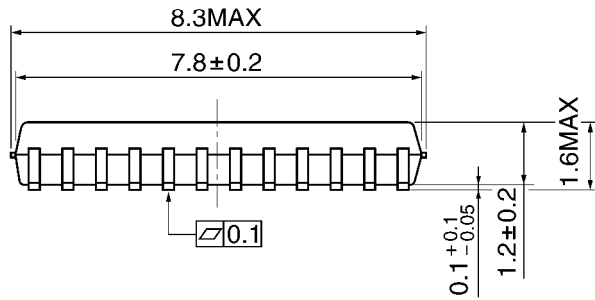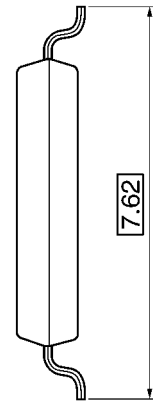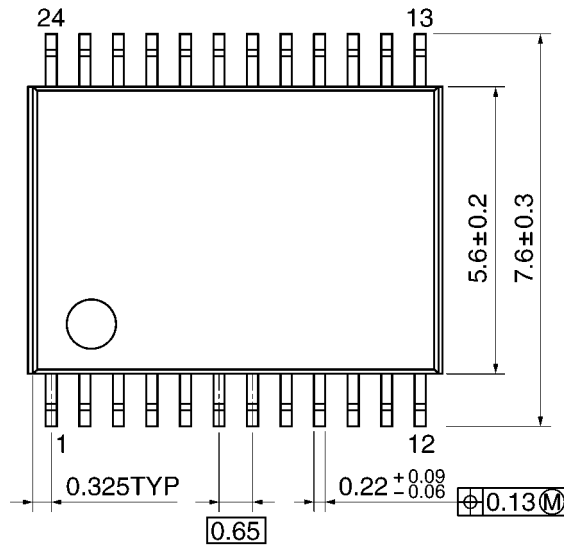
Weight: 0.14 g (typ.)

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