TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC299F, TC74VHC299FT

8-Bit PIPO Shift Register with Asynchronous Clear

The TC74VHC299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

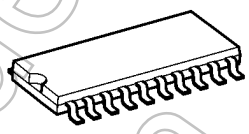
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G}1$, $\overline{G}2$) are high, the eight I/O are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

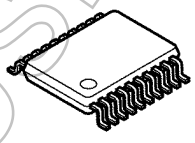
All inputs are equipped with protection circuits against static discharge.

TC74VHC299F



SOP20-P-300-1.27A

TC74VHC299FT



TSSOP20-P-0044-0.65A

Weight
SOP20-P-300-1.27A : 0.22 g (typ.)
TSSOP20-P-0044-0.65A : 0.08 g (typ.)

Features (Note 1) (Note 2) (Note 3)

- High speed: f_{max} = 160 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V
- Low noise: V_{OLP} = 1.2 V (max)
- Pin and function compatible with 74ALS299

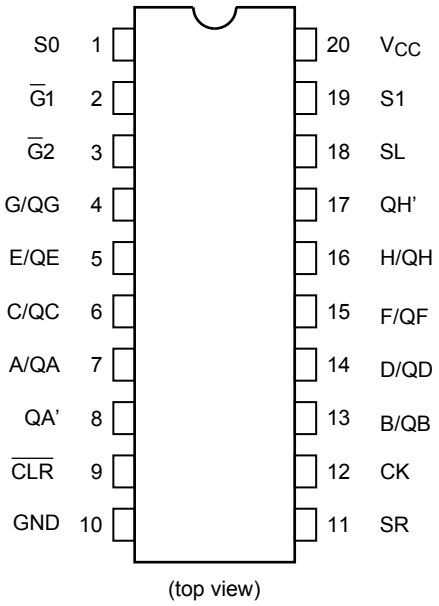
Note 1: Do not apply a signal to A/QA to H/QH bus terminal when it is in the output mode. Damage may result.

Note 2: All floating (high impedance) A/QA to H/QH bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Note 3: A parasitic diode is formed between A/QA to H/QH bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5 V to 3 V systems directly.

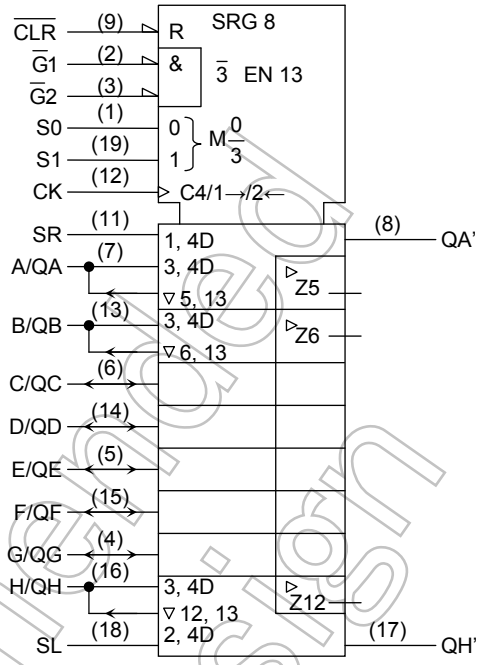
Start of commercial production
1992-10

Pin Assignment



(top view)

IEC Logic Symbol



Truth Table

Mode	Inputs								Inputs /Outputs		Outputs	
	$\overline{CLR}$	Function Select		Output Control		CK	Serial		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ (Note)	$\overline{G2}$ (Note)		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
Clear	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
Hold	H	L	L	L	L	X	X	X	QA_0	QH_0	QA_0	QH_0
Shift Right	H	L	H	L	L	↑	X	H	H	QG_n	H	QG_n
	H	L	H	L	L	↑	X	L	L	QG_n	L	QG_n
Shift Left	H	H	L	L	L	↑	H	X	QB_n	H	QB_n	H
	H	H	L	L	L	↑	L	X	QB_n	L	QB_n	L
Load	H	H	H	X	X	↑	X	X	a	h	a	h

Note: When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z: High impedance

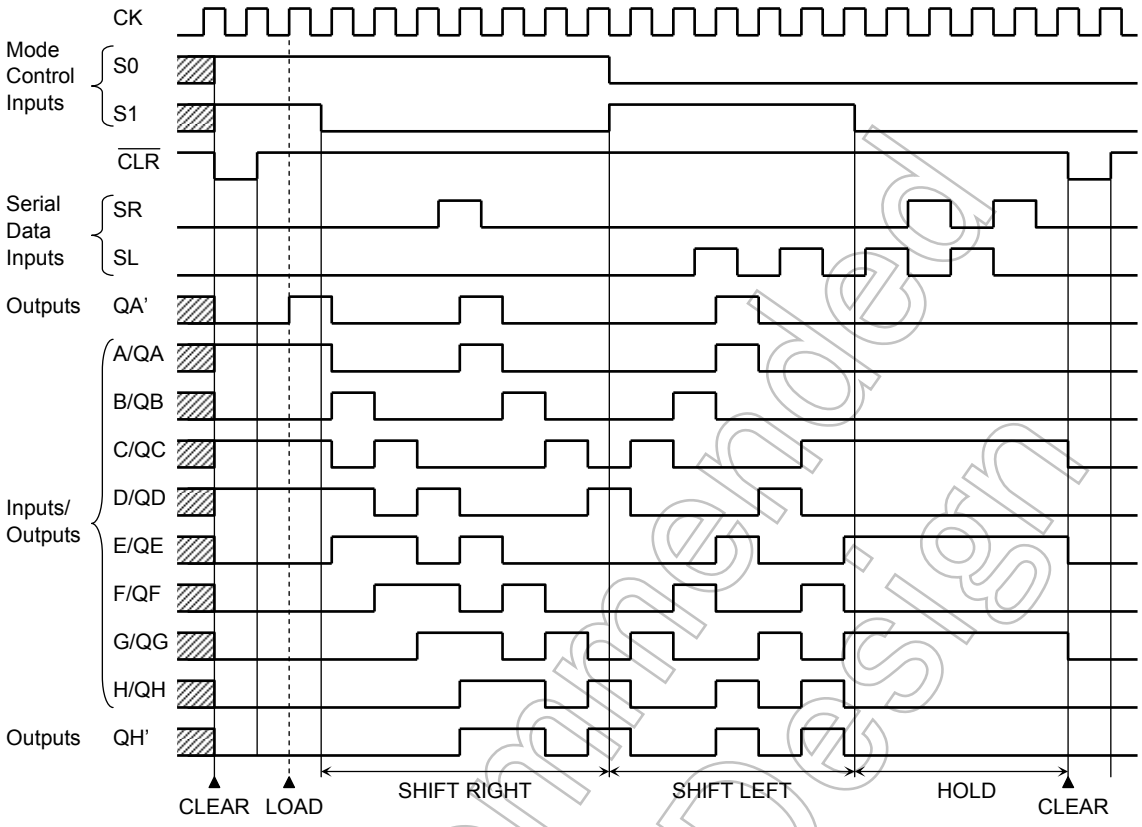
Q_{n0}: The level of Q_n before the indicated steady-state input conditions were established.

Q_{nn}: The level of Q_n before the most recent active transition indicated by ↓ or ↑.

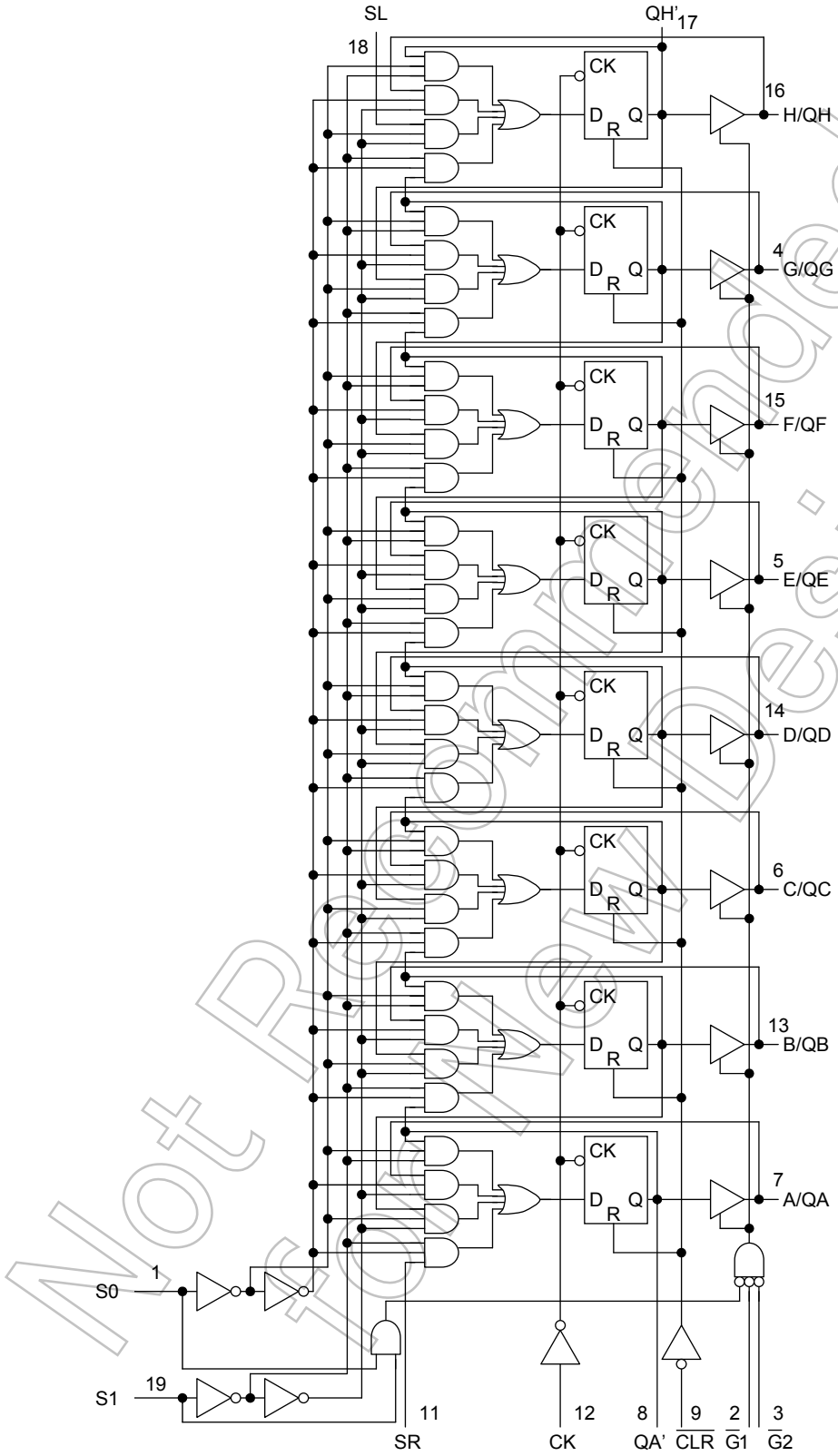
a, h: The level of the steady-state inputs A, H, respectively.

X: Don't care.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC bus I/O voltage (A/QA to H/QH')	$V_{IN/OUT}$	−0.5 to V_{CC} + 0.5	V
DC output voltage (QA' to QH')	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±80	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
DC bus I/O voltage (A/QA to H/QH)	$V_{IN/OUT}$	0 to V_{CC}	V
DC output voltage (QA' to QH')	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-QA', QH')	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	12.2	17.2	1.0	19.8	ns
				50	—	14.7	20.7	1.0	23.3	
			5.0 ± 0.5	15	—	8.5	10.8	1.0	12.0	
				50	—	10.0	12.8	1.0	14.0	
Propagation delay time ($\overline{CLR}$ -QA', QH')	t_{pHL}	—	3.3 ± 0.3	15	—	13.0	19.0	1.0	22.0	ns
				50	—	15.5	22.5	1.0	25.5	
			5.0 ± 0.5	15	—	9.1	11.2	1.0	13.5	
				50	—	10.8	13.2	1.0	15.5	
Propagation delay time (CK-QA to QH)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	10.3	14.3	1.0	16.6	ns
				50	—	12.8	17.8	1.0	20.1	
			5.0 ± 0.5	15	—	7.3	9.1	1.0	10.4	
				50	—	8.8	11.1	1.0	12.4	
Propagation delay time ($\overline{CLR}$ -QA to QH)	t_{pHL}	—	3.3 ± 0.3	15	—	10.8	17.0	1.0	19.5	ns
				50	—	13.3	20.5	1.0	23.0	
			5.0 ± 0.5	15	—	7.7	10.5	1.0	12.0	
				50	—	9.2	12.5	1.0	14.0	
Output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	3.3 ± 0.3	15	—	13.3	16.5	1.0	19.2	ns
				50	—	14.8	19.0	1.0	21.7	
			5.0 ± 0.5	15	—	8.9	9.7	1.0	11.3	
				50	—	10.4	11.2	1.0	12.6	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	3.3 ± 0.3	50	—	18.0	21.3	1.0	24.3	ns
			5.0 ± 0.5	50	—	11.8	13.2	1.0	15.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	65	100	—	55	—	MHz
				50	55	90	—	50	—	
			5.0 ± 0.5	15	125	160	—	110	—	
				50	115	150	—	100	—	
Input capacitance	C_{IN}	—			—	4	10	—	—	pF
Bus I/O capacitance (A/QA to H/QH)	C_{OUT}	—			—	8	—	—	—	pF
Power dissipation capacitance	C_{PD}			(Note)	—	110	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

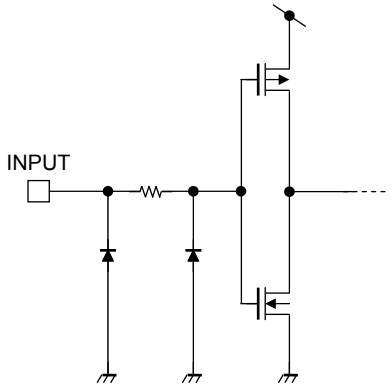
Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{w\,(H)}$	—	3.3 ± 0.3	—	7.0	8.0	ns
	$t_{w\,(L)}$		5.0 ± 0.5	—	7.0	8.0	
Minimum pulse width ($\overline{CLR}$)	$t_{w\,(L)}$	—	3.3 ± 0.3	—	6.0	7.0	ns
			5.0 ± 0.5	—	6.0	7.0	
Minimum set-up time (SL, SR)	t_s	—	3.3 ± 0.3	—	8.5	10.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time (A to H)	t_s	—	3.3 ± 0.3	—	8.0	9.0	ns
			5.0 ± 0.5	—	4.0	4.0	
Minimum set-up time (S0, S1)	t_s	—	3.3 ± 0.3	—	14.5	17.0	ns
			5.0 ± 0.5	—	7.0	8.0	
Minimum hold time (SL, SR)	t_h	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.0	1.0	
Minimum hold time (A to H)	t_h	—	3.3 ± 0.3	—	0.5	0.5	ns
			5.0 ± 0.5	—	1.5	1.5	
Minimum hold time (S0, S1)	t_h	—	3.3 ± 0.3	—	0	0	ns
			5.0 ± 0.5	—	0.5	0.5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	3.3 ± 0.3	—	5.0	6.0	ns
			5.0 ± 0.5	—	4.0	4.0	

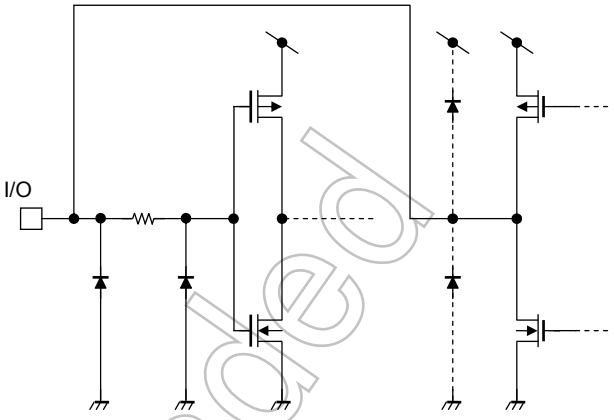
Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.9	1.2	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.9	−1.2	V
Minimum high level dynamic input Voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low high level dynamic input Voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit

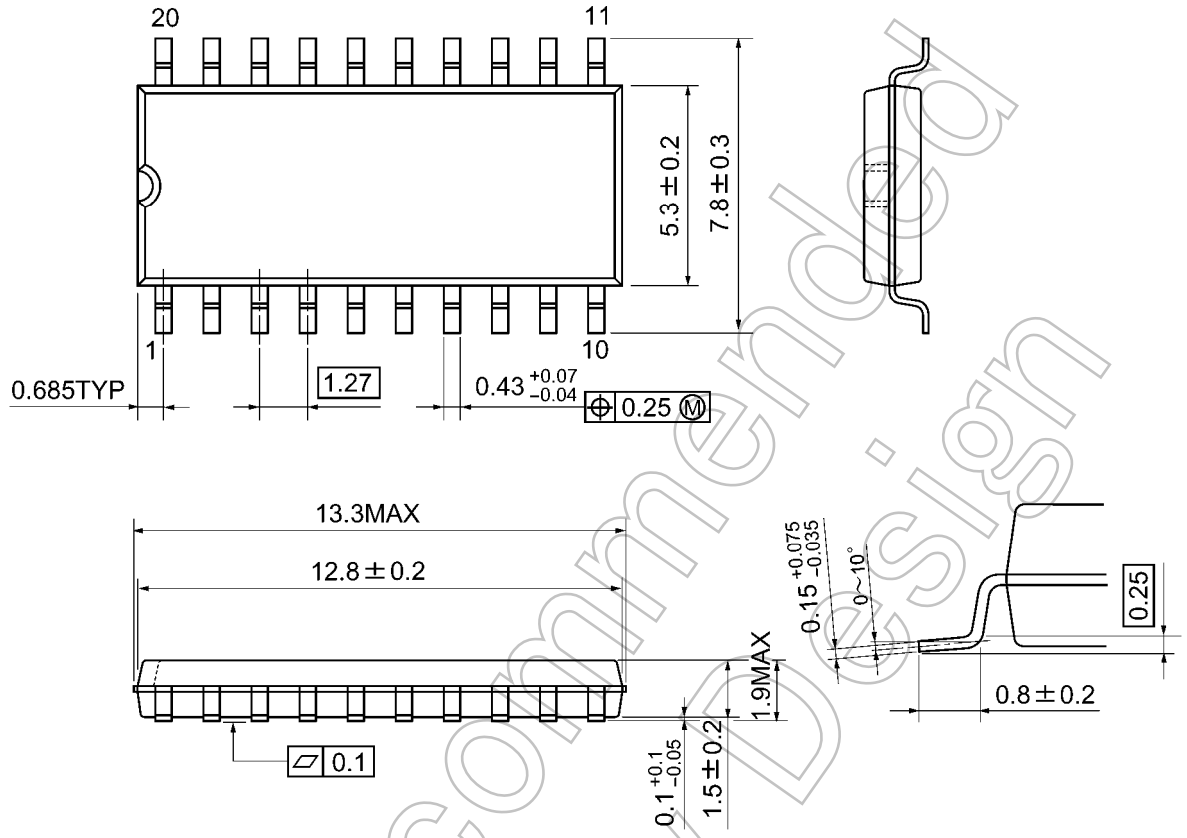


A/QA to H/QH Bus Terminal Equivalent Circuit



Package Dimensions

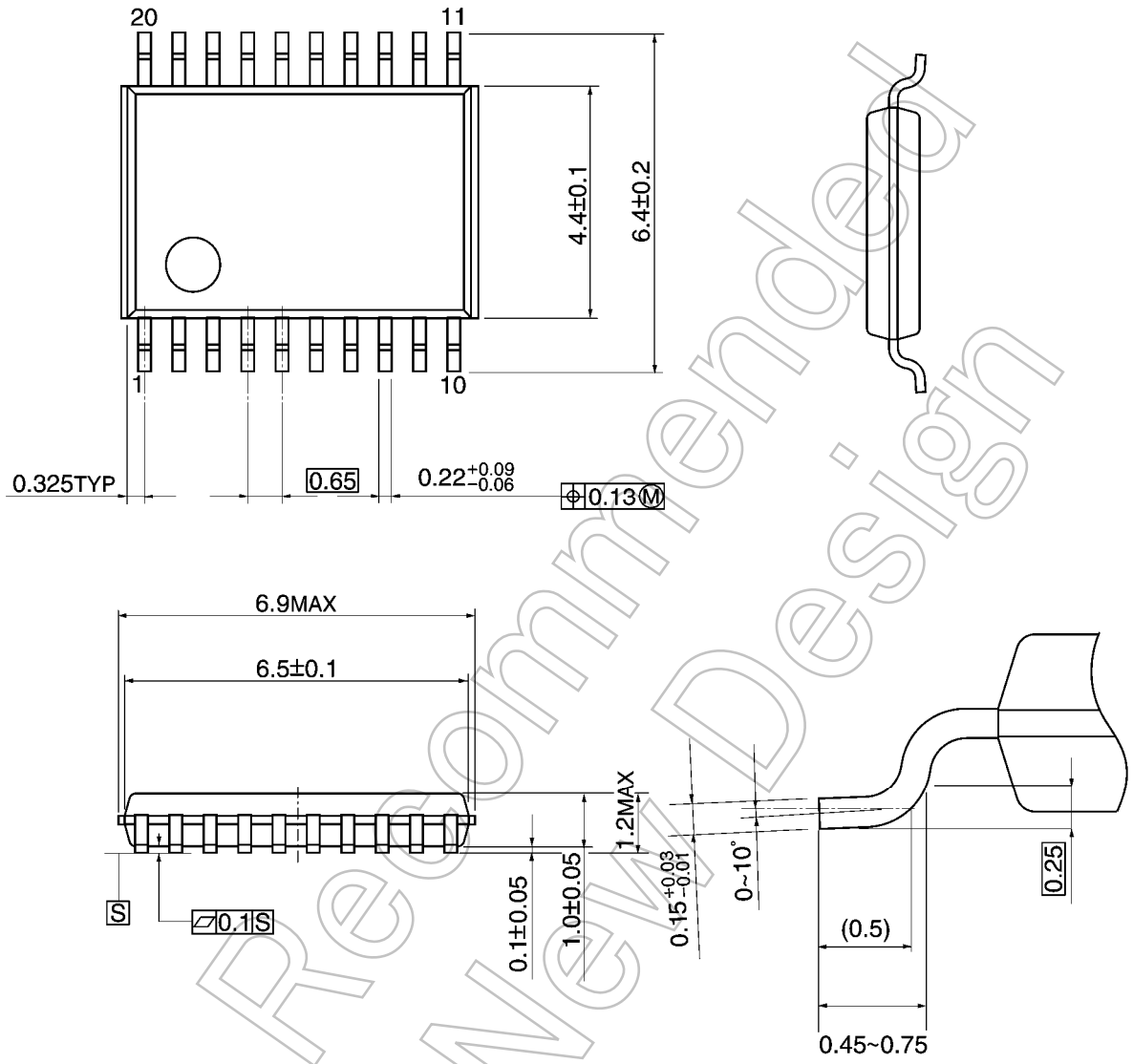
SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm



Weight: 0.08 g (typ.)

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