

TC74VHC393F, TC74VHC393FT, TC74VHC393FK

Dual Binary Counter

The TC74VHC393 is an advanced high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

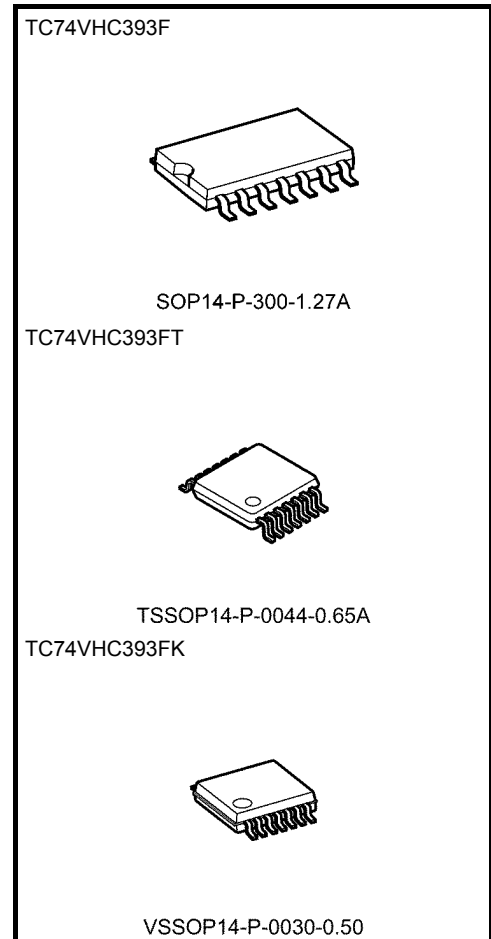
It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the $\overline{\text{CLOCK}}$ pulse. The counter can be reset to "0" (QA to QD = "L") by a high at the CLEAR input regardless of other inputs.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

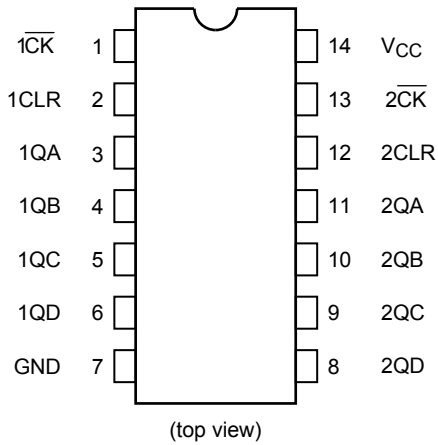
- High speed: $f_{\text{max}} = 170 \text{ MHz}$ (typ.) at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: $V_{\text{CC (opr)}} = 2 \text{ to } 5.5 \text{ V}$
- Low noise: $V_{\text{OLP}} = 0.8 \text{ V}$ (max)
- Pin and function compatible with 74ALS393



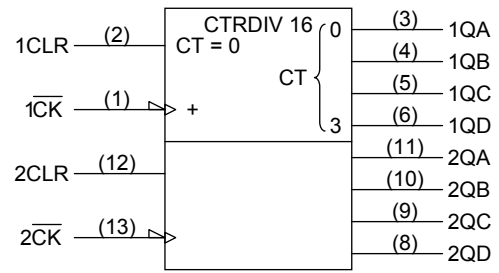
Weight	
SOP14-P-300-1.27A	: 0.18 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

Start of commercial production
1991-11

Pin Assignment



IEC Logic Symbol

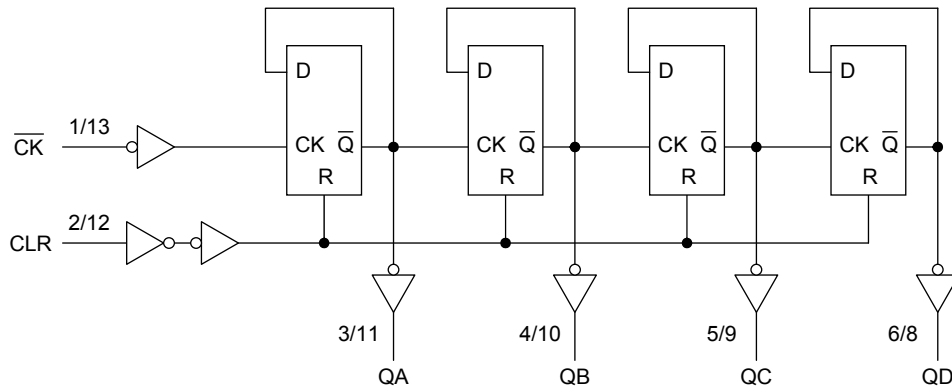


Truth Table

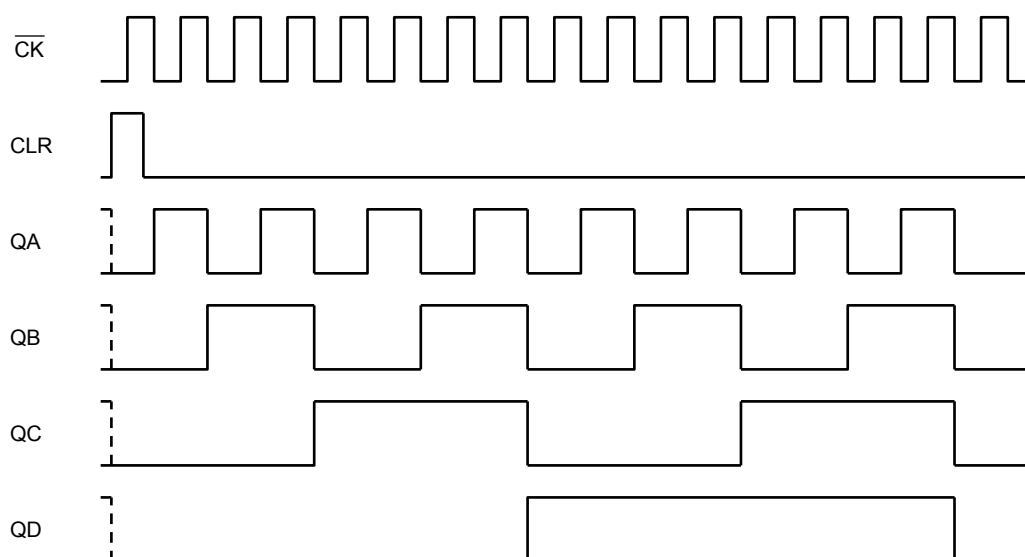
Inputs		Outputs			
\overline{CK}	CLR	QA	QB	QC	QD
X	H	L	L	L	L
	L	Count Up			
	L	No Change			

X: Don't care

System Diagram



Timing Chart



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	V_{IH}	—	2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V	
Low-level input voltage	V_{IL}	—	2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			$I_{OH} = -4 \text{ mA}$	3.0	2.58	—	—	2.48	—	
			$I_{OH} = -8 \text{ mA}$	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$I_{OL} = 4 \text{ mA}$	3.0	—	—	0.36	—	0.44	
			$I_{OL} = 8 \text{ mA}$	4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V or GND}$	0 to 5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				Typ.	Limit	Limit		
Minimum pulse width (CK)	$t_w (H)$	—		3.3 ± 0.3	—	5.0	5.0	ns
	$t_w (L)$			5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width (CLR)	$t_w (H)$	—		3.3 ± 0.3	—	5.0	5.0	ns
				5.0 ± 0.5	—	5.0	5.0	
Minimum removal time	t_{rem}	—		3.3 ± 0.3	—	5.0	5.0	ns
				5.0 ± 0.5	—	4.0	4.0	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min		Max
Propagation delay time ($\overline{CK} - Q_A$)	t_{pLH}	—	3.3 ± 0.3	15	—	8.6	13.2	1.0	15.5	ns
				50	—	11.1	16.7	1.0	19.0	
	t_{pHL}		5.0 ± 0.5	15	—	5.8	8.5	1.0	10.0	
				50	—	7.3	10.5	1.0	12.0	
Propagation delay time ($\overline{CK} - Q_B$)	t_{pLH}	—	3.3 ± 0.3	15	—	10.2	15.8	1.0	18.5	ns
				50	—	12.7	19.3	1.0	22.0	
	t_{pHL}		5.0 ± 0.5	15	—	6.8	9.8	1.0	11.5	
				50	—	8.3	11.8	1.0	13.5	
Propagation delay time ($\overline{CK} - Q_C$)	t_{pLH}	—	3.3 ± 0.3	15	—	11.7	18.0	1.0	21.0	ns
				50	—	14.2	21.5	1.0	24.5	
	t_{pHL}		5.0 ± 0.5	15	—	7.7	11.2	1.0	13.0	
				50	—	9.2	13.2	1.0	15.0	
Propagation delay time ($\overline{CK} - Q_D$)	t_{pLH}	—	3.3 ± 0.3	15	—	13.0	19.7	1.0	23.0	ns
				50	—	15.5	23.2	1.0	26.5	
	t_{pHL}		5.0 ± 0.5	15	—	8.5	12.5	1.0	14.5	
				50	—	10.0	14.5	1.0	16.5	
Propagation delay time (CLR-Q _n)	t_{pHL}	—	3.3 ± 0.3	15	—	7.9	12.3	1.0	14.5	ns
				50	—	10.4	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	5.4	8.1	1.0	9.5	
				50	—	6.9	10.1	1.0	11.5	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	75	120	—	65	—	MHz
				50	45	65	—	35	—	
			5.0 ± 0.5	15	125	170	—	105	—	
				50	85	115	—	75	—	
Input capacitance	C _{IN}	—		—	4	10	—	10	pF	
Power dissipation capacitance	C _{PD}	(Note)		—	23	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

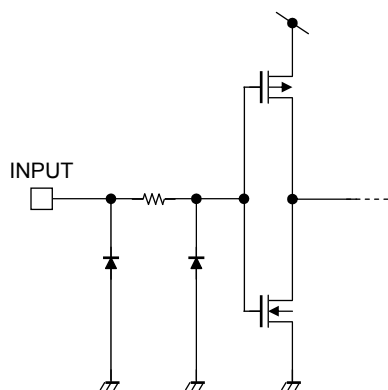
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per counter)}$$

Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V _{CC} (V)	Typ.	Max	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.5	-0.8	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5	V

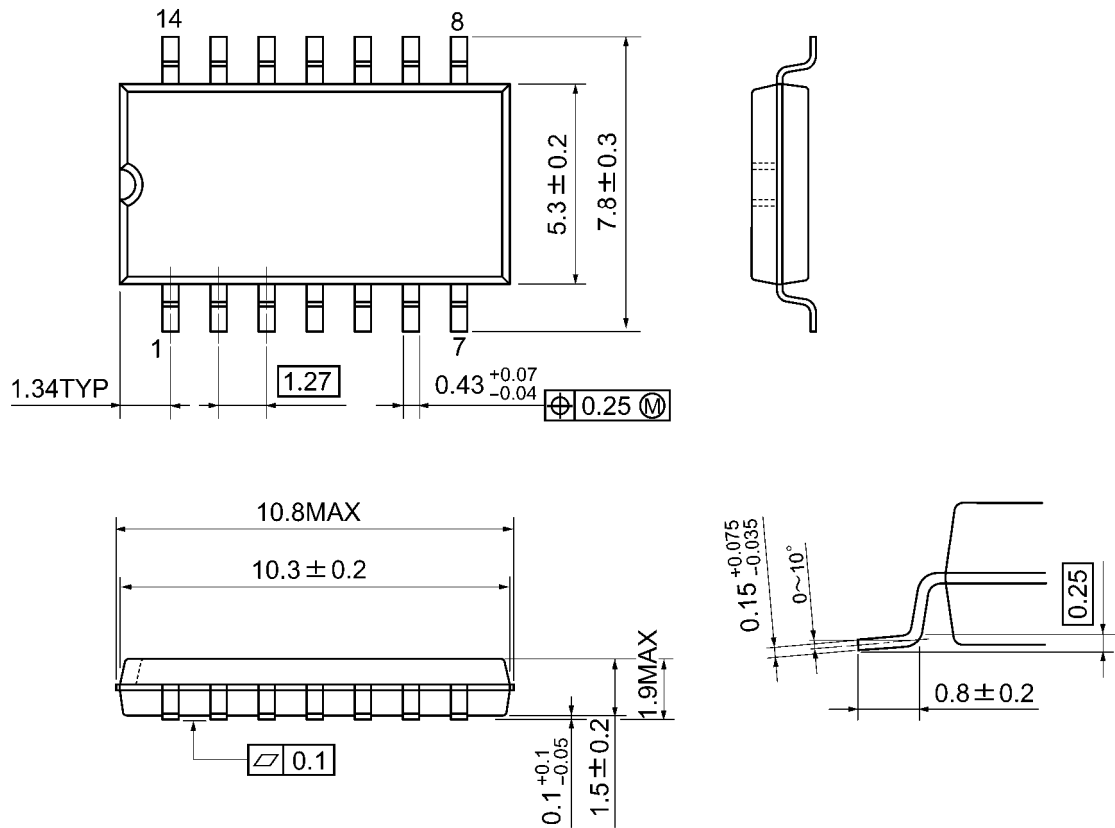
Input Equivalent Circuit



Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm

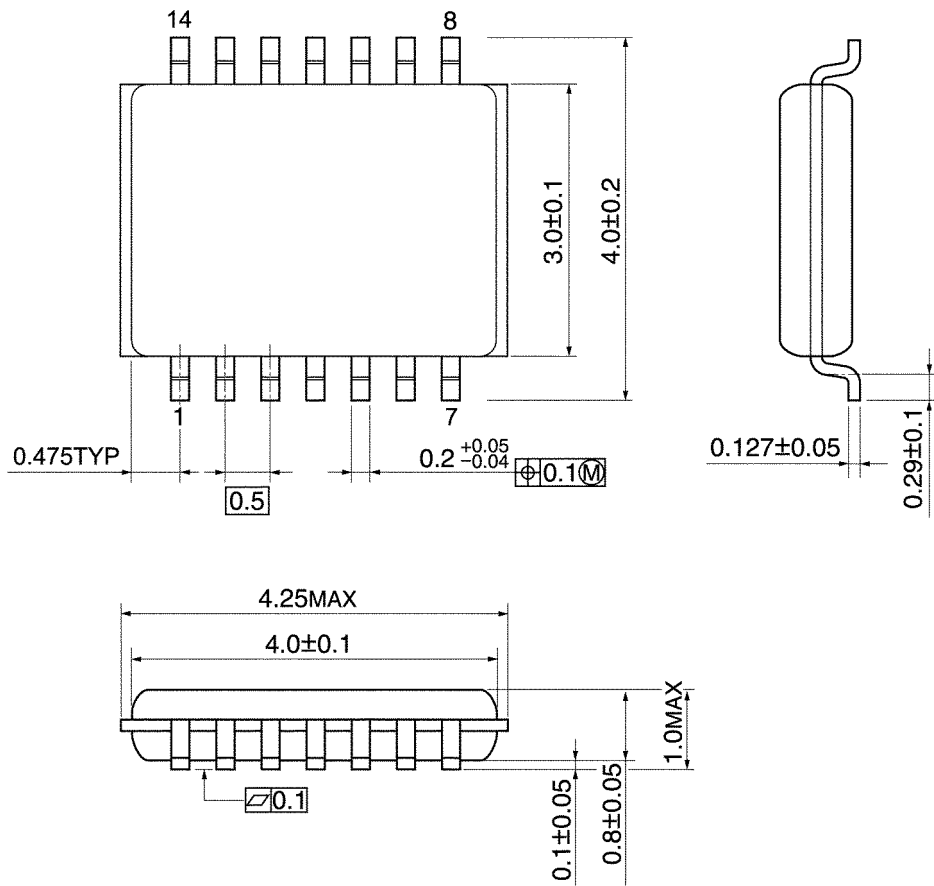


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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