

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHCT125AF, TC74VHCT125AFN, TC74VHCT125AFT
TC74VHCT126AF, TC74VHCT126AFN, TC74VHCT126AFT

TC74VHCT125AF / AFN / AFT QUAD BUS BUFFER
TC74VHCT126AF / AFN / AFT QUAD BUS BUFFER

(Note) : The JEDEC SOP (FN) is not available in Japan.

The TC74VHCT125A / 126A are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The TC74VHCT125A requires the 3-state control input \bar{G} to be set high to place the output into the high impedance state, whereas the TC74VHCT126A requires the control input G to be set low to place the output into high impedance.

The input voltage are compatible with TTL output voltage. This device may be used as a level converter for interfacing 3.3 V to 5 V system.

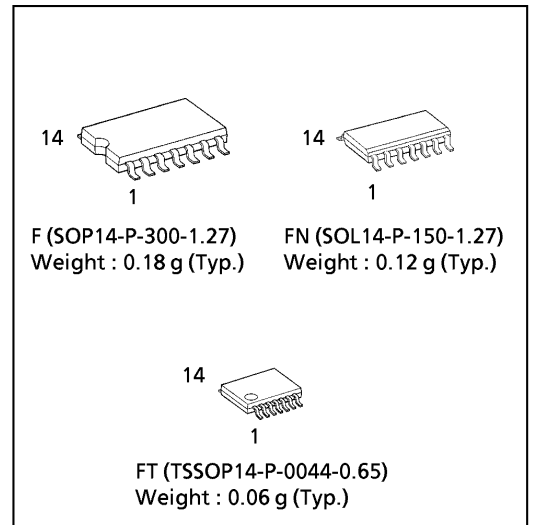
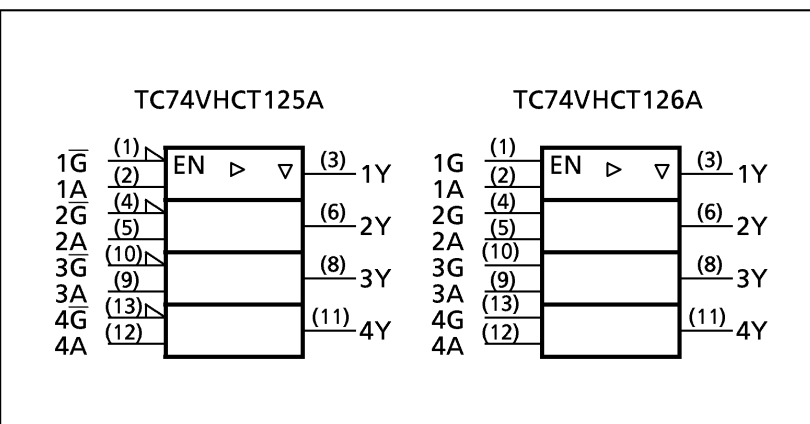
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

*1: V_{cc} = 0 V

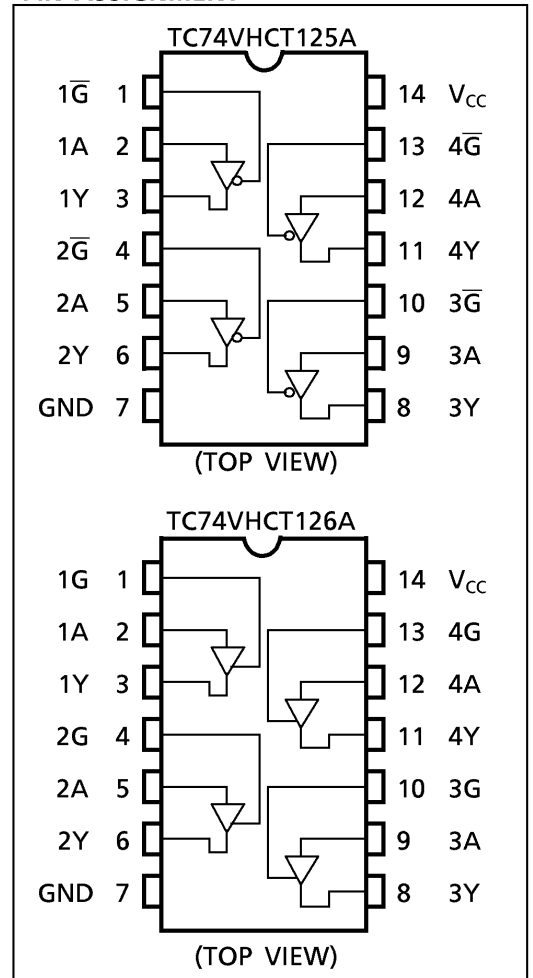
FEATURES:

- High Speed.....t_{pd} = 3.8 ns (typ.) at V_{CC} = 5 V
- Low Power Dissipation.....I_{CC} = 4 μA (Max.) at T_a = 25°C
- Compatible with TTL outputs....V_{IL} = 0.8 V (Max.)
V_{IH} = 2.0 V (Min.)
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays.....t_{pLH} ≈ t_{pHL}
- Low NoiseV_{OLP} = 0.8 V (Max.)
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 125 / 126 type.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



TRUTH TABLE

TC74VHCT125A			TC74VHCT126A		
INPUTS		OUTPUTS	INPUTS		OUTPUTS
\bar{G}	A	Y	G	A	Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

X: Don't Care
Z: High Impedance

X: Don't Care
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~7.0 (Note 1)	V
		-0.5 ~ V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20 (Note 3)	mA
DC Output Current	I_{OUT}	±25	mA
DC Vcc/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

(Note 1) : Output in Off-State

(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 4)	V
		0~ V_{CC} (Note 5)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~20	ns/V

(Note 4) : Output in Off-State

(Note 5) : High or Low State

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		4.5~5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V_{IL}		4.5~5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	4.5	4.40	4.50	—	4.40	—	V
			$I_{OH} = -8 \text{ mA}$	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 8 \text{ mA}$	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5 \text{ V}$ or GND	0~5.5	—	—	± 0.1	—	± 1.0	μA	
3-State Output Off-state Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.25	—	± 2.50		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0		
	I_{CCT}	PER INPUT : $V_{IN} = 3.4 \text{ V}$ OTHER INPUT : V_{CC} or GND	5.5	—	—	1.35	—	1.50	mA	
Output Leakage Current	I_{OPD}	$V_{OUT} = 5.5 \text{ V}$	0	—	—	0.5	—	5.0	μA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH}	5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	ns
	t _{pHL}		50	—	5.3	7.5	1.0	8.5	
Output Enable Time	t _{pZL}	RL = 1 kΩ	15	—	3.6	5.1	1.0	6.0	
	t _{pZH}		50	—	5.1	7.1	1.0	8.0	
Output Disable Time	t _{pLZ}	RL = 1 kΩ	5.0 ± 0.5	50	—	6.1	8.8	1.0	
	t _{pHZ}		5.0 ± 0.5	50	—	6.1	8.8	1.0	10.0
Output to Output Skew	t _{osLH} t _{osHL}	(Note 6)	5.0 ± 0.5	50	—	—	1.0	—	1.0
Input Capacitance	C _{IN}			—	4	10	—	10	pF
Output Capacitance	C _{OUT}			—	6	—	—	—	
Power Dissipation Capacitance (Note 7)	C _{PD}	TC74VHCT125A		—	14	—	—	—	
		TC74VHCT126A		—	15	—	—	—	

(Note 6) : Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 7) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

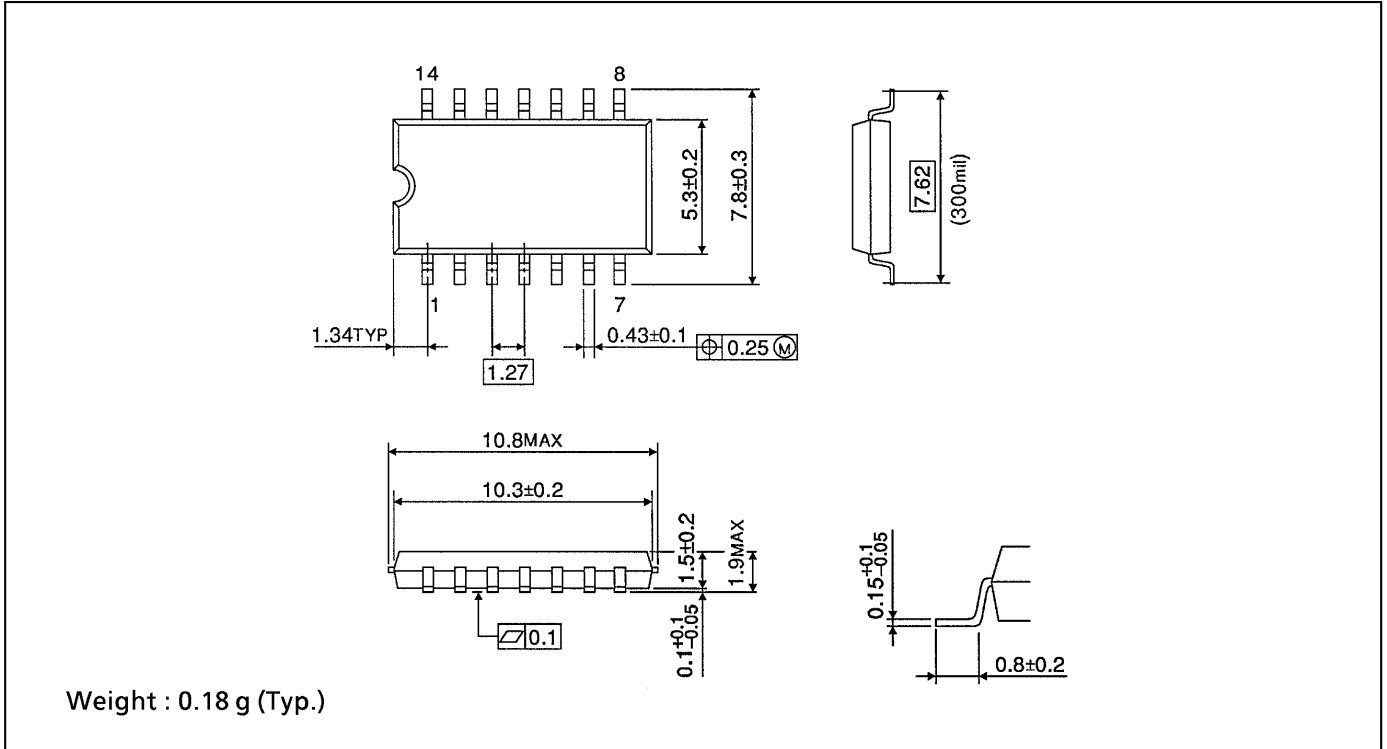
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
		V _{CC} (V)		TYP.	LIMIT	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.5	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50 pF	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50 pF	5.0	—	0.8	V

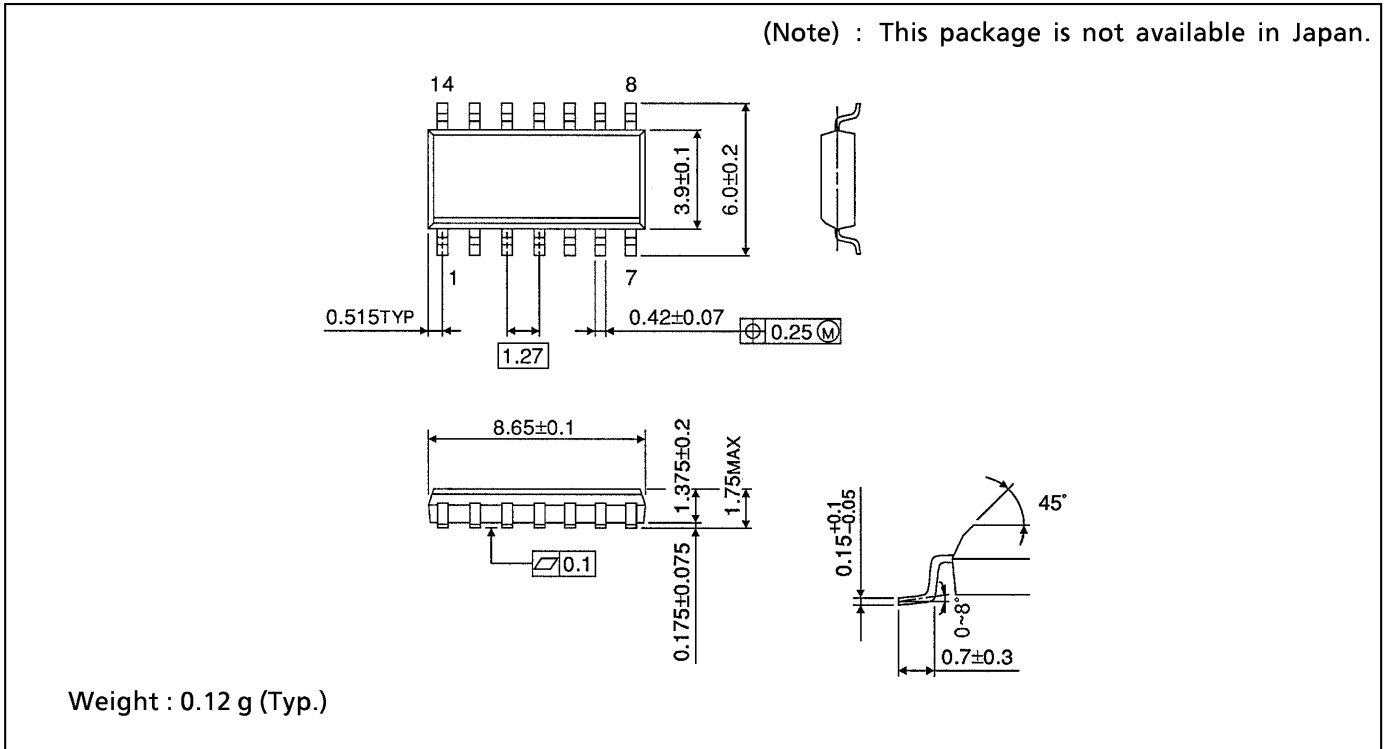
SOP 14 PIN (200 mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm



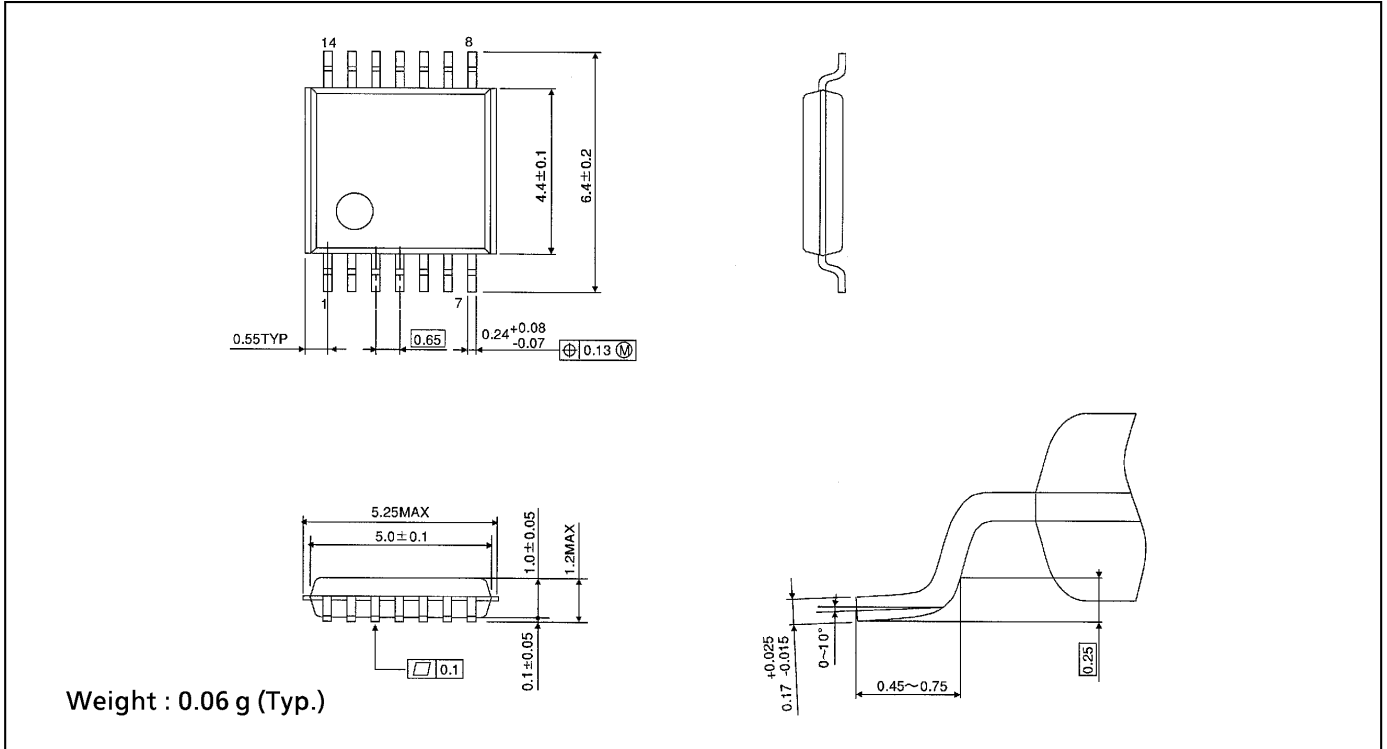
SOP 14 PIN (150 mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)

Unit in mm



TSSOP 14 PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm



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