

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S51F, TC75S51FU

Single Operational Amplifier

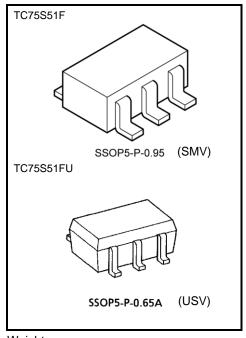
The TC75S51F/TC75S51FU is a CMOS single-operation amplifier which incorporates a phase compensation circuit. It is designed with a low-voltage and low-current power supply; this differentiates this device from general-purpose bipolar op-amps.

Features

- Low-voltage operation : $V_{DD} = \pm 0.75$ to ± 3.5 V or 1.5 to 7 V
- Low-current power supply : IDD (VDD = 3 V) = $60 \mu \text{A}$ (typ.)
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-compact package



Characteristics	Symbol	Rating	Unit
Supply voltage	V _{DD} , V _{SS}	7	V
Differential input voltage	DVIN	±7	V
Input voltage	VIN	V _{DD} to V _{SS}	V
Power dissipation	PD	200	mW
Operating temperature	T _{opr}	-40 to 85	°C
Storage temperature	T _{stg}	-55 to 125	°C



Weight

SSOP5-P-0.95 : 0.014 g (typ.) SSOP5-P-0.65A : 0.006 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

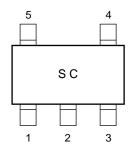
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

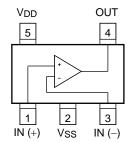
Start of commercial production 1993-07



Marking (top view)

Pin Connection (top view)





Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	Vio	1	$R_S = 1 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	_	2	10	mV
Input offset current	lio	_	_	_	1	_	pА
Input bias current	lį	_	_	_	1	_	pА
Common mode input voltage	CMVIN	2	$R_S = 1 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	0	_	2.5	V
Voltage gain (open loop)	Gv	_	_	60	70	_	dB
Maximum output voltage	Voн	3	R _L ≥ 100 kΩ	2.9	_	_	V
	VoL	4	R _L ≥ 100 kΩ	_	_	0.1	V
Common mode input signal rejection ratio	CMRR	2	V _{IN} = 0.0 to 2.5 V	55	65	_	dB
Supply voltage rejection ratio	SVRR	1	V _{DD} = 1.5 to 7.0 V	60	70	_	dB
Supply current	IDD	5	_	_	60	200	μА

DC Characteristics (V_{DD} = 1.5 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	VIO	1	$R_S = 10 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	_	2	10	mV
Input offset current	lio	_	_	_	1	_	pА
Input bias current	lį	_	_	_	1	_	pА
Common mode input voltage	CMVIN	2	$R_S = 10 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	0	_	1.0	V
Voltage gain (open loop)	G _V	_	_	60	70	_	dB
Maximum output voltage	Voн	3	R _L ≥ 100 kΩ	1.4	_	_	V
	VoL	4	R _L ≥ 100 kΩ	_	_	0.1	V
Supply current	I _{DD}	5	_	_	50	150	μΑ

Note: For this device, please use a source current of no more than 70 $\ensuremath{\mu A}.$



AC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

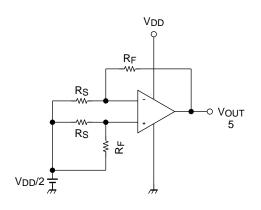
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	$A_V = 0 dB$	_	0.5	_	V/μs
Unity gain cross frequency	fΤ	_	A _V = 40 dB	_	0.6	_	MHz

AC Characteristics (V_{DD} = 1.5 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	Av = 0 dB	_	0.3	_	V/μs
Unity gain cross frequency	f⊤	_	Av = 40 dB	_	0.5	_	MHz

Test Circuit

1. SVRR, Vio



SVRR

For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.

When $V_{DD} = 1.5 \text{ V}$, $V_{DD} = V_{DD}1$ and $V_{OUT} = V_{OUT}1$ When $V_{DD} = 7.0 \text{ V}$, $V_{DD} = V_{DD}2$ and $V_{OUT} = V_{OUT}2$

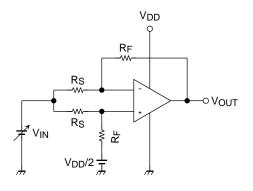
$$SVRR = 20 log \left(\frac{|V_{OUT}1 - V_{OUT}2|}{V_{DD}1 - V_{DD}2} | \times \frac{R_S}{R_F + R_S} \right)$$

Vio

Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMVIN



CMRR

Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.

When $V_{IN} = 0.0 \text{ V}$, $V_{IN} = V_{IN}1$ and $V_{OUT} = V_{OUT}1$ When $V_{IN} = 2.5 \text{ V}$, $V_{IN} = V_{IN}2$ and $V_{OUT} = V_{OUT}2$

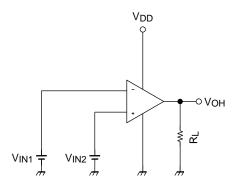
$$CMRR = 20 \log \left(\frac{|V_{OUT}1 - V_{OUT}2|}{|V_{IN}1 - V_{IN}2|} \times \frac{R_S}{R_F + R_S} \right)$$

CMV_{IN}

Input range within which the CMRR specification guarantees $V_{\mbox{\scriptsize OUT}}$ value (as varied by the $V_{\mbox{\scriptsize IN}}$ value).



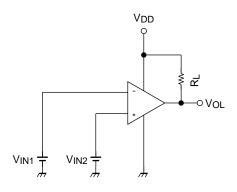
3. Vон



$$V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

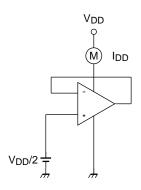
$$V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

4. Vol

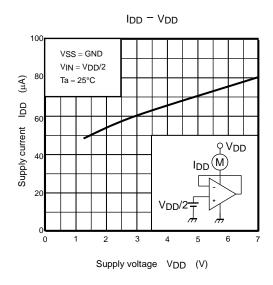


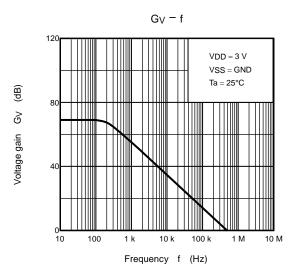
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$
$$V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

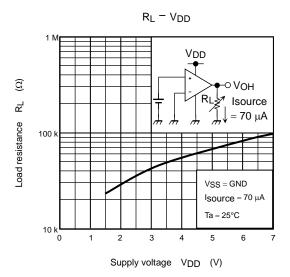
5. IDD

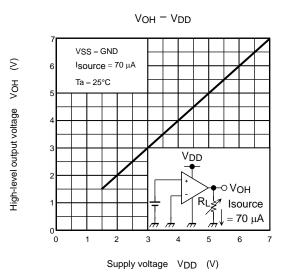






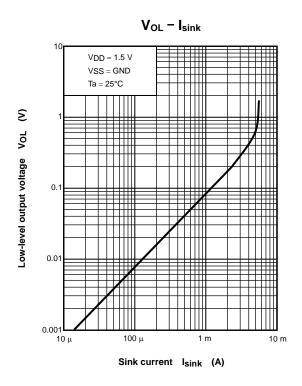


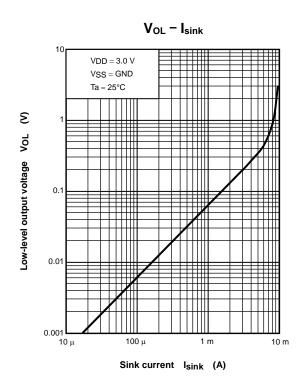


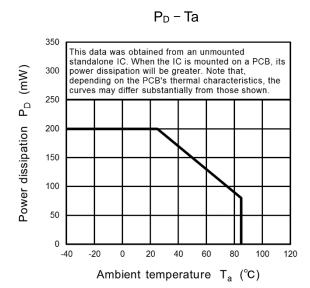


The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.







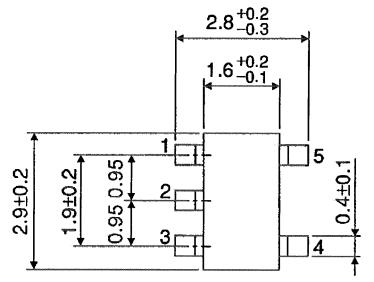


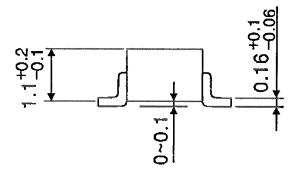
The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

SSOP5-P-0.95 Unit: mm



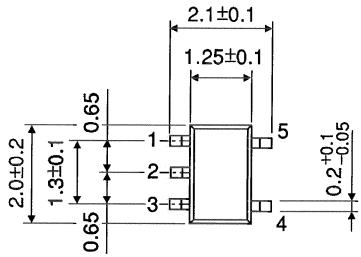


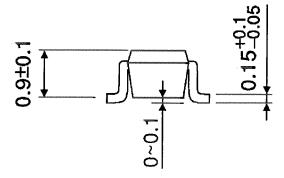
Weight: 0.014 g (typ.)



Package Dimensions

SSOP5-P-0.65A Unit: mm





Weight: 0.006 g (typ.)



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