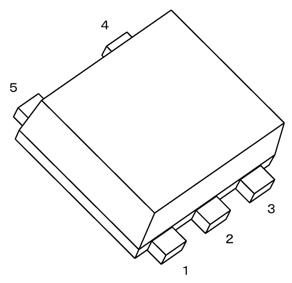
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

# TC75S63TU

Single Operational Amplifier (Low Noise Operational Amplifier)




Weight: 7m g (typ.)

## Features

- Low Noise. $V_{NI}$ = 7.8nV/√Hz (typ.) @ $V_{DD}$ = 3.3 V
- Small Phase Delay. -2.5 degrees @$V_{DD}$ = 3.3 V (typ.), f = 2kHz
- Low-current supply. 500μA @ $V_{DD}$ = 3.3 V (typ.)
- Ultra-compact package.

## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{SS}$ | 6 | V |
| Differential input voltage | $DV_{IN}$ | ±6 | V |
| Input voltage | $V_{IN}$ | $V_{DD}$ to $V_{SS}$ | V |
| Output current | $I_{OUT}$ | ±4 | mA |
| Power dissipation | $P_D$ | 450(Note1) | mW |
| Operating temperature | $T_{opr}$ | –40 to 85 | °C |
| Storage temperature | $T_{stg}$ | –55 to 125 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on a glass epoxy circuit board of 30 mm × 30 mm. Pad dimension of 35mm$^2$

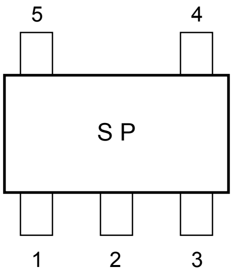
## Operating Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{SS}$ | 2.2 to 5.5 | V |

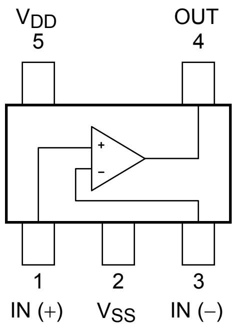
Note2: Do not use this product in a voltage follower circuit or outside the range of the common mode input voltage. (For the common mode input voltage, see DC Characteristics on Page 2). Failure to follow this instruction may cause voltage oscillation.
A higher load capacitance will increase the risk of voltage oscillation, even if this product is used within the range of the common mode input voltage. Allow sufficient capacitance value margin when designing your circuit and using this product to prevent voltage oscillation.

Start of commercial production
2009-09

## Marking (top view)




## Pin Connection (top view)




## Electrical Characteristics

### DC Characteristics ($V_{DD}$ = 3.3 V, $V_{SS}$ = GND, Ta = 25°C)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | 1 | $R_S$ = 1 kΩ, $R_F$ = 100 kΩ | – | 1 | 7 | mV |
| Input offset current | $I_{IO}$ | – | – | – | 1 | – | pA |
| Input bias current | $I_I$ | – | – | – | 1 | – | pA |
| Common mode input voltage | $CMV_{IN}$ | 2 | $R_S$ = 1 kΩ, $R_F$ = 100 kΩ | 0 | – | 2.4 | V |
| Voltage gain (open loop) | $G_V$ | – | – | – | 100 | – | dB |
| Maximum output voltage | $V_{OH}$ | 3 | $R_L$ ≥ 100 kΩ | 3.2 | – | – | V |
| | $V_{OL}$ | 4 | $R_L$ ≥ 100 kΩ | – | – | 0.1 | |
| Common mode input signal rejection ratio | CMRR | 2 | $V_{IN}$ = 0 to 2.4 V | 60 | 80 | – | dB |
| Supply voltage rejection ratio | SVRR | 1 | $V_{DD}$ = 2.2 to 5.5 V | 60 | 80 | – | dB |
| Supply current | $I_{DD}$ | 5 | – | – | 500 | 650 | μA |
| Source current | Isource | 6 | – | 1500 | – | – | μA |
| Sink current | Isink | 7 | – | 1500 | – | – | μA |

### AC Characteristics ($V_{DD}$ = 3.3 V, $V_{SS}$ = GND, Ta = 25°C)

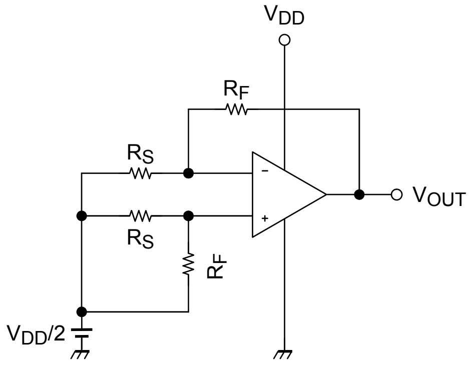
| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Equivalent input Noise Voltage | $V_{NI}$ | – | f = 1 kHz, $G_V$ = 40 dB, RS = 100 Ω, Rf = 10 kΩ | – | 7.8 | – | nV/√Hz |
| Unity Gain Cross Frequency | $f_T$ | – | $G_V$ = 40 dB | – | 3.5 | – | MHz |
| Phase delay | $\phi_D$ | 8 | f = 2 kHz | – | -2.5 | – | degrees |

### AC Characteristics ($V_{DD}$ = 1.65 V, $V_{SS}$ = -1.65V, Ta = 25°C)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Slew Rate | SR | 9 | $G_V$ = 12 dB, $V_{IN}$ = 0.4 V | – | 1.0 | – | V/μs |

## Test Circuit

### 1. SVRR, $V_{IO}$



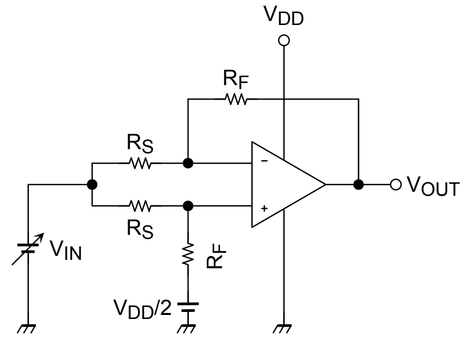

- SVRR
- For each of the two $V_{DD}$ values, measure the $V_{OUT}$ value, as indicated below, and calculate the value of SVRR using the equation shown.
  When $V_{DD} = 2.2$ V, $V_{DD} = V_{DD}1$ and $V_{OUT} = V_{OUT}1$
  When $V_{DD} = 5.5$ V, $V_{DD} = V_{DD}2$ and $V_{OUT} = V_{OUT}2$

$$\mathrm{SVRR} = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- $V_{IO}$
  Measure the value of $V_{OUT}$ and calculate the value of $V_{IO}$ using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

### 2. CMRR, $CMV_{IN}$

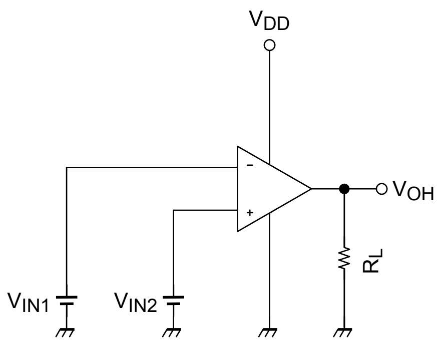



- CMRR
  Measure the $V_{OUT}$ value, as indicated below, and calculate the value of the CMRR using the equation shown.
  When $V_{IN} = 0$ V, $V_{IN} = V_{IN}1$ and $V_{OUT} = V_{OUT}1$
  When $V_{IN} = 2.4$ V, $V_{IN} = V_{IN}2$ and $V_{OUT} = V_{OUT}2$

$$\mathrm{CMRR} = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- $CMV_{IN}$
  Input range within which the CMRR specification guarantees $V_{OUT}$ value (as varied by the $V_{IN}$ value).

### 3. $V_{OH}$

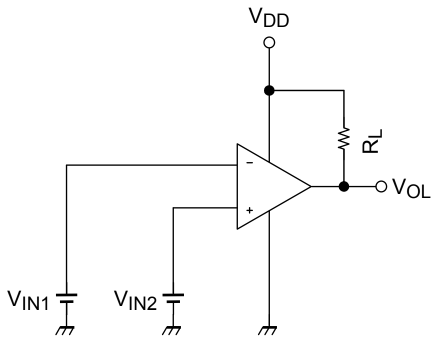



- $V_{OH}$

$$V_{IN}1 = \frac{V_{DD}}{2} - 0.05\ \mathrm{V}$$

$$V_{IN}2 = \frac{V_{DD}}{2} + 0.05\ \mathrm{V}$$

### 4. $V_{OL}$

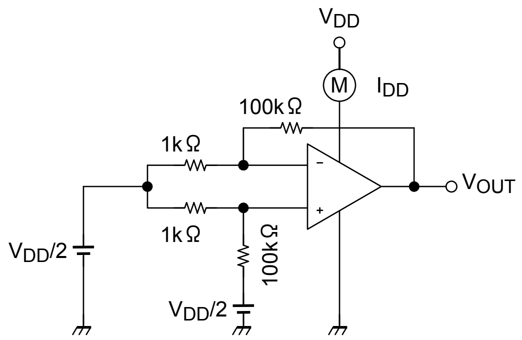



- $V_{OL}$

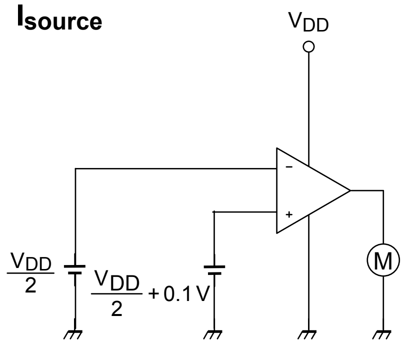
$$V_{IN}1 = \frac{V_{DD}}{2} + 0.05\ \mathrm{V}$$

$$V_{IN}2 = \frac{V_{DD}}{2} - 0.05\ \mathrm{V}$$

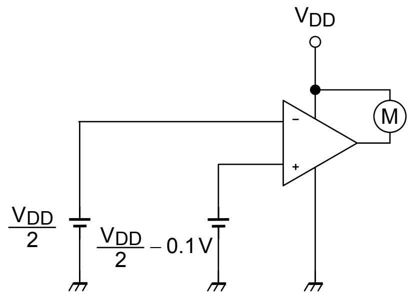
**5. $I_{DD}$**



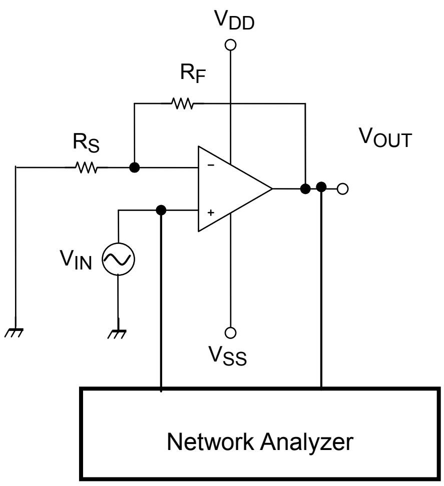

**6. $I_{source}$**

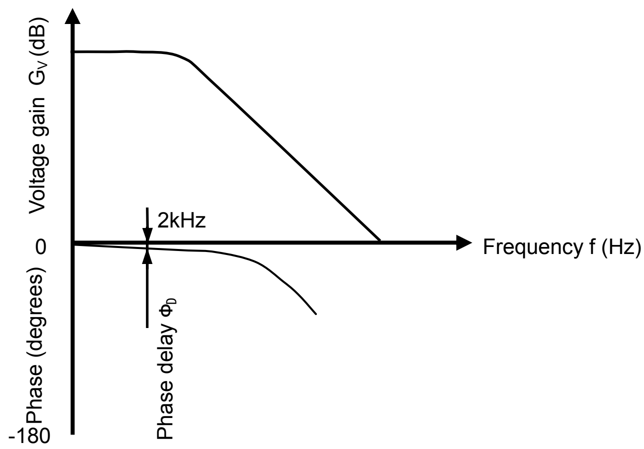



**7. $I_{sink}$**

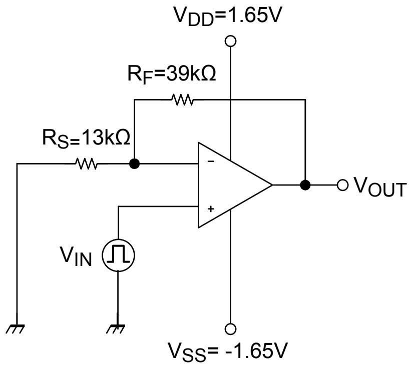



**8. $\phi_D$**



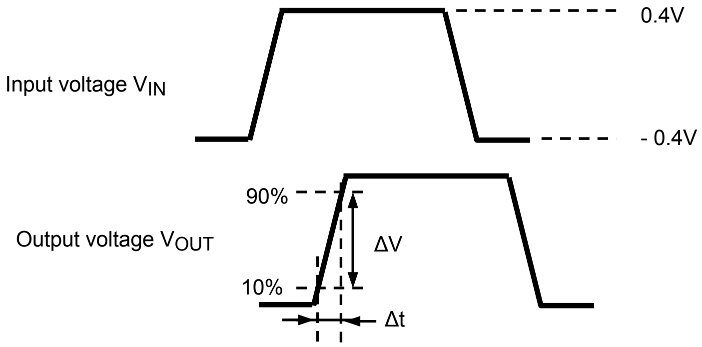
**9.SR**

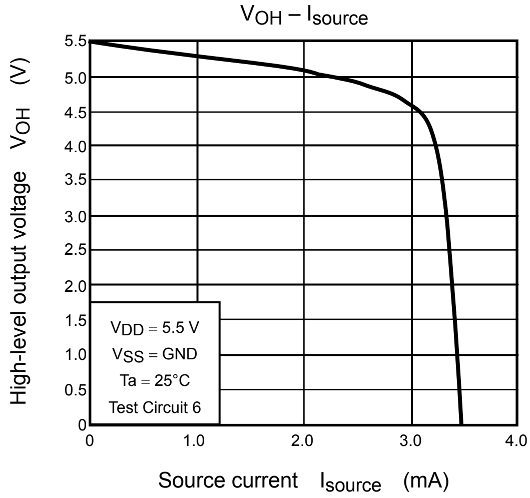


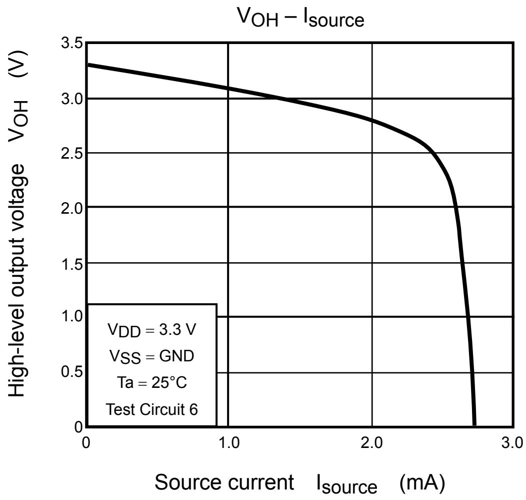

- SR

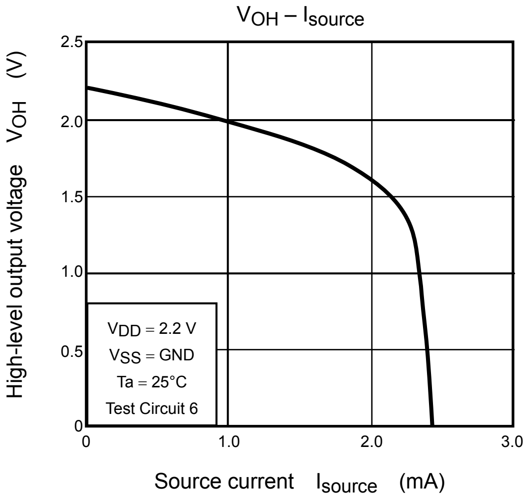
$$G_V = 1 + \frac{R_F}{R_S} = 12dB$$

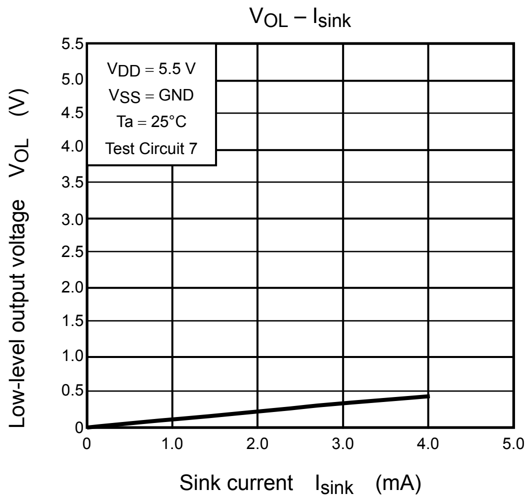
$$SR = \frac{\Delta t}{\Delta V}$$

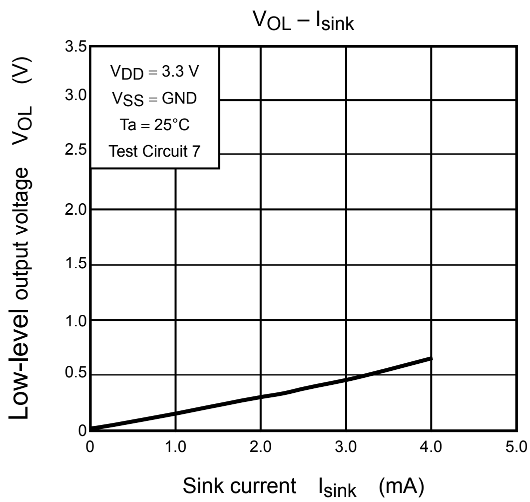


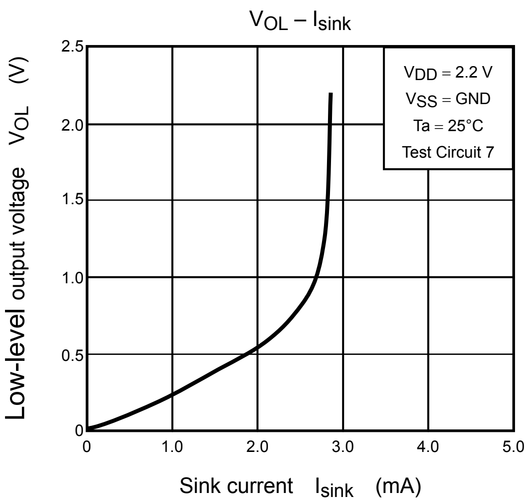

$V_{OH}$ – $I_{source}$
High-level output voltage $V_{OH}$ (V)
Source current $I_{source}$ (mA)
$V_{DD}$ = 5.5 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 6
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
1.0
2.0
3.0
4.0

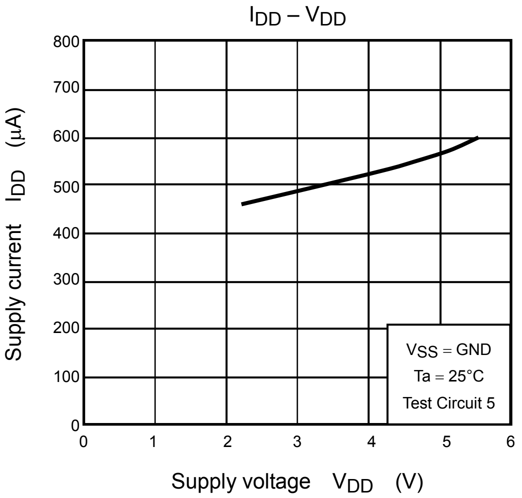

$V_{OH}$ – $I_{source}$
High-level output voltage $V_{OH}$ (V)
Source current $I_{source}$ (mA)
$V_{DD}$ = 3.3 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 6
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
1.0
2.0
3.0

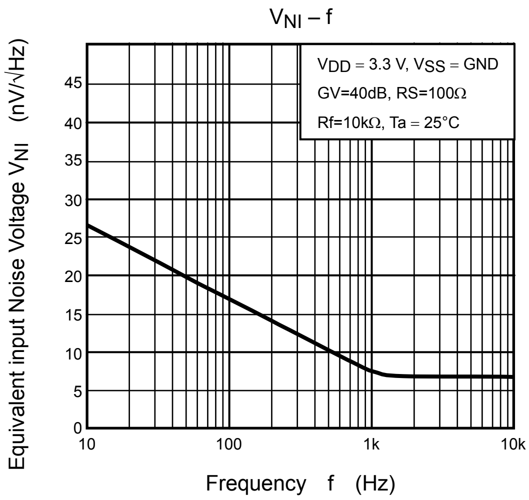

$V_{OH}$ – $I_{source}$
High-level output voltage $V_{OH}$ (V)
Source current $I_{source}$ (mA)
$V_{DD}$ = 2.2 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 6
0
0.5
1.0
1.5
2.0
2.5
1.0
2.0
3.0

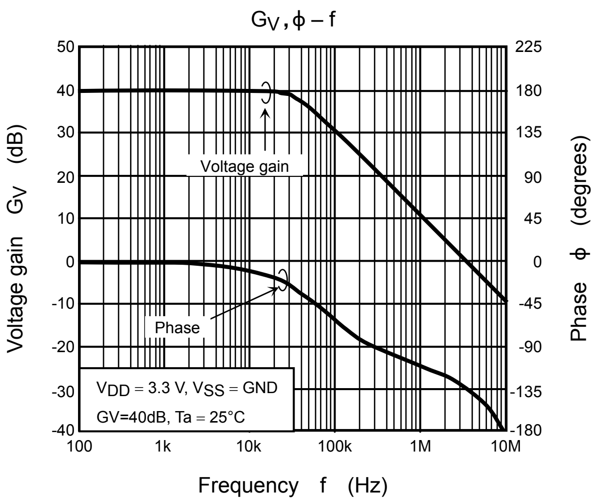

$V_{OL}$ – $I_{sink}$
Low-level output voltage $V_{OL}$ (V)
Sink current $I_{sink}$ (mA)
$V_{DD}$ = 5.5 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 7
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
1.0
2.0
3.0
4.0
5.0

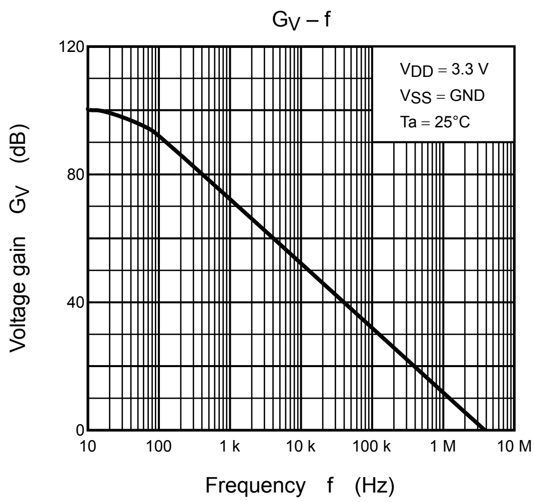

$V_{OL}$ – $I_{sink}$
Low-level output voltage $V_{OL}$ (V)
Sink current $I_{sink}$ (mA)
$V_{DD}$ = 3.3 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 7
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
1.0
2.0
3.0
4.0
5.0

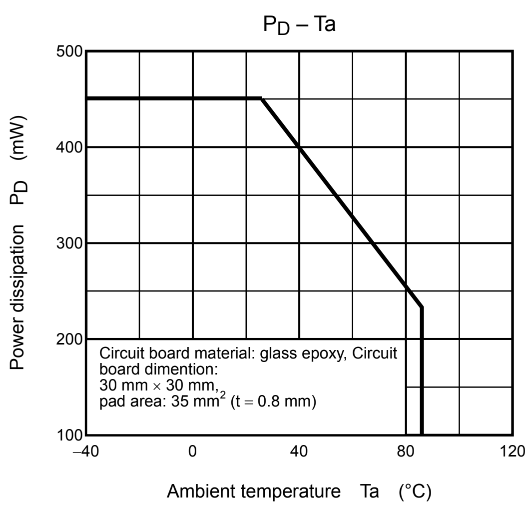

$V_{OL}$ – $I_{sink}$
Low-level output voltage $V_{OL}$ (V)
Sink current $I_{sink}$ (mA)
$V_{DD}$ = 2.2 V
$V_{SS}$ = GND
Ta = 25°C
Test Circuit 7
0
0.5
1.0
1.5
2.0
2.5
1.0
2.0
3.0
4.0
5.0


IDD – VDD
Supply current IDD (μA)
Supply voltage VDD (V)
VSS = GND
Ta = 25°C
Test Circuit 5


VNI – f
Equivalent input Noise Voltage VNI (nV/√Hz)
Frequency f (Hz)
VDD = 3.3 V, VSS = GND
GV=40dB, RS=100Ω
Rf=10kΩ, Ta = 25°C

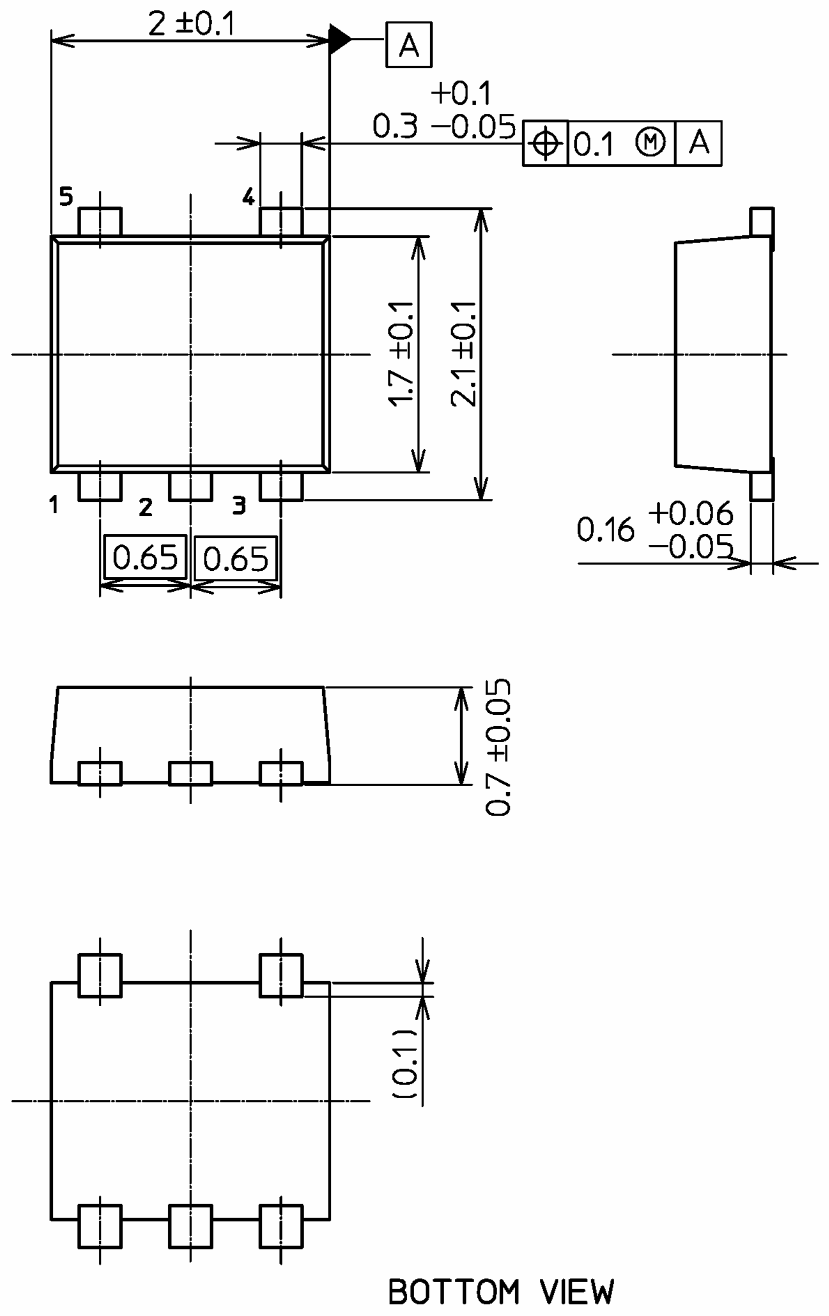

GV , ϕ – f
Voltage gain GV (dB)
Phase ϕ (degrees)
Frequency f (Hz)
Voltage gain
Phase
VDD = 3.3 V, VSS = GND
GV=40dB, Ta = 25°C


GV – f
Voltage gain GV (dB)
Frequency f (Hz)
VDD = 3.3 V
VSS = GND
Ta = 25°C


PD – Ta
Power dissipation PD (mW)
Ambient temperature Ta (°C)
Circuit board material: glass epoxy, Circuit board dimention:
30 mm × 30 mm,
pad area: 35 mm2 (t = 0.8 mm)

## Package Dimension

SON5-P-0202-0.65S Unit:mm




Weight : 7m g (typ.)

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