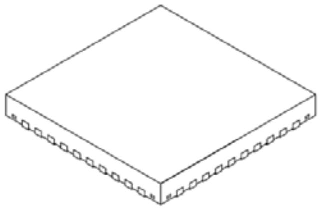
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TC78B004FTG

3-phase Full-wave Sine-wave PWM driving Brushless Motor Controller with Speed Control Function

1. Outline

TC78B004FTG is a 3-phase full-wave Sine-wave PWM driving brushless motor control IC with the speed control function.
Sine-wave PWM driving with 2-phase modulation enables driving in high efficiency and low noise condition.
The speed control function which can change speed of the motor is built in this product.



P-WQFN40-0606-0.50-001

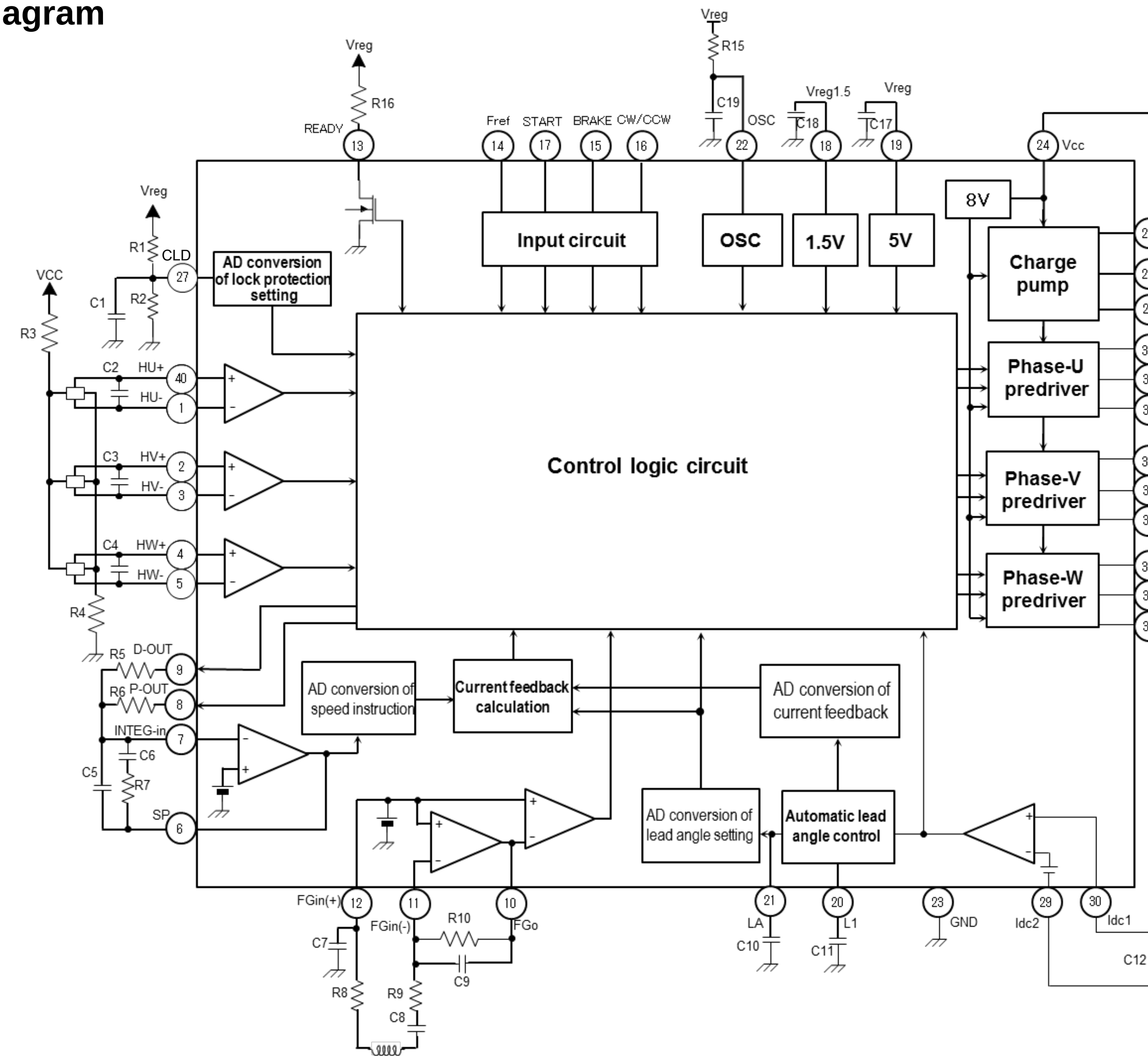
Weight: 0.0849 g (typ.)

2. Features

- Sine-wave PWM driving system
- 2-phase modulation system with low switching loss
- Dead time function included
- External clock input
- FLL + PLL speed control circuit
- READY circuit output
- FG amplifier included
- Auto lead-angle control function included
- CW/Stop (Standby) / CCW / Brake functions included
- Current limitation function included
- Lock protection function included

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.
The IC should be installed correctly. Otherwise, the IC or peripheral parts and devices may be degraded or permanently damaged.

3. Block Diagram

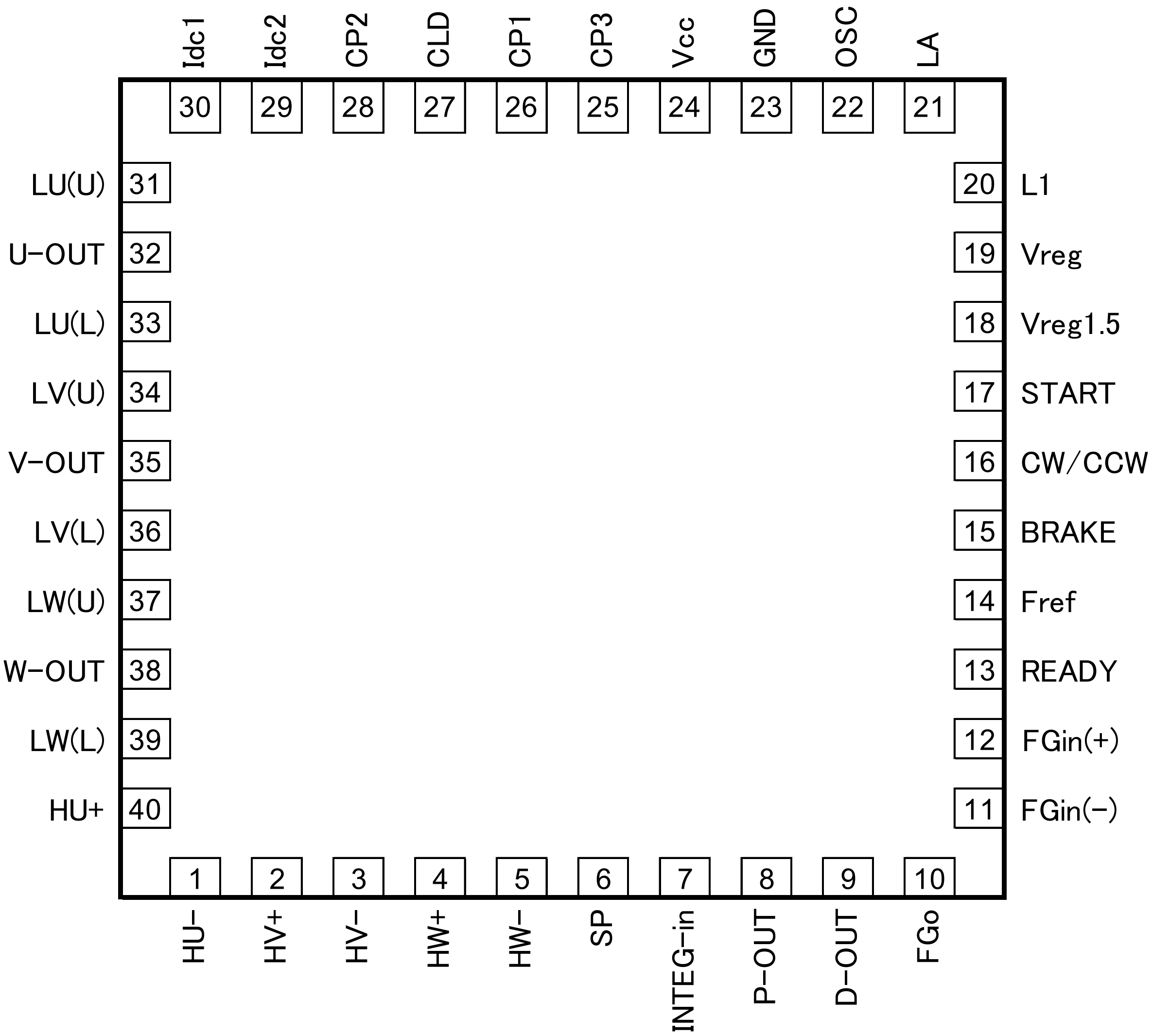


Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for expla

4. Pin Description

Pin No.	Pin name	Description	Note
1	HU-	Hall signal (Phase-U -) input pin	Hall element (Phase-U) signal - input
2	HV+	Hall signal (Phase-V +) input pin	Hall element (Phase-V) signal + input
3	HV-	Hall signal (Phase-V -) input pin	Hall element (Phase-V) signal - input
4	HW+	Hall signal (Phase-W +) input pin	Hall element (Phase-W) signal + input
5	HW-	Hall signal (Phase-W -) input pin	Hall element (Phase-W) signal - input
6	SP	Integral amplifier output / speed instruction input	-
7	INTEG-in	Integral amplifier output	(-) pin
8	P-OUT	Phase deviation signal output	-
9	D-OUT	Discriminator deviation signal output	-
10	FGo	FG amplifier output pin	-
11	FGin (-)	FG amplifier input - pin	FG signal input
12	FGin (+)	FG amplifier input + pin	FG signal input
13	READY	READY output pin	Open collector output In the range of ±6.25%: L, out of the range of ±6.25%: High impedance
14	Fref	External clock input	Pull-up resistor 50 kΩ (typ.)
15	BRAKE	Brake signal input	Pull-up resistor 50 kΩ (typ.), L: Brake (Lower all phases ON)
16	CW/CCW	CW/CCW switching pin	Pull-up resistor 50 kΩ (typ.), H: CCW, L: CW
17	START	Start signal input	Pull-up resistor 50 kΩ (typ.), L: Start, H: Standby
18	Vreg1.5	1.5V reference power supply	Connecting capacitor to GND against 1.5V output
19	Vreg	5 V reference power supply	Connecting capacitor to GND against 5V output
20	L1	Lead angle correction circuit	External capacitor
21	LA	Lead angle correction circuit	ADC input
22	OSC	Internal reference clock frequency setting pin	Reference clock generation with external C/R
23	GND	Ground pin	-
24	V_{CC}	Power supply voltage applying pin for control system	Vcc (opr.) = 10 to 28 V
25	CP3	Charge pump pin	For upper Nch FET gate voltage generation
26	CP1	Charge pump pin	For upper Nch FET gate voltage generation
27	CLD	Lock protection setting / current feedback gain setting	-
28	CP2	Charge pump pin	For upper Nch FET gate voltage generation
29	Idc2	Output current detection signal input pin	Sense pin at GND side
30	Idc1	Output current detection signal input pin	Into gate block operation under the condition of 0.25 V (typ.) or more
31	LU (U)	Phase-U driving signal output (U)	Phase-U output FET gate (for upper-side Nch drive)
32	U-OUT	Phase-U motor pin	-
33	LU (L)	Phase-U driving signal output (L)	Phase-U output FET gate (for lower-side Nch drive)
34	LV (U)	Phase-V driving signal output (U)	Phase-V output FET gate (for upper-side Nch drive)
35	V-OUT	Phase-V motor pin	-
36	LV (L)	Phase-V driving signal output (L)	Phase-V output FET gate (for lower-side Nch drive)
37	LW (U)	Phase-W driving signal output (U)	Phase-W output FET gate (for upper-side Nch drive)
38	W-OUT	Phase-W motor pin	-
39	LW (L)	Phase-W driving signal output (L)	Phase-W output FET gate (for lower-side Nch drive)
40	HU+	Hall signal (Phase-U +) input pin	Hall element (Phase-U) signal + input

5. Pin Assignment



6. Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC1}	31 (Note 1)	V
	V_{CC2}	40 (Note 2)	V
Input voltage	V_{IN}	-0.3 to 5.5 (Note 3)	V
Output voltage	V_{OUT}	5.5 (Note 4)	V
		-0.3 to 40 (Note 5)	V
		15 (Note 6)	V
	Vreg	5.5	V
	Vreg1.5	1.65	V
Output current	I_{OUT}	10 (Note 7)	mA
		100 (Note 8)	mA
		25 (Note 9)	mA
Power dissipation	P_D	3.9 (Note 10)	W
Operation temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: V_{CC} (in normal operation)

Note 2: V_{CC} (When 8 V charge pump is disabled, without external C for the charge pump.)
* In normal operation, maximum rating is Vcc_1, as charge pump function is necessary for the operation.

Note 3: CW/CCW, Fref, START, BRAKE, HU(+), HU(-), HV(+), HV(-), HW(+), and HW(-)

Note 4: READY

Note 5: LU(U), LV(U), LW(U), U-OUT, V-OUT, and W-OUT

Note 6: LU(L), LV(L), and LW(L)

Note 7: LU(U), LV(U), LW(U), LU(L), LV(L), and LW(L) source current, and peak current at FET driving

Note 8: LU(U) ,LV(U), LW(U), LU(L), LV(L), and LW(L), sink current, and peak current at FET drivint

Note 9: Vreg

Note 10: Mounted on PCB (Glass epoxy 76.2 mm × 114.3 mm × 1.6 mm, Cu area 60 %, double layer)

Absolute maximum rating is the standard without any exception even in a moment.
If the IC is operated in a condition beyond the rating, destruction, degeneration or damaging of IC or external parts possibly occurs. Design to avoid the condition beyond the rating in any operating condition.
Operate within the condition described in next table “Operating condition”.

7. Operating Condition (Ta = −30 to 85°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	10 to 28	V
External clock frequency	Fref	200 to 4000	Hz

8. Description for Operation

Note: Equivalent circuit may be partially omitted and simplified for explanatory purposes.

8.1. Sine-Wave PWM Driving

<Energization mode switching>

When starting, TC78H004FTG operates rectangle driving of 120° energization signal with position detection signal. After “f” (frequency every 1 phase of position detection signal (hall element signal)) exceeds “f_H” (setting frequency), at HU falling timing next-after IC counts 6 times of hall signal switching edges, the operation mode is switched to 180° energization mode. (For hall input signal, refer to section 8.8 Hall Amplifier Circuit.)
The setting frequency “f_H” is determined as follows.

Setting frequency: $f_H = 1 / \{(2^{16}-1) \times (1 / f_x) \times 6\}$

The f_x is internal reference clock determined with OSC external constants setting.
When f_x = 4 MHz, f_H = 10.17 Hz, f_x = 5 MHz, f_H = 12.7 Hz, f_x = 6 MHz, f_H = 15.25 Hz.

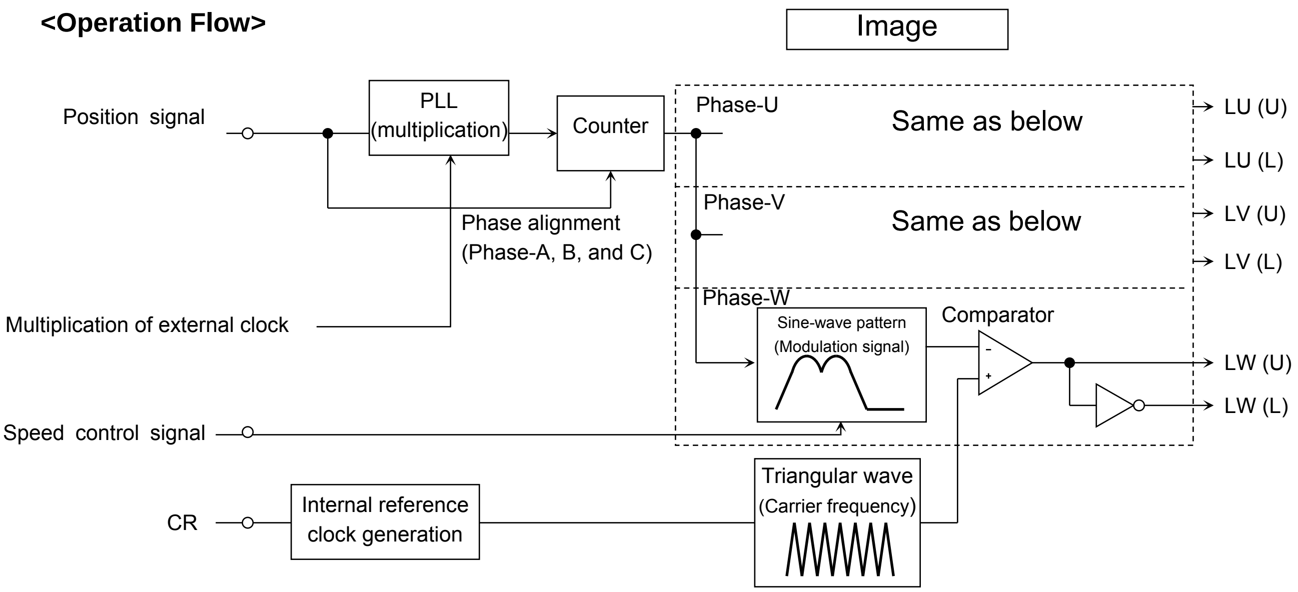
(Mode table)

Rotating state	Driving mode
$f_H > f$	Rectangle driving (120° energization)
$f_H < f$	Sine-wave PWM driving (180°energization)

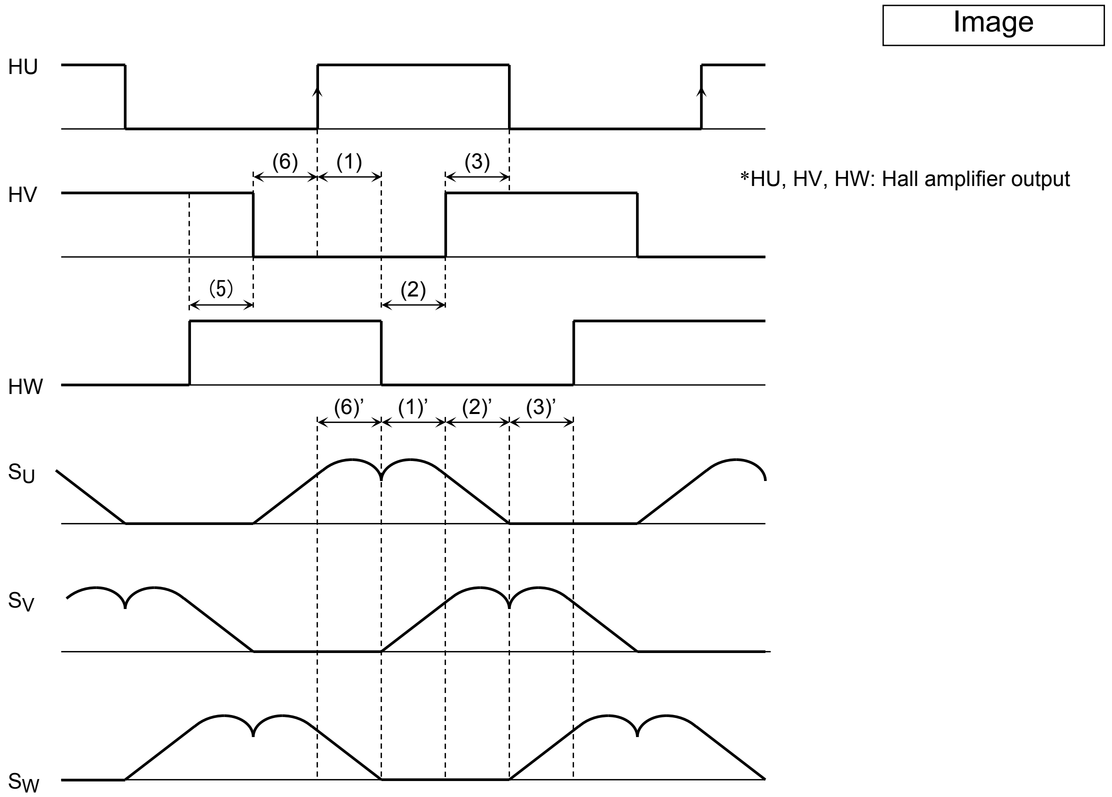
Note: To avoid malfunction from noise, IC operates in 120° energization mode when “f” is higher than set frequency. The conditions are as follows: 666.7 Hz when f_X = 4 MHz, 833.3 Hz when f_X = 5 MHz, 1 kHz or more when f_X = 6 MHz.

The following figure is actually processed digitally with the image chart in the IC.

<Operation Flow>



The modulation wave is generated by position detection signal. Sine-wave PWM signal is generated by comparing this modulation wave to triangular wave.
IC counts the time between one zero-cross timing to next zero-cross timing of 3 position detect signals (60° electrical angle), and use this time as next 60° phase length.
The 60° phase length of the modulation signal consists of 32 data, and time length for 1 data is 1/32 of time length of the previous 60° phase length, so that the modulation wave advances with this length.

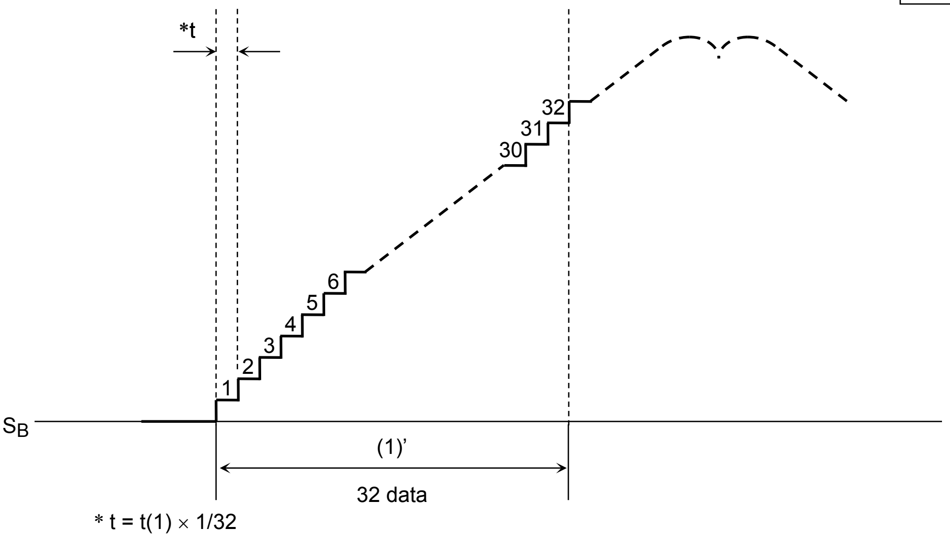


The resolution of PWM output is 1/128.

The figure on the previous page, the modulation wave (1)' data progresses by 1/32 time length of (1) (from HU:↑ to HW:↓). The modulation wave (2)' data also progresses by 1/32 time length of (2) (from HW:↓ to HV:↑).

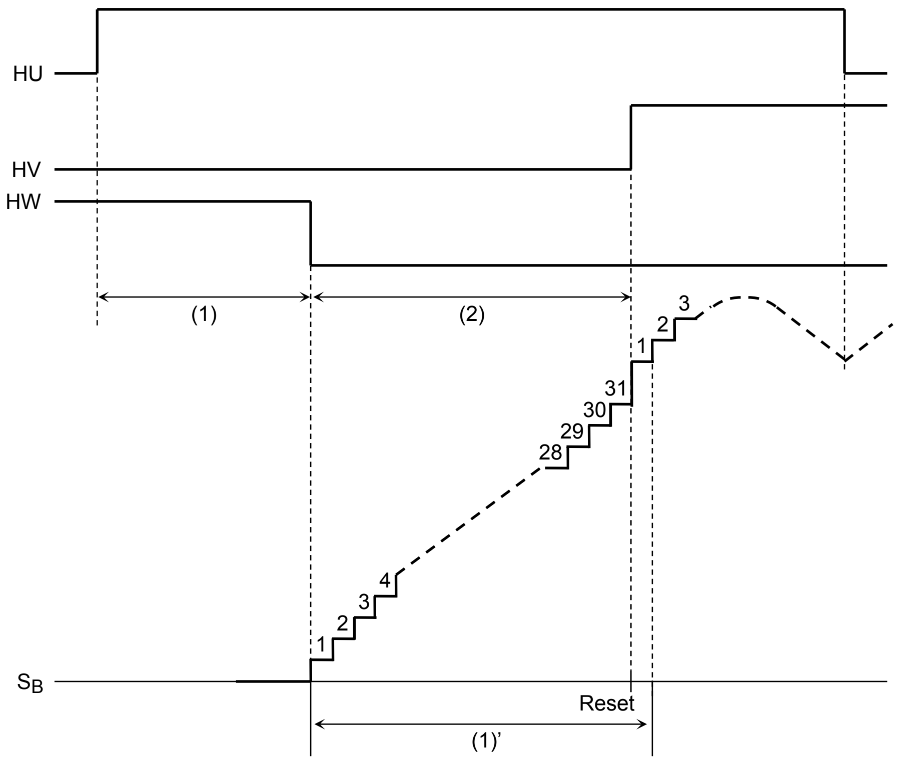
If next zero-cross point does not come even 32 data completed, next 32 data progresses on same time length by next zero-cross point comes.

Image



At the same time, phase alignment with the modulation wave is done on every zero-cross timing of position detection signal. On every 60° electrical angle, the modulation wave is reset in synchronization with up or down edge of position detection signal (hall amplifier output signal). Therefore, if the next zero-cross timing comes before the end of 32 data for 60° phase because of the lag of zero-cross timing of position detection signal, the data is reset and next data for 60° phase starts. In such case, the modulation wave has discontinuous point on the reset timing.

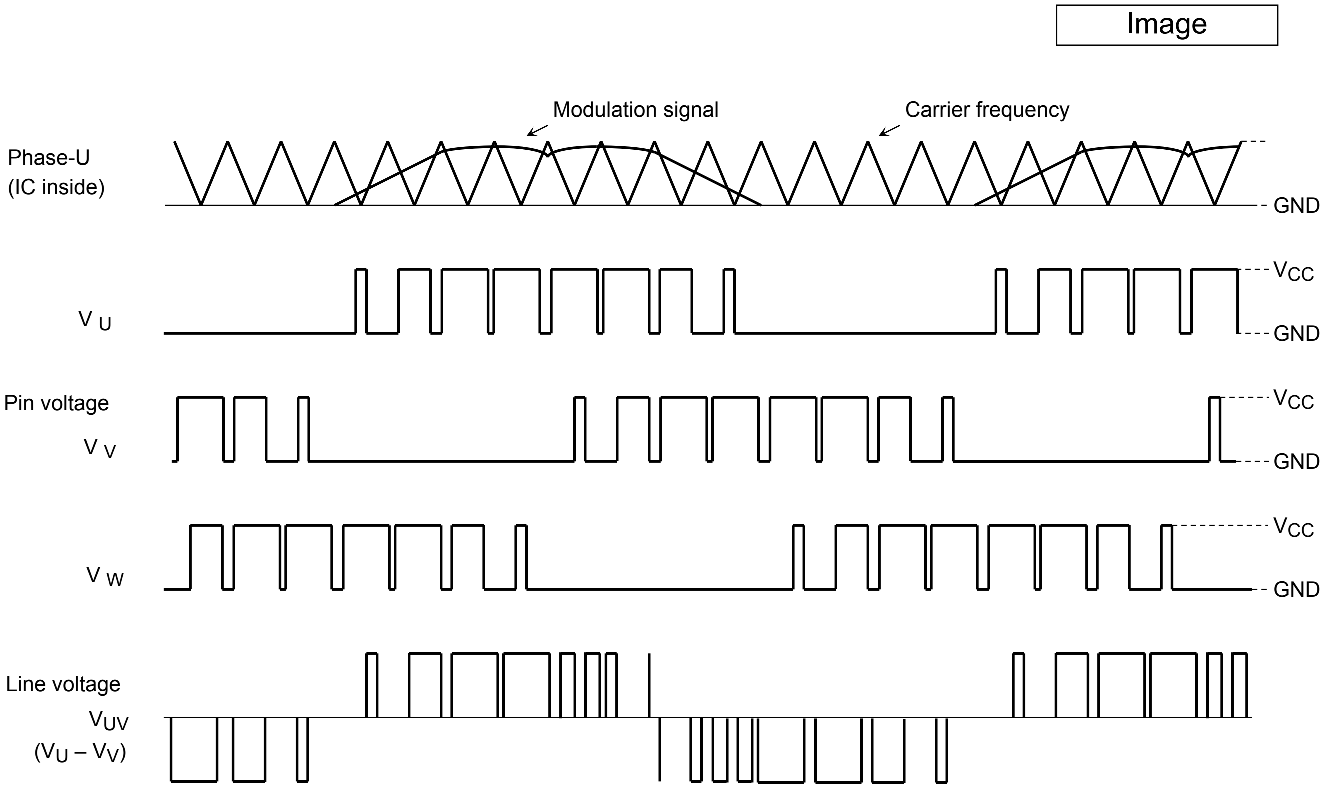
Image



Note: Timing charts may be simplified for explanatory purposes.

(Operation waveform of Sine-wave PWM driving)

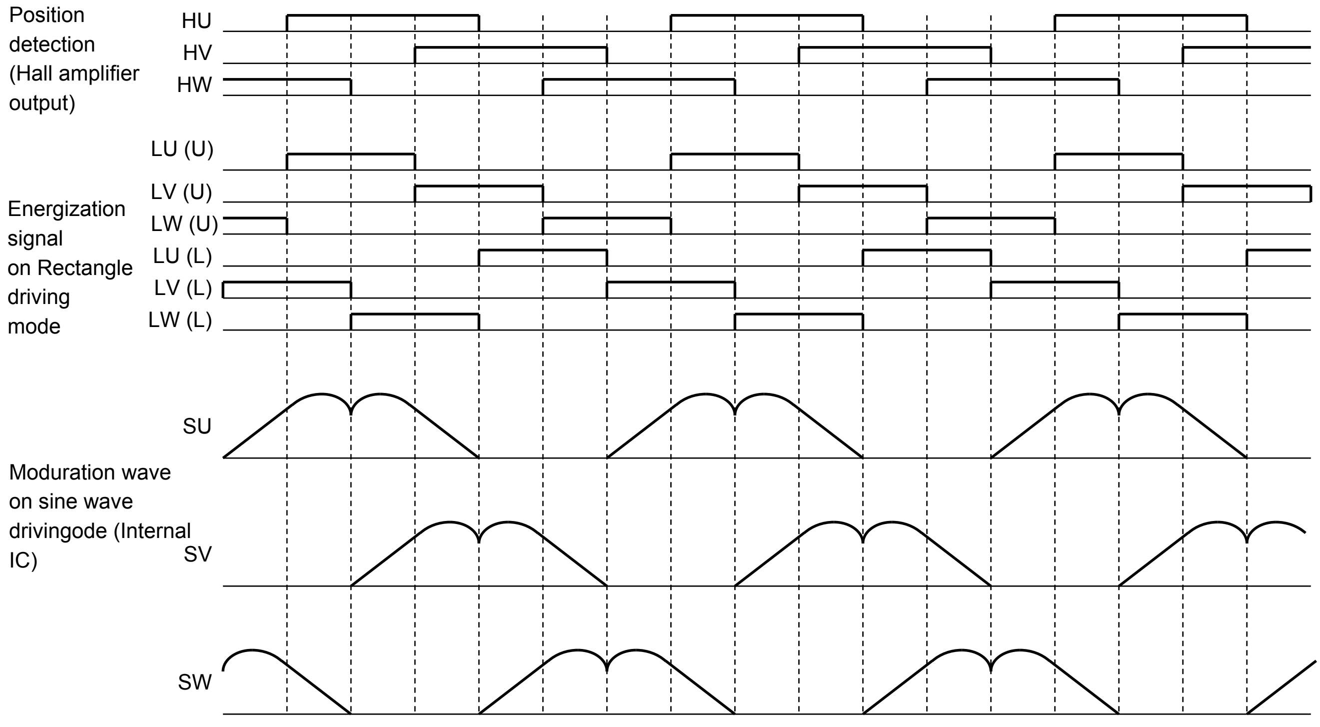
Note: Timing charts may be simplified for explanatory purposes.



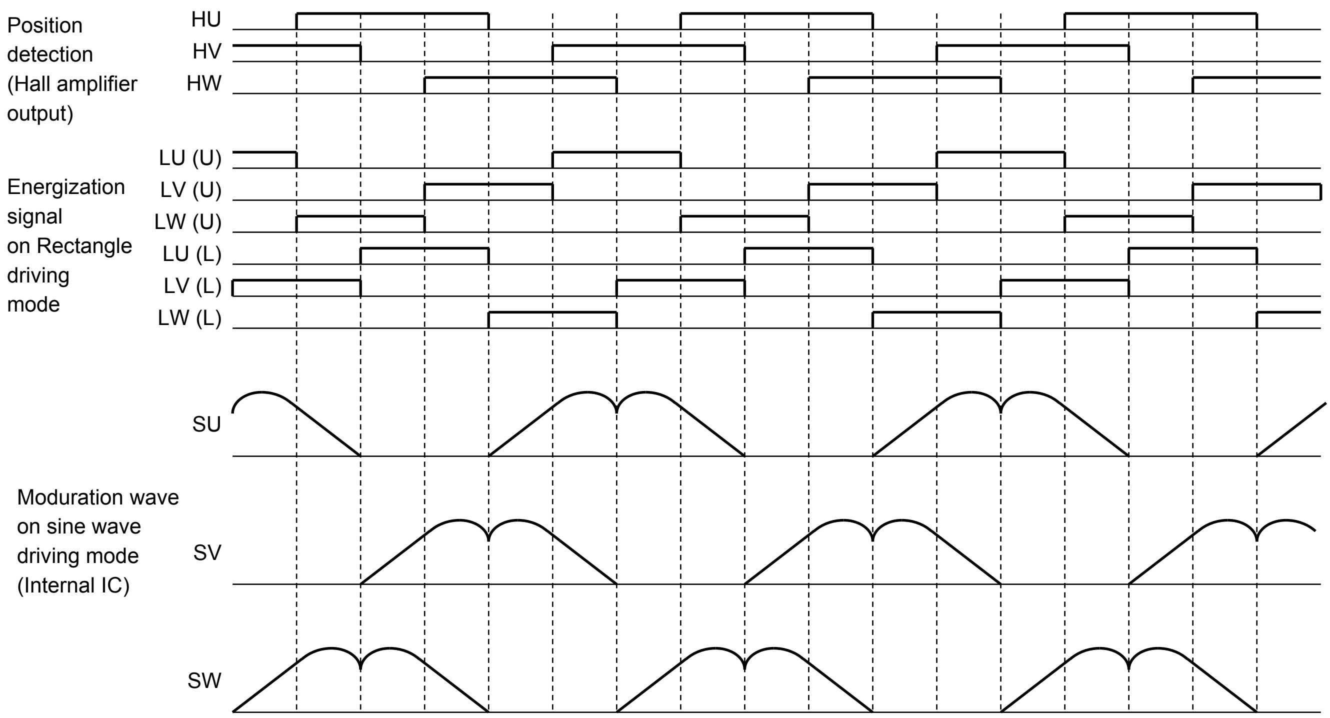
Timing Chart

Image

Note: Timing charts may be simplified for explanatory purposes.



CW



CCW

*HU, HV, and HW: Hall amplifier output

8.2. Internal Reference Clock Frequency

The reference clock is generated internally with external C and R attached to OSC pin.
When External C and R = 2.4 kΩ / 100pF, 5MHz±10%.
This reference clock is used as follows:

- PWM frequency
- Dead time
- Reference clock of charge pump (booster circuit)
- Reference clock of ADC block in lead angle circuit
- Reference clock of the counter for time measurement of external clock
- Reference clock of FLL and PLL

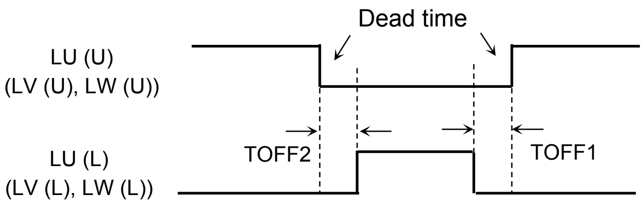
Note: It stops when START = H (Standby).

8.3. PWM Frequency

When the internal reference clock frequency is defined as f_X, the PWM frequency fqwm = f_X/248.
For example,
f_X = 6MHz: fpwm = 24.2 kHz
f_X = 5MHz: fpwm = 20.1 kHz
f_X = 4MHz: fpwm = 16.1 kHz
Note: Triangular wave is reset on the rising timing of phase-U with a consideration of its synchronization (360° reset).

8.4. Dead Time Setting

Dead time on driving signal output is generated to avoid same-timing ON of upper and lower output power FET because TC78B004FTG controls output FET using PWM with synchronous commute system.
The Dead time is set by using the reference clock generated by external C and R.



The internal reference clock is defined as f_X, the dead time TOFF1 = TOFF2 = (1/f_X) × 6.
For example,
f_X = 6 MHz: TOFF1 = TOFF2 = 1.0 μs
f_X = 5 MHz: TOFF1 = TOFF2 = 1.2 μs
f_X = 4 MHz: TOFF1 = TOFF2 = 1.5 μs

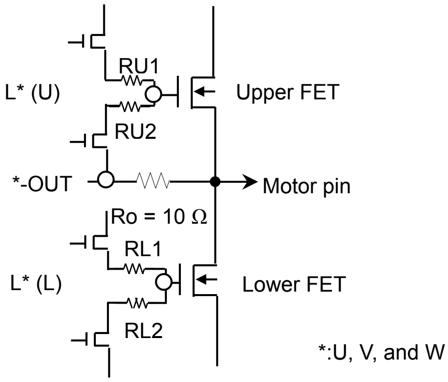
The wave form shown above is in the timing of ON or OFF of FET gate drive output.
In this timing, the IC drives with FET gate through internal resistor.
The rising or falling of gate wave form is changed depending on the gate capacity of external FET.
Please confirm that the FET to be used does not have a through current.

8.5. Charge Pump (Booster Circuit)

TC78B004FTG is for Nch + Nch external output FET system. So charge pump circuit is included to generate voltage for upper Nch Gate voltage.
The booster voltage is V_{CC} + 8 V. Gate voltage of upper FET is V_{CC} + 7.75 V.
The voltage is boosted with 1/16 frequency of the internal reference clock (f_X). (f_X = 5 MHz: 312.5 kHz.)
CP3 pin voltage which is the charge pump voltage is output ON if the voltage is more than V_{CC} + 6.35 V (typ.). Then, it is output OFF if the voltage is less than V_{CC} + 5.8 V (typ.).

8.6. External FET Gate Drive Output

To suppress the switching noise on FET driving, source and sink output for FET driving is configured as right figure.
Next value resistors are built in the output portion to control the output FET.

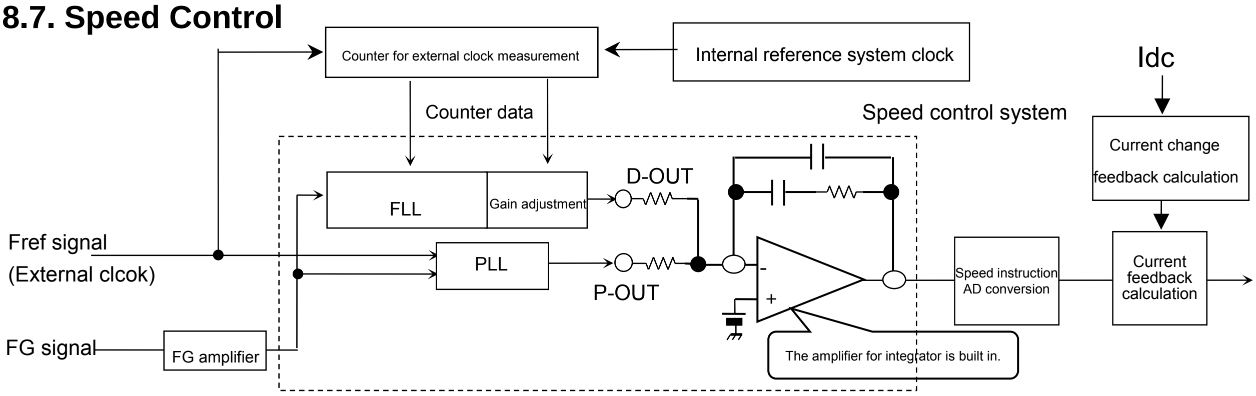


Built-in resistor

Upper side source	RU1 = 1 kΩ (typ.)
Upper side sink	RU2 = 100 Ω (typ.)
Lower side source	RL1 = 1 kΩ (typ.)
Lower side sink	RL2 = 100 Ω (typ.)

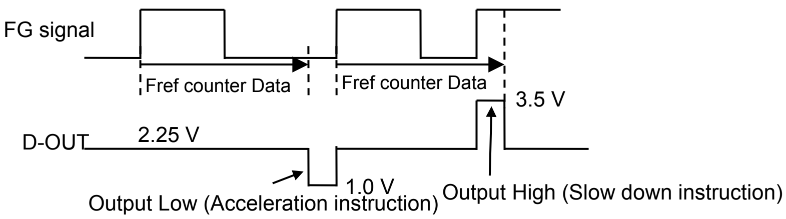
Note: Ro = 10Ω should be surely inserted between each OUT pin and the motor pin.

8.7. Speed Control



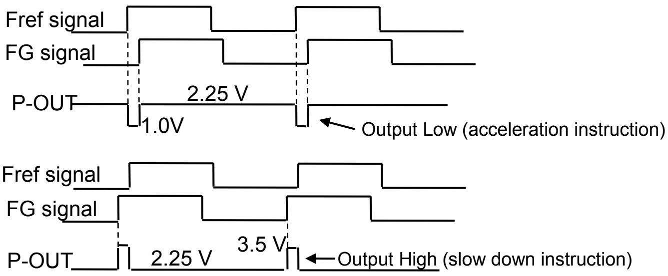
The input frequency range of Fref is restricted by the number of bit of the counter for external clock measurement.
Fref (min) = 200 Hz, Fref (max) = 4 kHz

<D-OUT output>



The cycle of external clock Fref is counted with internal reference clock.
The time of the counter DATA is compared with the FG cycle.
When the FG cycle is longer than Fref cycle (counter DATA), the acceleration instruction (1.0 V) is issued.
When the FG cycle is shorter than Fref cycle (counter DATA), the slow down instruction (3.5V) is issued.
Moreover, the amplitude level of D-OUT is changed by the gain adjustment circuit.

<P-OUT output>



P-OUT is output in the timing of which motor rotation speed is in the stable area (READY = Low).
The phase difference between Fref signal and FG signal is output.
When the FG signal is later than the Fref signal, the acceleration instruction (1.0V) is issued.
When the FG signal is progressing from the Fref signal, the slow down signal (3.5V) is issued.
P-OUT and D-OUT outputs are Low (pull-down to the GND at 40 kΩ) in the standby mode (START = H), then the pull-down resistor is open after startup.

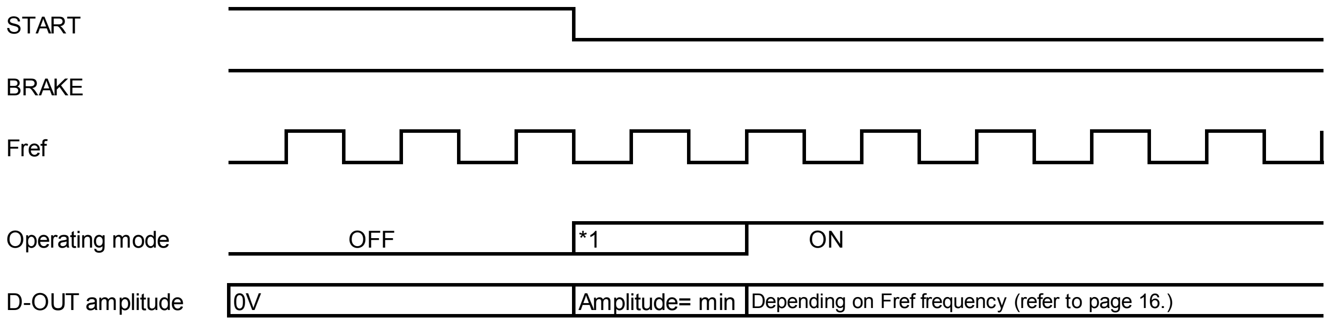
The counter is insufficient when the Fref is quite slower than the use range (200 Hz to 4 kHz).

In details, when the Fref slower than around 150 Hz (CLK cycle × 8 × 16^3 = 6.55 ms) is input, in case of f_X = 5 MHz setting. The counter is full, and the driving output is OFF (overflow detection).

(If f_X = 4 MHz, the counter is full at 122Hz. If f_X =6 MHz, the counter is full at 183 Hz.) The OFF mode is cleared when the START is set to H, or the BRAKE is set to L at once. The operation is started after restarting. To start certainly, please set a START signal and a BRAKE signal after the Fref frequency determination which is not overflowed.

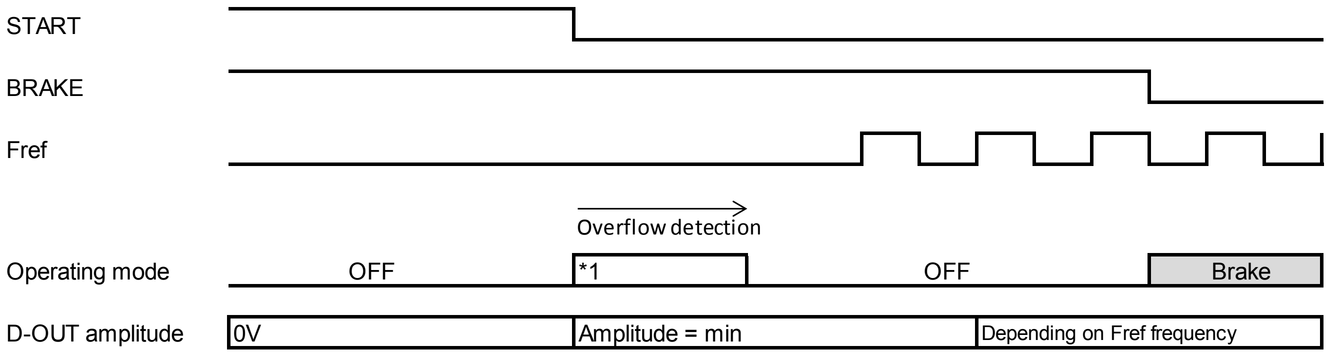
■In case of start / stop control with START pin

(1) Normal operation (Fref is within the operating frequency)



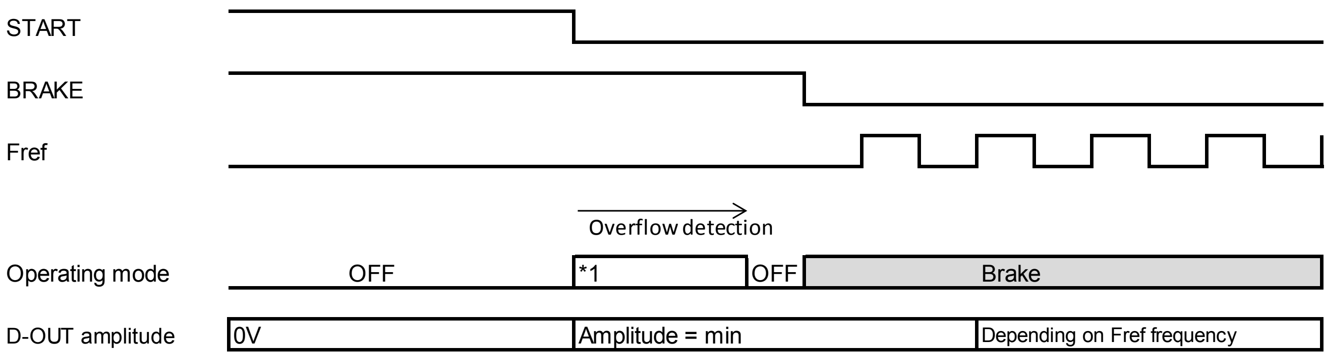
*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)
Note) After starting, two edges of FG signal are in the accelerated mode. (The amplitude of D-OUT is depending on Fref frequency.) (Except *1 period.)

(2) In case that Fref is input slowly 1 (Fref is within the operating frequency)



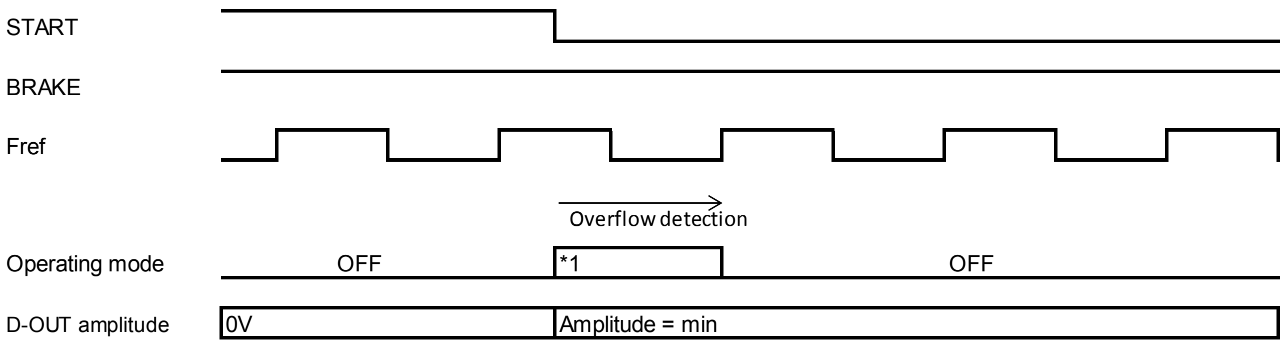
*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

(3) In case that Fref is input slowly 2 (Fref is within the operating frequency)



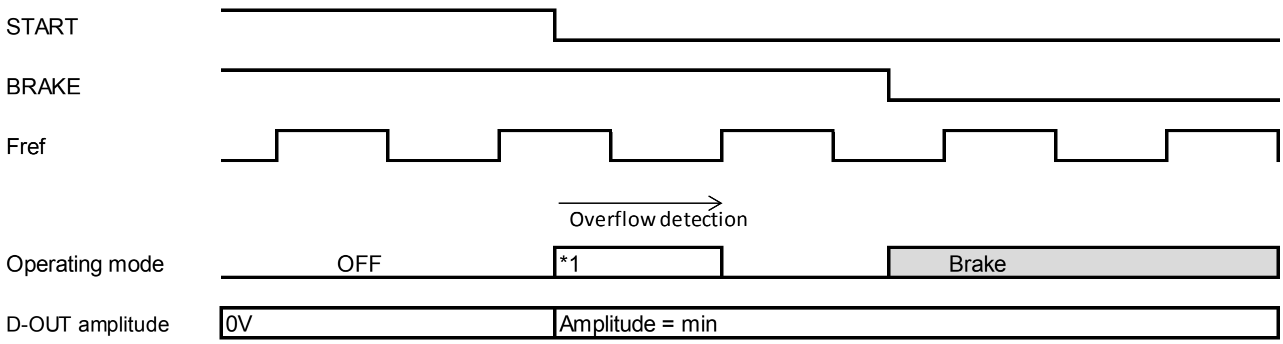
*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

(4) In case that Fref frequency is lower than the operating frequency 1



*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

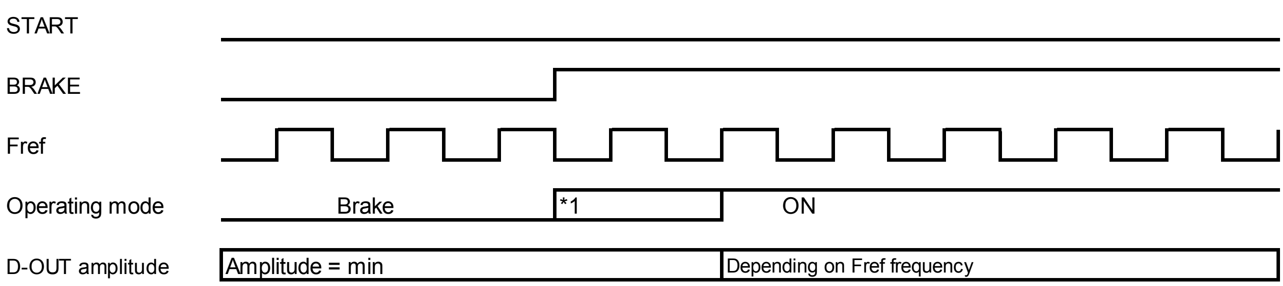
(5) In case that Fref frequency is lower than the operating frequency 2



*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

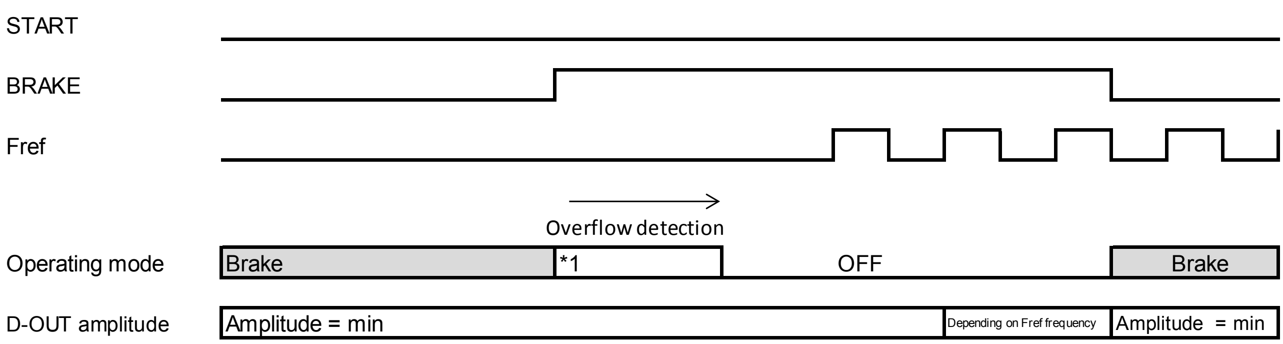
■ **In case of start / stop control with BRAKE pin**

(6) Normal operation (Fref is within the operating frequency)



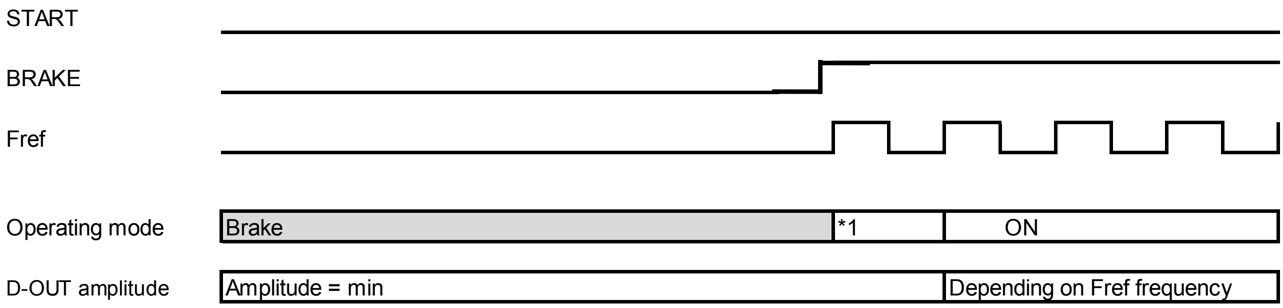
*1) After starting, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)
Note) After starting, two edges of FG signal are in the accelerated mode. (The amplitude of D-OUT is depending on Fref frequency.) (Except *1 period.)

(7) In case that Fref is input slowly (Fref is within the operating frequency)



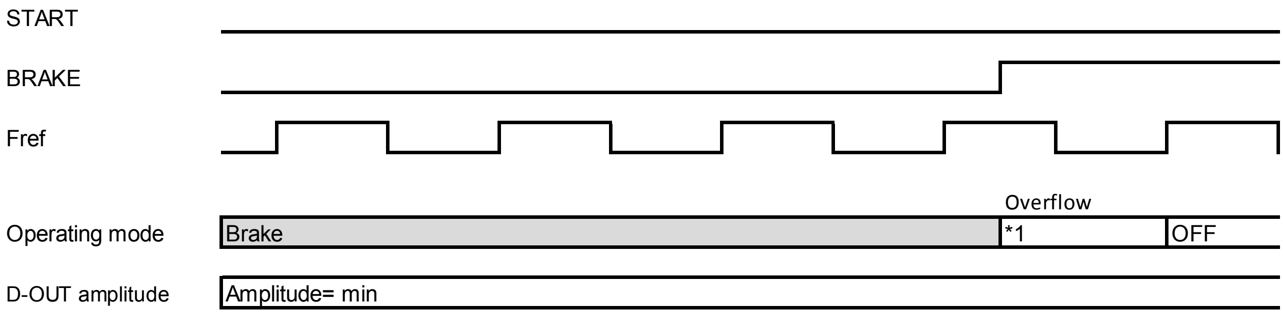
*1) After releasing BRAKE pin, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

(8) In case that Fref is input slowly (Fref is within the operating frequency, and Fref is input immediately after BRAKE =H.)



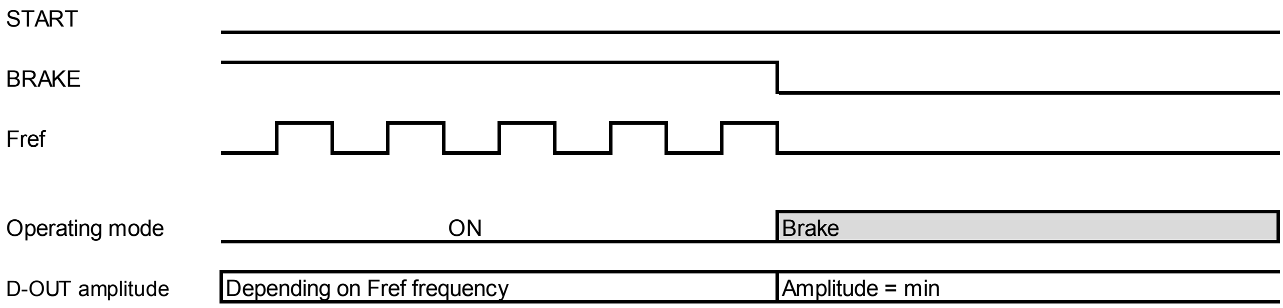
*1) After releasing BRAKE pin, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

(9) In case that Fref frequency is lower than the operating frequency



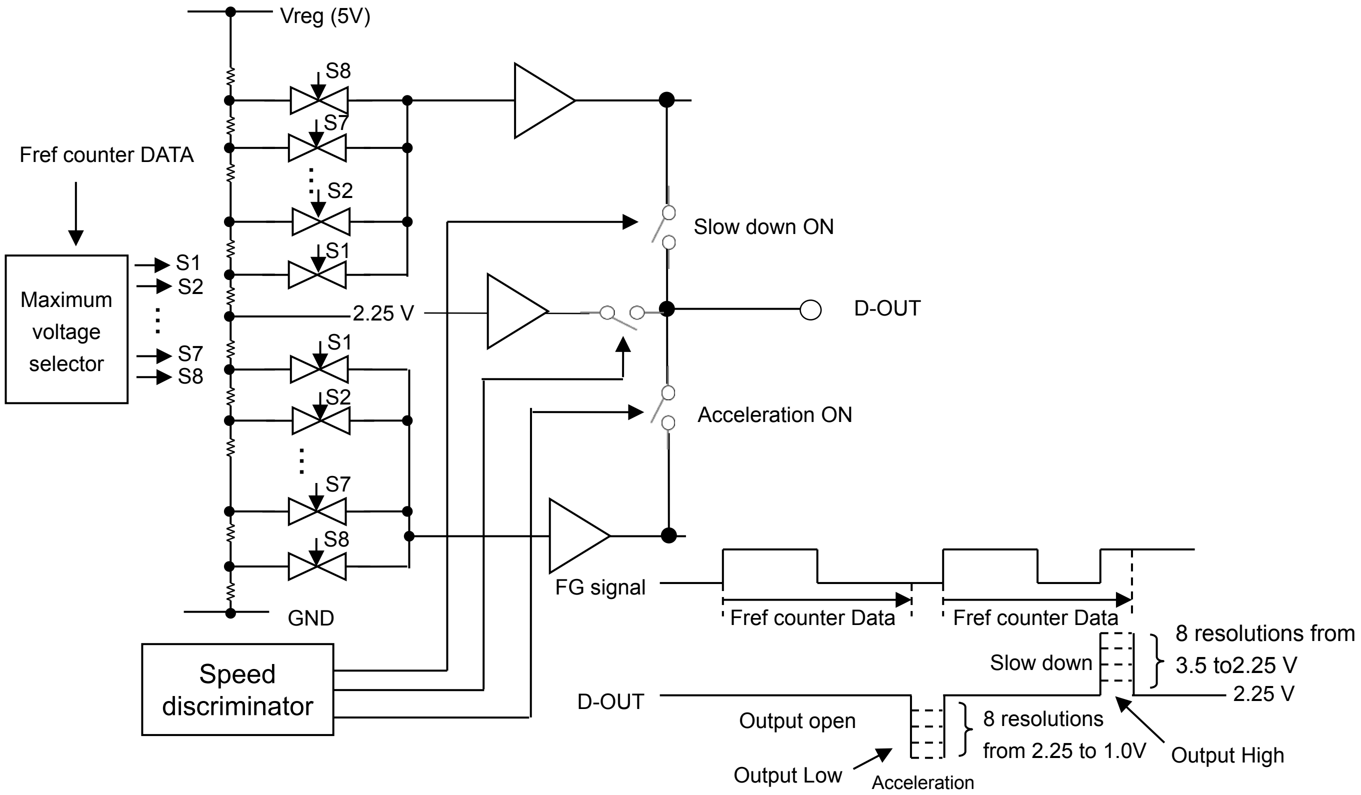
*1) After releasing BRAKE pin, the amplitude of D-OUT is accelerated min (2.094V), and the operation with minimum amplitude starts up. (Two rising edges of Fref)

(10) Fref frequency and signal are not input (in case of motor stop)



8.7.1. Gain Adjustment Circuit

This is the function to switch the amplitude of D-OUT output depending on the rotation speed instruction (Fref frequency).

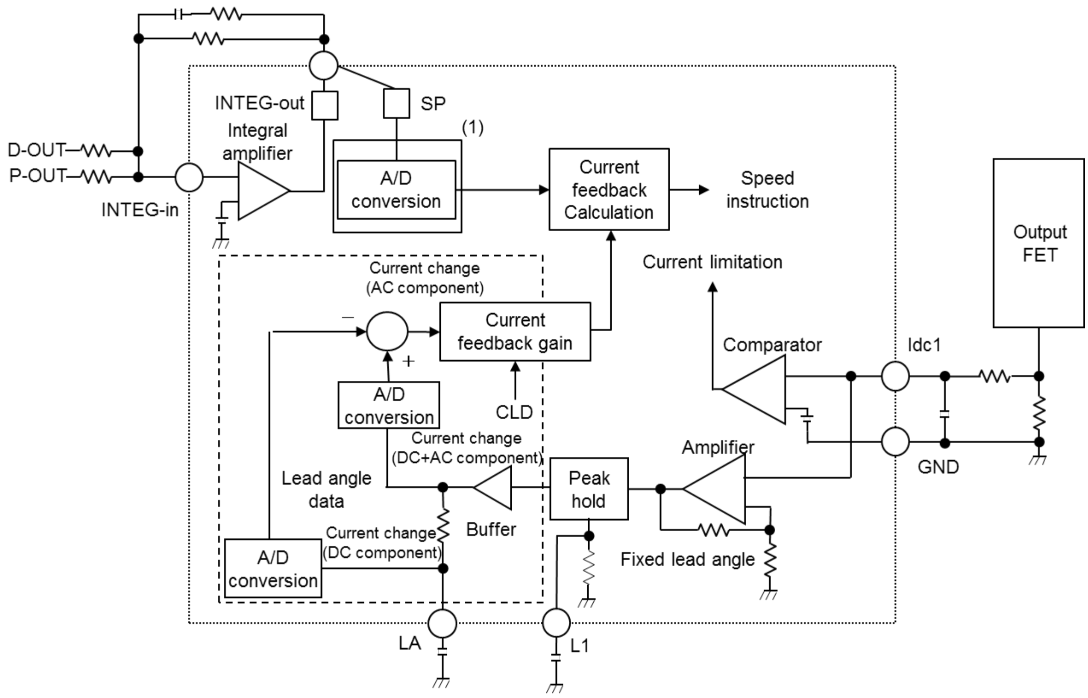


Fref counter DATA is changed depending on Fref frequency.
Corresponding to this counter DATA, the peak voltage of D-OUT signal is switched as follows.

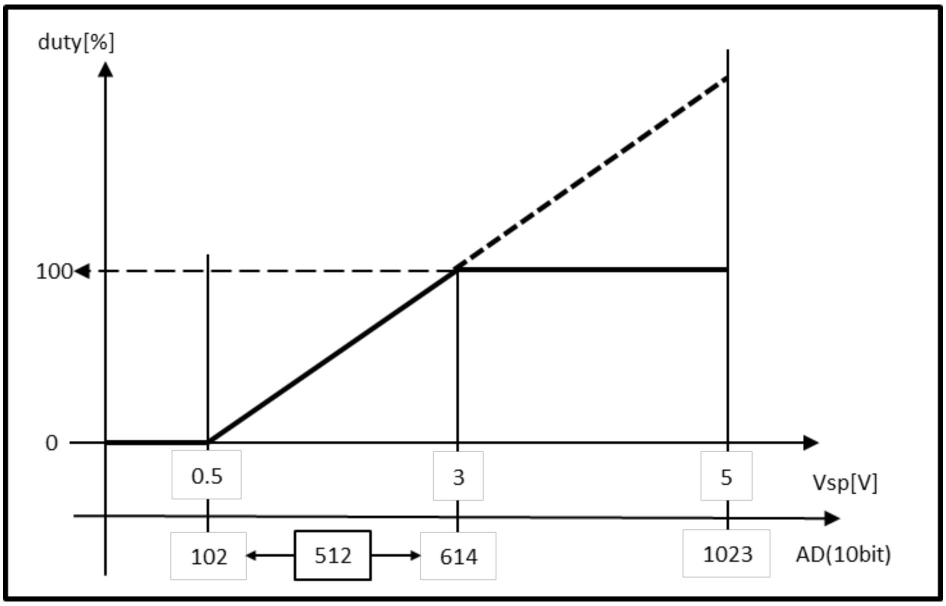
For the switching frequency, refer to the following table.

Counter data	Switching frequency at f_X = 4 MHz	Switching frequency at f_X = 5 MHz	Switching frequency at f_X = 6 MHz	Analog SW	D-OUT (min)	D-OUT (max)
16667	240Hz or less	300Hz or less	360Hz or less	S1 ON	2.094	2.406
13333	240 to 300Hz	300 to 375Hz	360 to 450Hz	S2 ON	1.938	2.563
11111	300 to 360Hz	375 to 450Hz	450 to 540Hz	S3 ON	1.781	2.719
9524	360 to 420Hz	450 to 525Hz	540 to 630Hz	S4 ON	1.625	2.875
7843	420 to 510Hz	525 to 637.5Hz	630 to 765Hz	S5 ON	1.469	3.031
6667	510 to 600Hz	637.5 to 750Hz	765 to 900Hz	S6 ON	1.313	3.188
4445	600 to 900Hz	750 to 1125Hz	900 to 1350Hz	S7 ON	1.156	3.344
4444	900Hz or more	1125Hz or more	1350Hz or more	S8 ON	1.000	3.500

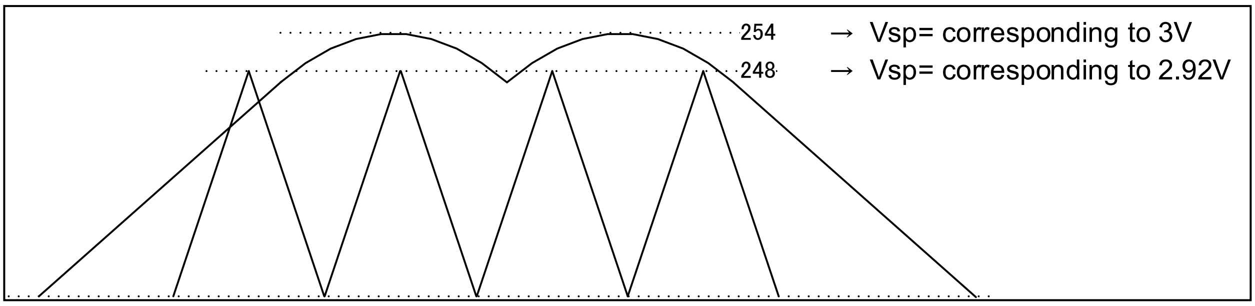
8.7.2. Speed Instruction Input Block



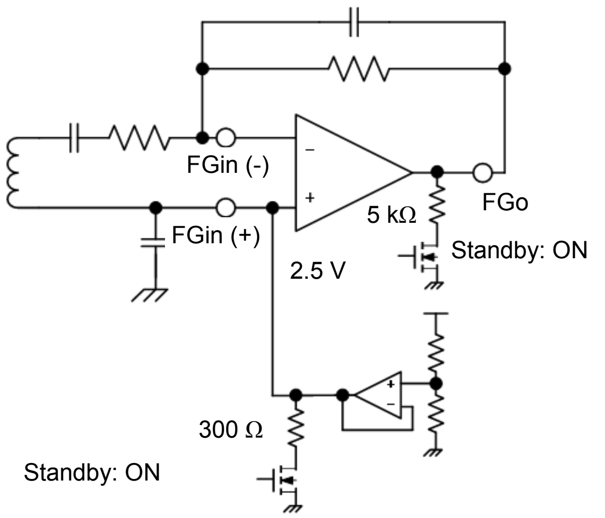
(1) The output voltage of the integral amplifier is input to AD converter for the speed instruction.
Control range of SP voltage: 0.5 to 3.0V   Resolution: 512



This circuit has 0.5V (typ.) of offset, and if the voltage of SP pin exceeds the value, an energization signal output operates. When the voltage of SP pin is 3.0V (typ.), the amplitude of internal modulation waveform (PWM duty of energization signal output) becomes maximum. When the voltage of SP pin is around 3V, the modulation waveform is output as the following image.



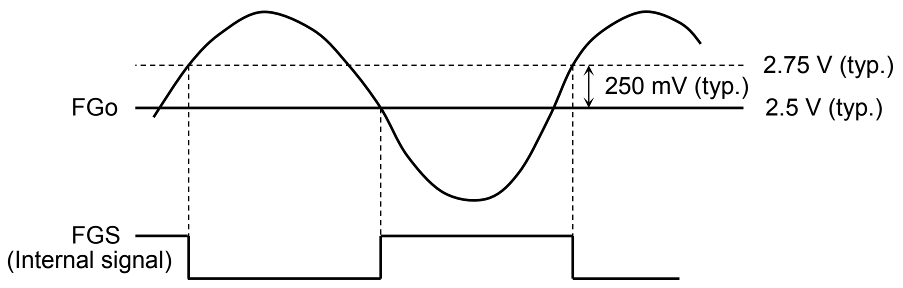
8.7.3. FG Amplifier / Hysteresis Comparater Circuit



The FG amplifier supports a pattern FG and sets 2.5V of the reference voltage internally.
The signal for the multiple of a gain is output by inputting sine wave more than 50 mVpp.
The open loop gain is 40 dB (min) (@10 kHz, design target value).

The rear-stage has a hysteresis comparator, which compares FGo output.
The single-side hysteresis of 250 mV is provided in this comparator to the reference voltage of 2.5V, and the rectangle wave of FGS (internal signal) is input to the internal counter.

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

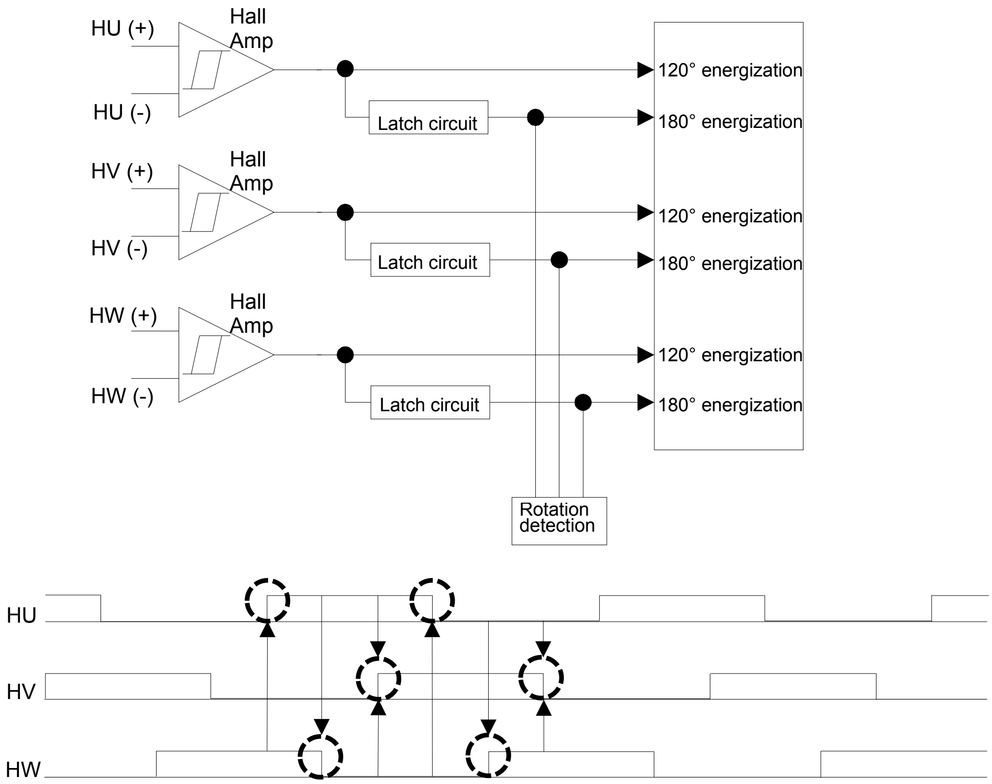


The dynamic range of FGo output is as follows.
1.2 V to V_{reg} - 1.2 V at IFGo = ±100 μA

To improve the margin to a noise, a filter (1 μs) is added to the FG comparator at a switching edge.

8.8. Hall Amplifier Circuit

Input the hall element output signal. If noise exists in the input signal, connect a capacitor between the input pins.
Common mode input voltage range, VCMRH = 0.5 to 3.5 V.
To avoid a chattering or a malfunction during the 180° energization mode, latch circuit is included. It detects the hall signal state of other phase, checks the L/H level and if the level is adequate, and so it goes to latch state. Rotating direction is detected and confirmed at the same time, with detection of 3 phase hall signals.
Hall amplifier has input hysteresis (16mV@typ.). During 120° energization operation, malfunction is avoided by only its hysteresis. If all hall input are opened, all low, and all high, all outputs for motor will be Hi-impedance.
The hall IC input (single side input = Vreg/2, input from 0 to 5V) can be also supported.



8.9. READY Circuit

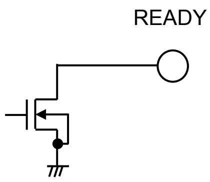
As the state of number of motor rotations, L or HZ is output by open drain output.
When the motor rotates, FG signal is counted. Then, whether the frequency is within ±6.25% or not to the setting value, the following is output.
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Within ±6.25% to the number of motor rotation: L output

Not within±6.25% to the number of motor rotation: HZ (High impedance)

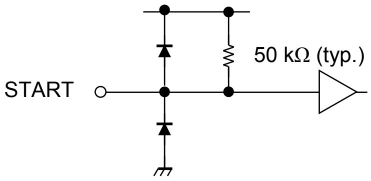
In case of Standby (START = H), the READY output is high impedance.
In case of CW/CCW pin settings and reversal rotations, if FG signal to the setting value is within ±6.25%, the READY output is L.
Connect pull-up resistor to the READY output pin. Determine the resistor value in consideration with the following characteristics. The input current is 2 mA (max).

VDS = 0.5 V (max) at IR = 2 mA



Note: There is no power supply side protection diode of the READY pin.

8.10. Start / Standby Circuit



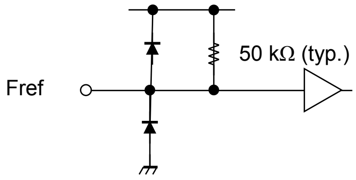
START pin is TTL input and includes 5 V pull-up resistor inside.
To avoid malfunction by input noise, a CR filter is included in back of the input buffer.
The reflection to the input is delay by the filter time.
Filter time: 7.5 µs (typ.) Dispersion: 5 to 10µs

START input	Mode
H	Standby
L	Start

Standby function

- The internal reference clock and the boosting circuit of upper side Nch output drive are turned OFF.
- Vreg and Vreg1.5 operate.
- Current consumption at Standby: 500 µA (typ.)

8.11. Fref (External Clock Input) Circuit



The input is TTL input and includes 5 V pull-up resistor inside.
To avoid malfunction by input noise, a CR filter is included in back of the input buffer.
The reflection to the input is delay by the filter time.
Filter time: 7.5 µs (typ.) Dispersion: 5 to 10µs

8.12. Power Supply Monitor Circuit

This product has a power supply monitoring function for Vreg and V_{CC} voltage.

V_{CC} Power supply (24 V applied externally)
・V_{CC} (H) ≤ 9.0 V (typ.) V_{CC} (L) ≤ 8.0 V (typ.)

(Power supply ON)
In V_{CC} Power supply voltage rising, when the voltage is lower than 9.0V (typ.), the upper and lower FET is OFF and the internal logic is reset.

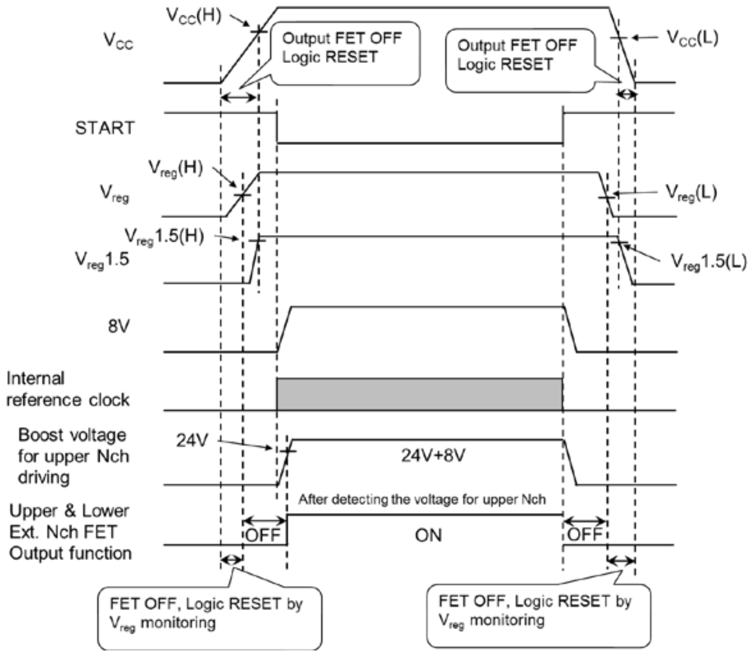
(Power supply OFF)
In V_{CC} Power supply voltage falling, when the voltage is lower than 8.0V (typ.), the upper and lower FET is OFF and the internal logic is reset.

* This product includes another V_{CC} monitoring function to protect boosting voltage. (Refer to 8.17.Function to avoid boosting power supply voltage V_{CC}.)

Vreg power supply (5 V, internal reference power supply)
・Vreg (H) ≤ 4.2 V (typ.) Vreg (L) ≤ 3.5 V (typ.)

(Power supply ON)
In V_{CC} Power supply voltage rising, when the voltage is lower than 4.2V (typ.), the upper and lower FET is OFF and the internal logic is reset.

(Power supply OFF)
In V_{CC} Power supply voltage falling, when the voltage is lower than 3.5 V (typ.), the upper and lower FET is OFF and the internal logic is reset.



Power supply sequence

The right figure shows a general operation.
When the input signal is entered, and the voltage with incomplete Vreg potential is entered, the power supply monitoring of Vreg operates.
When the power supply is turned off during rotating the motor, V_{CC} power supply monitoring operates.

Vreg 1.5V power supply (internal logic power supply)
・Vreg1.5 (H) ≤ 1.4 V (typ.) Vreg1.5 (L) ≤ 1.3 V (typ.)

(Power supply ON)
When VCC is rising, the Vreg voltage output starts up. Vreg 1.5 starts up at V_{CC} > 9.0 V and Vreg > 4.2 V.
When Vreg1.5 voltage is lower than 1.4 V, external upper and lower FET is set to OFF and the internal logic is reset.

(Power supply OFF)
When V_{CC} is falling, the Vreg voltage output falls. Vreg 1.5 shuts down at V_{CC} < 8.0V or Vreg < 3.5 V.
When Vreg1.5 voltage is lower than 1.3V, external upper and lower FET is set to OFF and the internal logic is reset.

<In case of startup>

In the following startup conditions, two times of FG pulse are D-OUT = L, and are full accelerated mode.

(1) BRAKE = L (Brake) to H (Brake release), at START = L (Start)

(2) After START = H (Standby) to L (Start) and detecting upper Nch voltage, at BRAKE = H (Brake release)

(Voltage detection of upper Nch)

When CP3 voltage output starts, the output is ON at CP3 voltage – Vcc> 6.35V (typ.). When CP3 voltage output shuts donw, the output is off at CP3 voltage – Vcc < 5.8V (typ.).

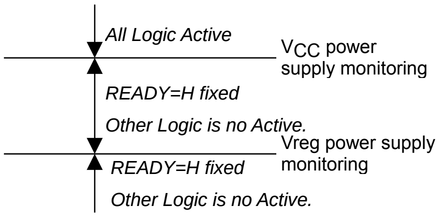
<Standby>

D-OUT = L, and P-OUT = L are fixed.

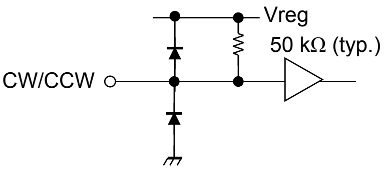
In case of START = H,

Other logic is invalid in the fixation of READY = H.

Power supply monitoring and Logic in case of START=L



8.13. CW / CCW Circuit



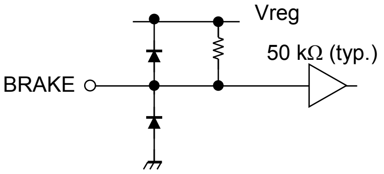
The input is TTL input and includes 5 V pull-up resistor inside.
To avoid malfunction by input noise, a CR filter is included in back of the input buffer.
The reflection to the input is delay by the filter time.
Filter time: 7.5 μs (typ.) Dispersion: 5 to 10μs

CW/CCW input	Mode
H	CCW
L	CW

CW: Hall element signal: $HU^{+} \rightarrow HV^{+} \rightarrow HW^{+}$

Output FET could be destroyed with counter torque, if switched CW/CCW suddenly.

8.14. BRAKE



The input is TTL input and includes 5 V pull-up resistor inside.

BRAKE input	Mode
H	OPERATION
L	BRAKE

BRAKE: Lower output Nch all phases ON

Output FET could be destroyed, if switched from high speed rotating to brake-on suddenly.

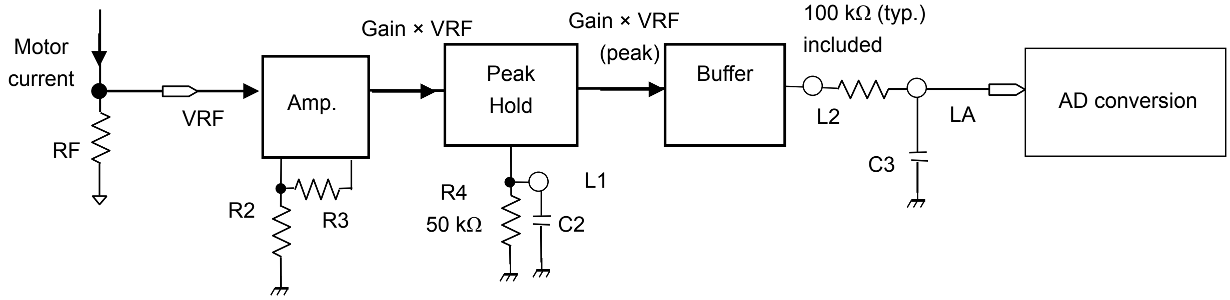
* In the following state, Output-off has higher priority so brake function does not work.
V_{CC} is lower than the voltage monitoring level, charge pump is not working for driving upper side Nch FET.

* In the following state, brake function works if BRAKE = L.
V_{CC} voltage bounce protection is working, over-current limitation circuit is working.

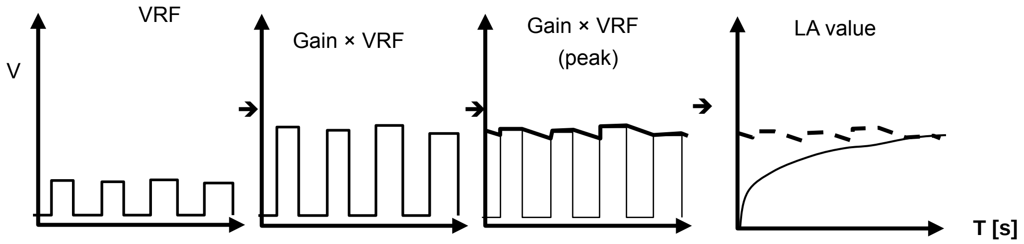
To avoid malfunction by input noise, a CR filter is included in back of the input buffer.
The reflection to the input is delay by the filter time.
Filter time: 7.5 μs (typ.) Dispersion: 5 to 10μs

8.15. Automatic Phase Lead Angle Adjustment Circuit

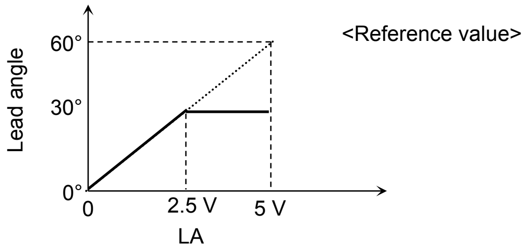
This product includes the circuit which adjusts a lead angle using a motor current value. (Automatic lead angle adjustment)



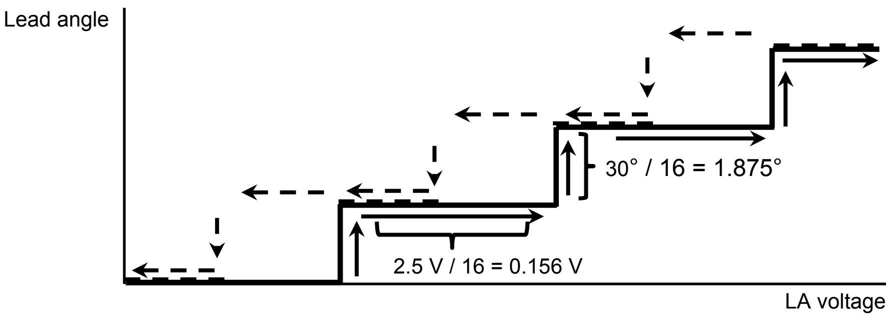
*) Gain = (R2 + R3) / R2 = 17 times fixed, R4 resistor included



Phase of energization signal can be leaded by inputting voltage whose range is 0 to 2.5 V (16 steps).
0 V -> 0°
2.5 V -> 30° (If the LA voltage of 2.5 V or more is input, the lead angle is 30°)



LA voltage is clumped at 30° (max) of lead angle. Input voltage is not clumped. It is clumped at 30° setting internal logically.



1 step = 2.5 / 16 = 0.156 V
The hysteresis width is a half of the above value.

(Timing of lead angle reflection)

The timing of the reflection of lead angle is reflected once per 16 cycles of hall signal (HU) data.
The first lead angle after starting rotations is reflected at the timing of 16th rising of hall HU after switching to 180° energization.

10 axis ⇒16/(10/2) = Once per 3.2 rotations
16 axis ⇒16/(16/2) = One per 2 rotations

8.16. Lock Protection Circuit

This is the function to turn off the output power FET when motor is locked.
When the READY signal is detected and the following condition is matched, the upper and lower output FET is turned off.
The latch state of this circuit is released by making it the stop state or brake state at once.

Detection signal	Condition to operate the lock protection circuit
READY signal	READY signal output: HZ continues for 1 s (typ.) or 3 s (typ.)

The lock detection time is set with a feedback current gain by the input voltage of CLD pin.

When CLD voltage is configured by resistance divider, please set the Vreg supply by the following resistance value. ”
The resistance should use the thing of ±5% of precision.

External resistor (kΩ)		CLD pin Input voltage (V)		Mode	Lock detection time	Current feedback gain constant
R1	R2	min	max			
100	0	0.00	0.48	Invalid	-	0
82	18	0.68	1.07	Latch	1 (s)	0.0625
68	27	1.27	1.65			0.125
56	38	1.85	2.23			0.5
47	51	2.43	2.82		3 (s)	0.0625
36	62	3.02	3.40			0.25
0	100	3.60	Vreg			0.5

Note: The lock detection time 1 (s) and 3 (s) have different two modes of current feedback gain constants, which are 0.125 and 0.25.
Note: CLD pin voltage is detected every 3.2 ms and switched after continuing three times of same mode.

8.17. Function to avoid boosting power supply voltage Vcc

This product includes the function to avoid boosting power supply voltage in a sharp deceleration state. When the function works, the driving system is changed from synchronous rectification state to 120° driving (Upper side PWM) state.

Switching the energization mode uses following two judgments;

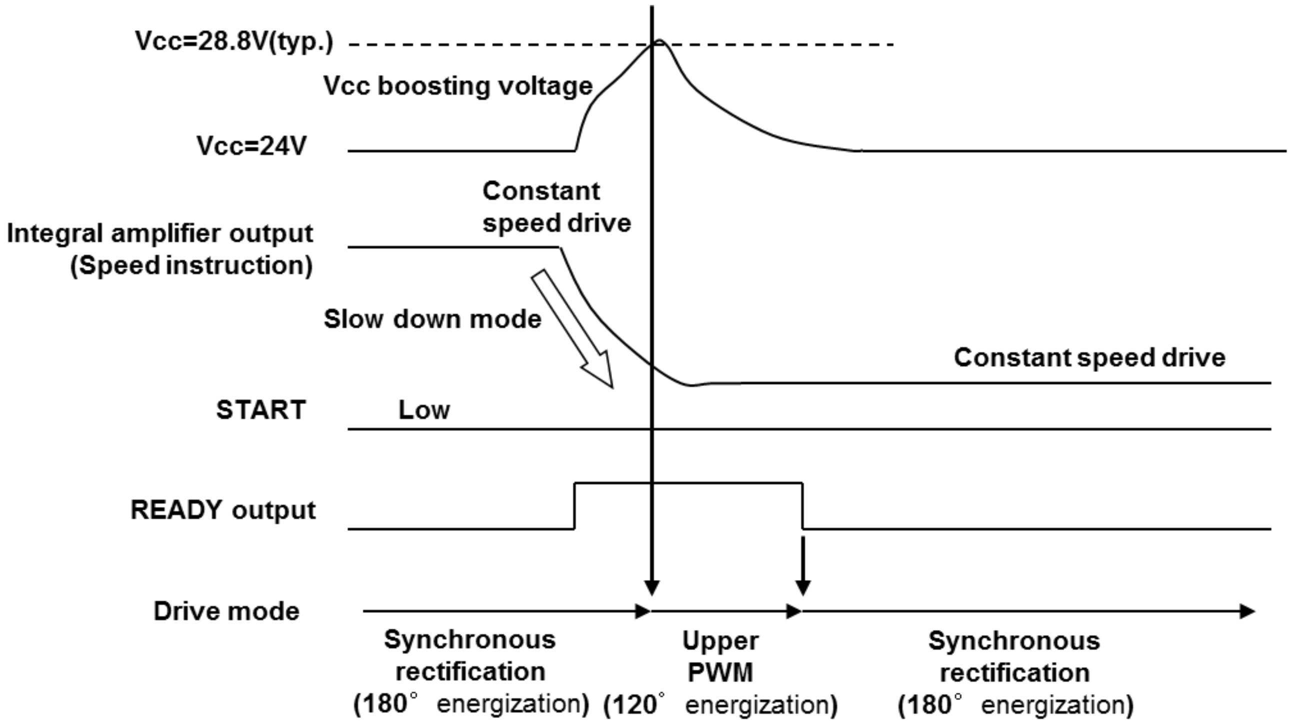
(1) Synchronous rectification to upper PWM condition

When the Vcc power supply voltage is monitored, and is more than 28.8 V (typ.), the synchronous rectification (180° energization) is switched to upper PWM (120° energization).

(2) Upper PWM to synchronous rectification condition

If the operating condition is in the constant operating (READY = Low), the upper PWM (120° energization) is switched to the synchronous rectification (180° energization).

<Boosting voltage avoiding mode (normal) >



The maximum Vcc of the power supply voltage to be used in normal operation should be set VK = 27.8 V or less.

Note: This function does not avoids all boosting power supply voltage. Please add other boosting protection circuit if the power supply voltage is boosted by a factor of a power supply circuit.

8.18. Constant Voltage Circuit

(1) Vreg

5 V voltage for internal logic bias is output from Vreg pin.
Connect capacitor (recommended value: 0.1 to 1μF) between Vreg pin and GND to avoid the oscillation or noise absolutely.

(2) Vreg1.5

1.5V power supply is included as Logic power supply.
Connect capacitor (recommended value: 0.1 to 1μF) surely close to the IC.

(3) 8 V power supply

8 V power supply is generated in the IC as the gate drive circuit of output FET.

8.19. Over Current Limitation Circuit

When detect voltage become higher than 0.25 V (typ.), all upper side power FET attached external is off.
The off mode is cleared on every career frequency.
(Detect-> Off on synchronous rectification part, PWM Duty = 0. The channel that lowers side full-on keeps on state.)
Note: Idc pin has high sensitivity as it is input to analog comparator directly, so add a filter comprised of C, R externally to prevent malfunctions from noise of output current chopping.
Idc1 pin is output OFF at open.

Note: These protection functions are functions to avoid abnormal conditions, such as an output short circuit, temporarily, and it does not guarantee that IC does not break.

8.20. Current Feedback

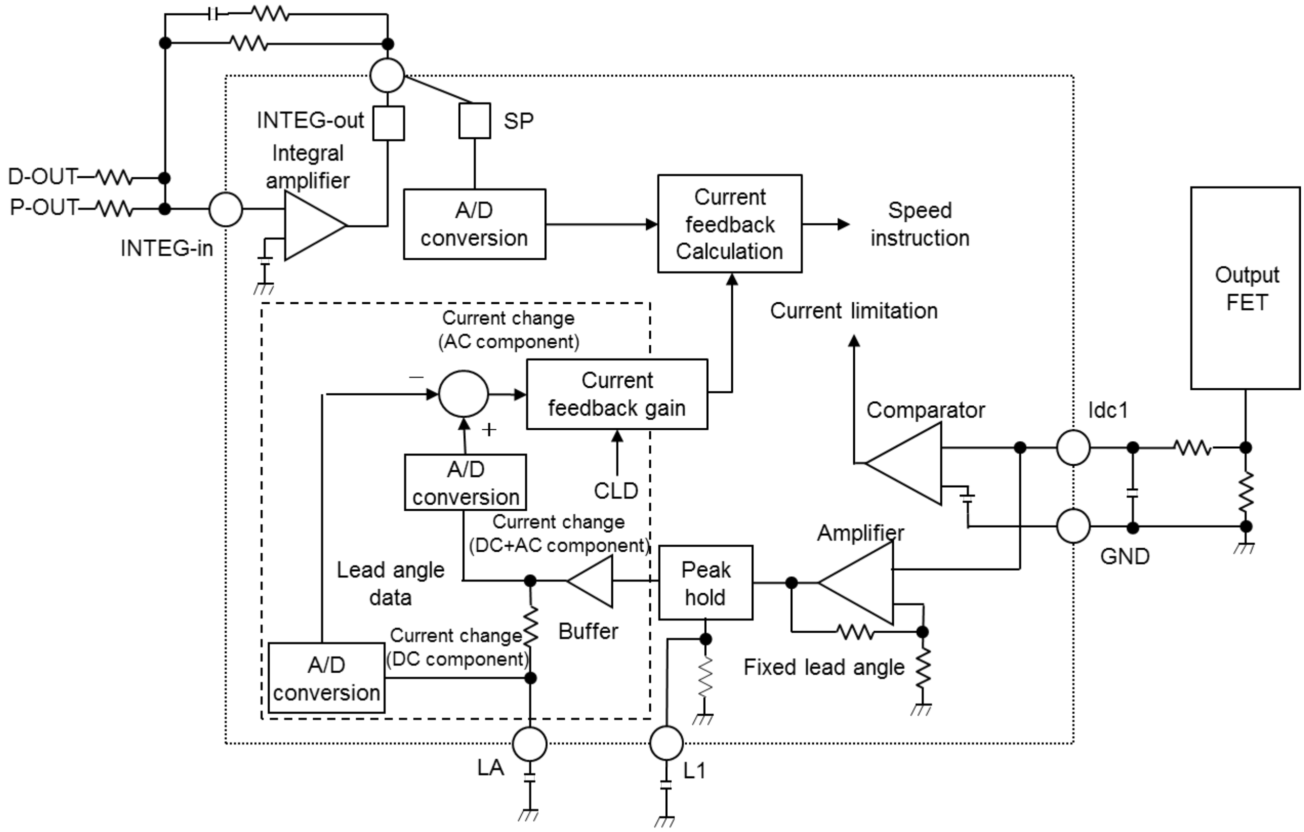
To avoid irregular rotation, current feedback functions are included to suppress the fluctuation of motor current (power supply current).
The system which makes the current fluctuation feedback to the speed control is used.

<Function of current detection block>

As functions using current (detected resistor voltage),

- Current limitation function
- Current feedback function
- Automatic lead-angle function

are included. The circuit configuration is as follows.



The current feedback gain is set with the CLD voltage.
When CLD voltage is configured by resistance divider, please set the Vreg supply by the following resistance value.
The resistance should use the thing of ±5% of precision.

External resistor (kΩ)		CLD pin Input voltage (V)		Mode	Lock detection time	Current feedback gain constant
R1	R2	min	max			
100	0	0.00	0.48	Invalid	-	0
82	18	0.68	1.07	Latch	1 (s)	0.0625
68	27	1.27	1.65			0.125
56	38	1.85	2.23			0.5
47	51	2.43	2.82		3 (s)	0.0625
36	62	3.02	3.40			0.25
0	100	3.60	Vreg			0.5

Note: The lock detection time 1 (s) and 3 (s) have different two modes of current feedback gain constants, which are 0.125 and 0.25.
Note: CLD pin voltage is detected every 3.2 ms and switched after continuing three times of same mode.

9. Electrical Characteristics

Electrical Characteristics (1) (VCC = 24 V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Supply current		I_{CC1}	START = L	3	5	8	mA
		I_{CC2}	START = H, Standby mode	0.3	0.5	0.7	
Hall amplifier	Common mode input voltage range	VCMRH	-	0.5	-	3.5	V
	Input amplitude range	VH	-	50	-	-	mVpp
	Input hysteresis	VhysH	-	8	16	24	mV
	Input current	IinH	VCMRH = 2.5 V, single phase	0	-	1	μA
READY circuit	Output remaining voltage	VCER	Open corrector output ICER = 2 mA	0.1	-	0.5	V
	Output leak current	ILR	Vready = 5 V	0	-	1	μA
FG amplifier	Input offset voltage	VOSFG	-	0	-	±7	mV
	Output remaining volage (upper)	VOFG (H)	IFG = 100 μA (Source current)	Vreg -1.2	-	Vreg	V
	Output remaining volage (lower)	VOFG (L)	IFG = 100 μA (Sink current)	-	-	1.2	
	Reference voltage	VrefFG	-	2.2	Vreg/2	2.8	V
FG hysteresis comparator	Hysteresis width	VhysS	-	0.20	0.25	0.30	V
Control input circuit	Input voltage (H)	Vin (H)	CW/CCW, BRAKE, and START	2.0	-	5.5	V
	Input voltage (L)	Vin (L)		0	-	0.8	
	Input current (H)	Iin (H)	CW/CCW, BRAKE, and START Vin = Vreg	0	-	1	μA
	Input current (L)	Iin (L)	CW/CCWBRAKE,START Vin = GND	70	100	150	
Fref Input circuit	Input voltage (H)	Vin (H)	Fref	2.0	-	5.5	V
	Input voltage (L)	Vin (L)	Fref	0	-	0.8	
	Input current (H)	Iin (H)	Vin = Vreg	0	-	1	μA
	Input current (L)	Iin (L)	Vin = GND	70	100	150	
Charge pump voltage		VG	CP1 - CP2: 0.047 μF CP3: 0.1 μF	Vcc + 7	Vcc + 8	Vcc + 9	V
Energization signal output voltage		VO (U) - (H)	LA(U)/LB(U)/LC(U) Io = 1 mA	VG - 1.5	-	VG	V
		VO (U) - (L)	LA(U)/LB(U)/LC(U) Io = 5 mA	0.1	-	0.825	
		VO (L) - (H)	LA(U)/LB(U)/LC(U) Io = 1 mA	6.9	7.7	8.5	
		VO (L) - (L)	LA(U)/LB(U)/LC(U) Io = 5 mA	0.1	-	0.775	
Internal voltage source output (5V)		Vreg5	Ireg5 = 10 mA	4.5	5.0	5.5	V
Internal voltage source output(1.5V)		Vreg1.5	-	1.4	1.5	1.6	V
Current limiter circuit reference voltage		Vdc	-	0.23	0.25	0.27	V
Internal reference clock frequency		fx	R = 2.4 kΩ, C = 100 pF	4.5	5.0	5.5	MHz
Dead time		TOFF1	R = 2.4 kΩ, C = 100 pF	0.9	1.2	1.5	μs
		TOFF2	R = 2.4 kΩ, C = 100 pF	0.9	1.2	1.5	
Lead angle control circuit	Upper side clump lead angle	ACLH	-	-	30	-	°

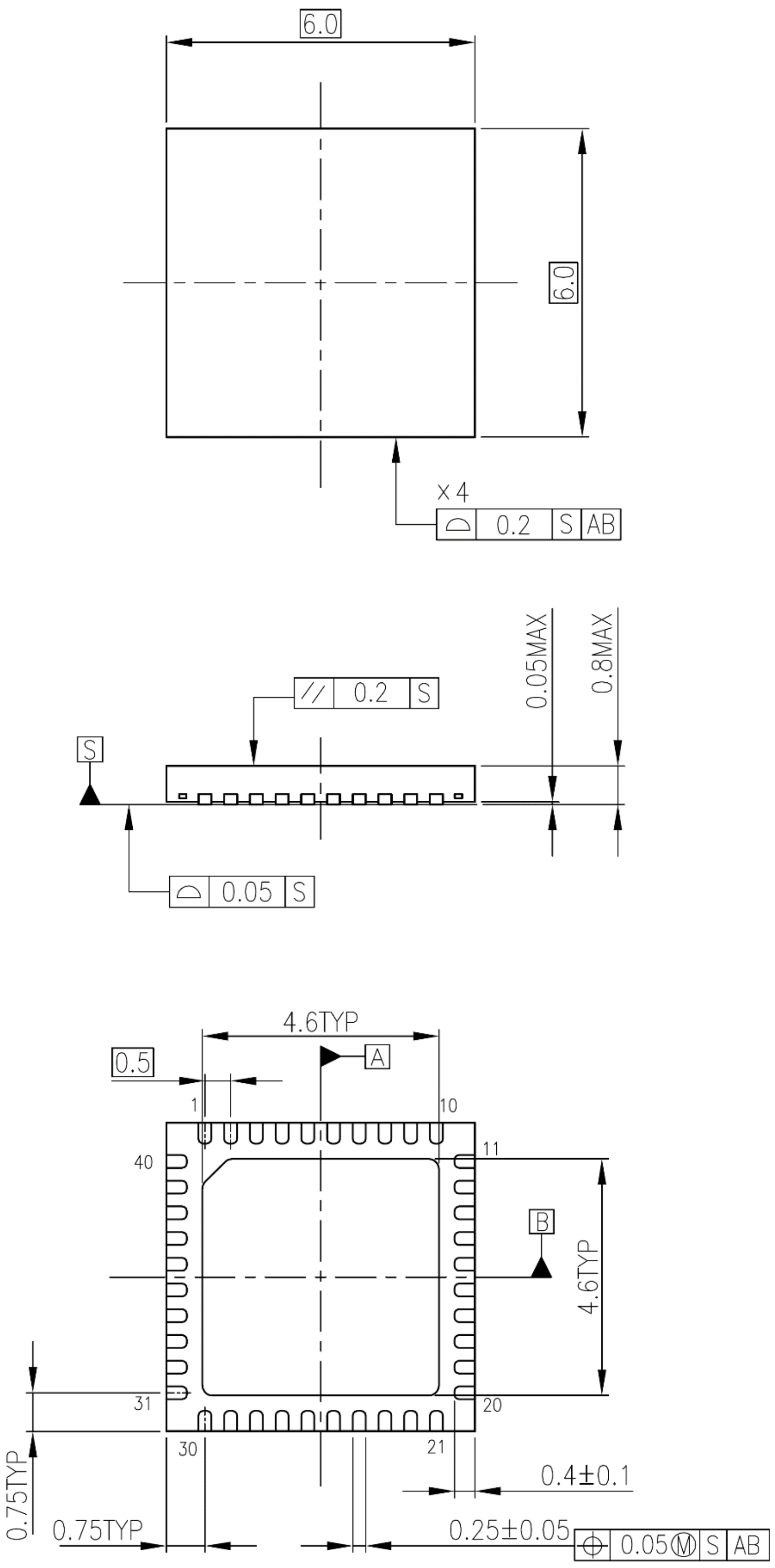
Electrical characteristics (2) (V_{CC} = 24 V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Integral amplifier circuit	Reference voltage	Vr	-	2.1	2.25	2.4	V
	Output High level voltage	Vint (H)	-	3.25	3.5	3.75	
	Output Low level voltage	Vint (L)	-	-	-	0.3	
	Input bias current	IB (int)	-	-1	-	1	μA
	Input offset voltage	VOSFG	-	0	-	±7	mV
	Open loop GAIN	A_{OL}	(Target design value)	-	100	-	dB
Speed FLL output (D-OUT output)	Max output voltage	VD (H)	-	3.25	3.5	3.75	V
	Reference voltage	VrD	-	2.1	2.25	2.4	
	Reference voltage deviation	ΔVrd	Vr - VrD	0	-	±10	mV
	Min output voltage	VD (L)	-	0.75	1.0	1.25	V
Speed PLL output (P-OUT output)	Max output voltage	VP (H)	-	3.25	3.5	3.75	
	Reference voltage	VrP	-	2.1	2.25	2.4	
	Reference voltage deviation	ΔVrP	Vr - VrP	0	-	±10	mV
	Min output voltage	VP (L)	-	0.75	1.0	1.25	V
Power supply monitor	Monitor voltage of PWM driving	VK	-	27.8	28.8	29.8	V

10. Package Dimensions

P-WQFN40-0606-0.50-001

"Unit:mm"



Weight: 0.0849 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Any license to any industrial property rights is not granted by provision of these application circuit examples.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(5) Others

Utmost care is necessary in the design of the output, V_{CC}, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

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