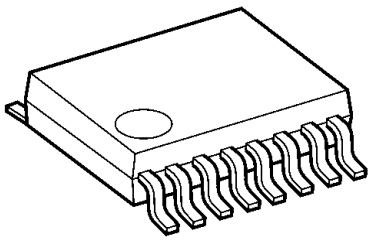
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

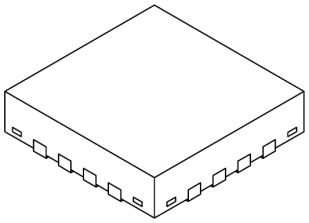
TC78B006FNG TC78B006FTG TC78B006AFNG TC78B006AFTG TC78B006BFNG TC78B006BFTG TC78B006CFNG TC78B006CFTG

Single Phase Full-wave Pre-driver for Fan Motor

The TC78B006 series are single phase full-wave pre-drivers for fan motors.



SSOP16-P-225-0.65B



P-WQFN16-0303-0.50-003

Weight:

SSOP16-P-225-0.65B 0.07g (typ.)

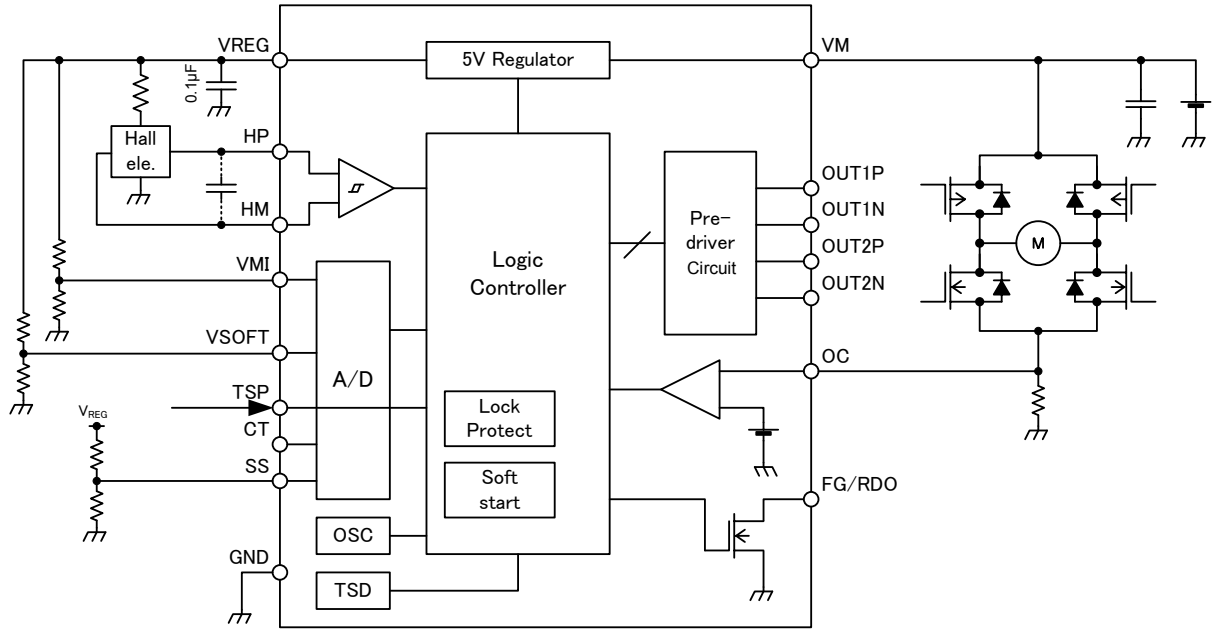
P-WQFN16-0303-0.50-003 0.02g (typ.)

Features

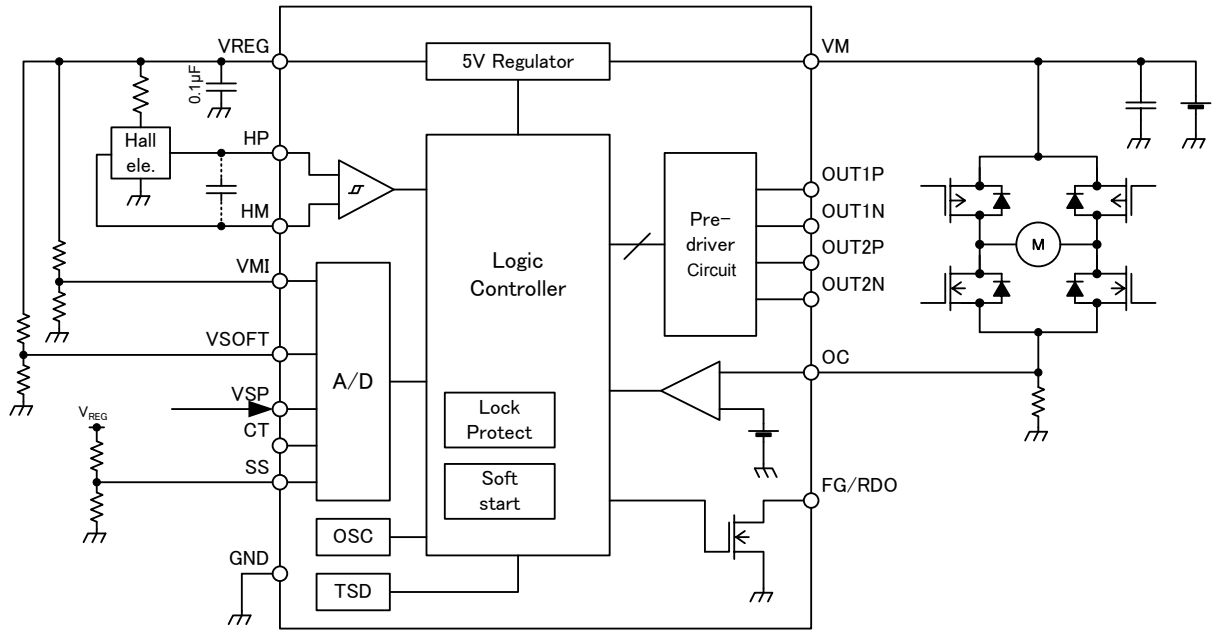
- Single-phase full-wave drive
- Motor power supply voltage: VM=30V (maximum operating range)
- Standby mode
- Output PWM control
- Built-in oscillation circuit
- Soft switching drive
- Lock protection, Automatic restart
- Quick start
- Soft start
- Built-in voltage regulator
- Current limit function
- Built-in thermal shut down circuit
- TC78B006FNG: Direct PWM input, Rotation Speed Detection output, SSOP16
  TC78B006FTG: Direct PWM input, Rotation Speed Detection output, WQFN16
  TC78B006AFNG: Direct PWM input, Lock Detection Output, SSOP16
  TC78B006AFTG: Direct PWM input, Lock Detection Output, WQFN16
  TC78B006BFNG: Analog voltage input, Rotation Speed Detection output, SSOP16
  TC78B006BFTG: Analog voltage input, Rotation Speed Detection output, WQFN16
  TC78B006CFNG: Analog voltage input, Lock Detection Output, SSOP16
  TC78B006CFTG: Analog voltage input, Lock Detection Output, WQFN16

Block Diagram (Application circuit)

Direct PWM input (TSP) type

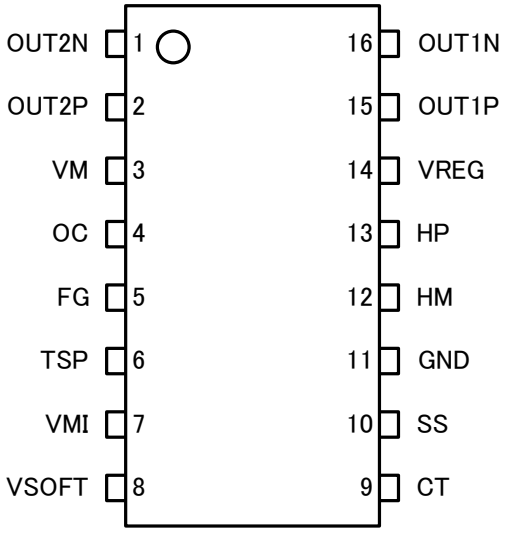


Analog voltage input (VSP) type

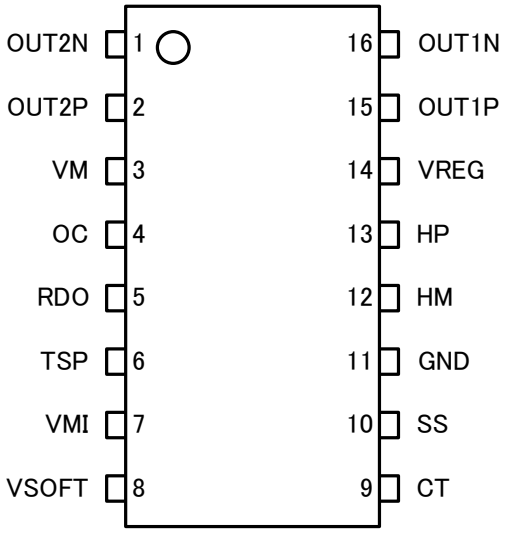


Pin Assignment

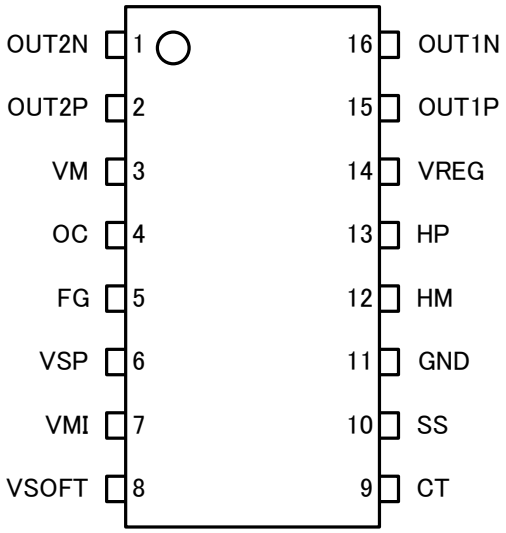
■ FNG Direct PWM input (TSP 6pin), Rotation speed detection output (FG 5pin)



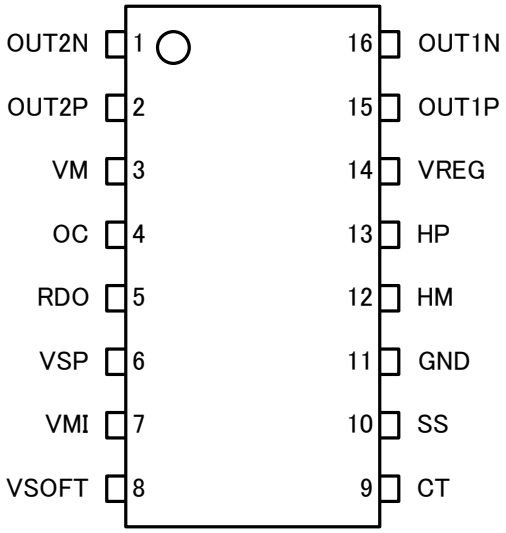
■ AFNG Direct PWM input (TSP 6pin), Lock detection output (RDO 5pin)



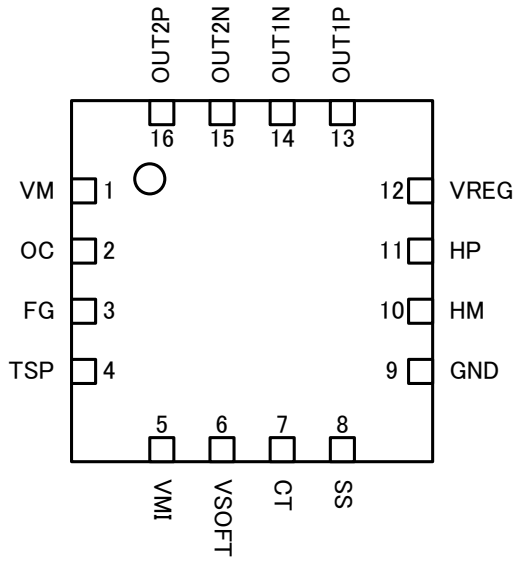
■ BFNG Analog voltage input (VSP 6pin), Rotation speed detection output (FG 5pin)



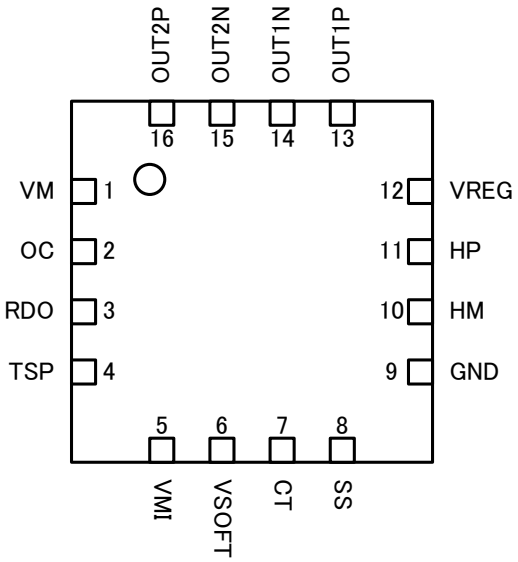
■ CFNG Analog voltage input (VSP 6pin), Lock detection output (RDO 5pin)



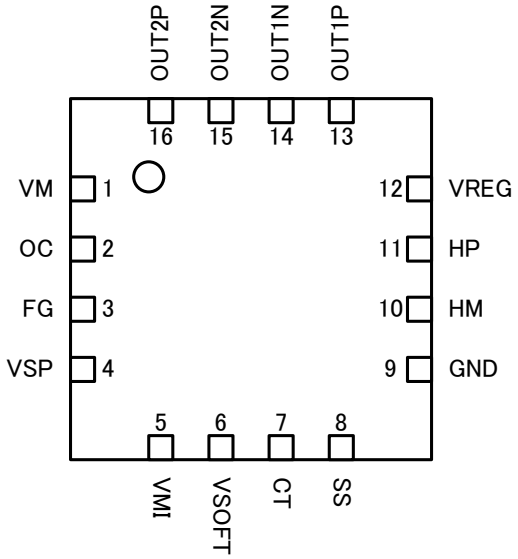
■ FTG　Direct PWM input (TSP 4pin), Rotation speed detection output (FG 3pin)



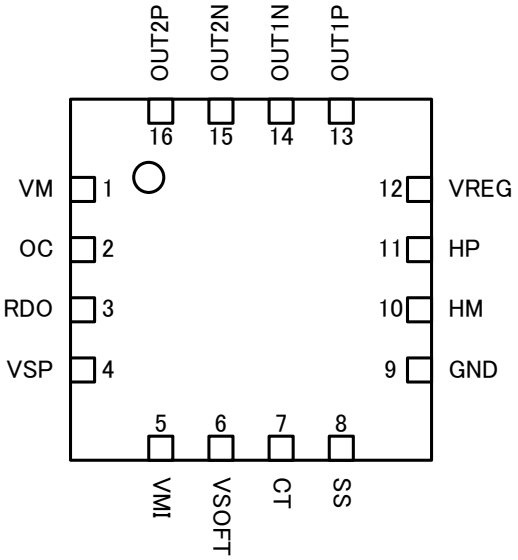
■ AFTG　Direct PWM input (TSP 4pin), Lock detection output (RDO 3pin)



■ BFTG　Analog voltage input (VSP 4pin), Rotation speed detection output (FG 3pin)



■ CFTG　Analog voltage input (VSP 4pin), Lock detection output (RDO 3pin)



Pin Description

■ FNG/FTG Direct PWM input (TSP), Rotation speed detection output (FG) type

Pin No.		Pin name	Description
FNG	FTG		
14	12	VREG	Output pin for reference voltage of 5 V
13	11	HP	Hall signal input pin +
12	10	HM	Hall signal input pin -
3	1	VM	Power supply pin
11	9	GND	Connection pin for ground
15	13	OUT1P	Output pin 1 for high side drive
16	14	OUT1N	Output pin 1 for low side drive
2	16	OUT2P	Output pin 2 for high side drive
1	15	OUT2N	Output pin 2 for low side drive
4	2	OC	Current limit detection pin
5	3	FG	Rotating output pin
6	4	TSP	Setting pin for output duty
7	5	VMI	Setting pin for minimum output duty
8	6	VSOFT	Adjusting pin for soft switching
9	7	CT	Setting pin for lock protection term
10	8	SS	Setting pin for soft start term

■ AFNG/AFTG Direct PWM input (TSP), Lock detection output (RDO) type

Pin No.		Pin name	Description
AFNG	AFTG		
14	12	VREG	Output pin for reference voltage of 5 V
13	11	HP	Hall signal input pin +
12	10	HM	Hall signal input pin -
3	1	VM	Power supply pin
11	9	GND	Connection pin for ground
15	13	OUT1P	Output pin 1 for high side drive
16	14	OUT1N	Output pin 1 for low side drive
2	16	OUT2P	Output pin 2 for high side drive
1	15	OUT2N	Output pin 2 for low side drive
4	2	OC	Current limit detection pin
5	3	RDO	Output pin for lock detection signal
6	4	TSP	Setting pin for output duty
7	5	VMI	Setting pin for minimum output duty
8	6	VSOFT	Adjusting pin for soft switching
9	7	CT	Setting pin for lock protection term
10	8	SS	Setting pin for soft start term

■ BFNG/BFTG Analog voltage input (VSP), Rotation speed detection output (FG) type

Pin No.		Pin name	Description
BFNG	BFTG		
14	12	VREG	Output pin for reference voltage of 5 V
13	11	HP	Hall signal input pin +
12	10	HM	Hall signal input pin -
3	1	VM	Power supply pin
11	9	GND	Connection pin for ground
15	13	OUT1P	Output pin 1 for high side drive
16	14	OUT1N	Output pin 1 for low side drive
2	16	OUT2P	Output pin 2 for high side drive
1	15	OUT2N	Output pin 2 for low side drive
4	2	OC	Current limit detection pin
5	3	FG	Rotating output pin
6	4	VSP	Setting pin for output duty
7	5	VMI	Setting pin for minimum output duty
8	6	VSOFT	Adjusting pin for soft switching
9	7	CT	Setting pin for lock protection term
10	8	SS	Setting pin for soft start term

■ CFNG/CFTG Analog voltage input (VSP), Lock detection output (RDO) type

Pin No.		Pin name	Description
CFNG	CFTG		
14	12	VREG	Output pin for reference voltage of 5 V
13	11	HP	Hall signal input pin +
12	10	HM	Hall signal input pin -
3	1	VM	Power supply pin
11	9	GND	Connection pin for ground
15	13	OUT1P	Output pin 1 for high side drive
16	14	OUT1N	Output pin 1 for low side drive
2	16	OUT2P	Output pin 2 for high side drive
1	15	OUT2N	Output pin 2 for low side drive
4	2	OC	Current limit detection pin
5	3	RDO	Lock detection output pin
6	4	VSP	Setting pin for output duty
7	5	VMI	Setting pin for minimum output duty
8	6	VSOFT	Adjusting pin for soft switching
9	7	CT	Setting pin for lock protection term
10	8	SS	Setting pin for soft start term

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_M	40	V
		V_{REG}	6 (Note 1)	
Input voltage	VMI, VSOFT, CT, SS, OC HP, HM	V_{IN}	-0.3 to 6	V
	TSP, VSP		-0.3 to 40	
Output voltage	OUT1P, OUT2P, FG, RDO	V_{OUT}	40	V
	OUT1N, OUT2N		15 (Note 2)	
Output current	OUT1P, OUT2P	I_{OUT}	20	mA
	OUT1N, OUT2N		-20	
	VREG		-10	
	FG, RDO		10	
Power dissipation		P_D	0.96 (Note 3)	W
			2.5 (Note 4)	
Operating temperature		T_{opr}	-40 to 105	°C
Storage temperature		T_{stg}	-55 to 150	°C

As for current items, current flowing to the IC is indicated “plus” and that flowing from the IC is indicated “minus”.

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

Note 1: Voltage of V_{REG} is generated in the IC. Do not apply the voltage from external.

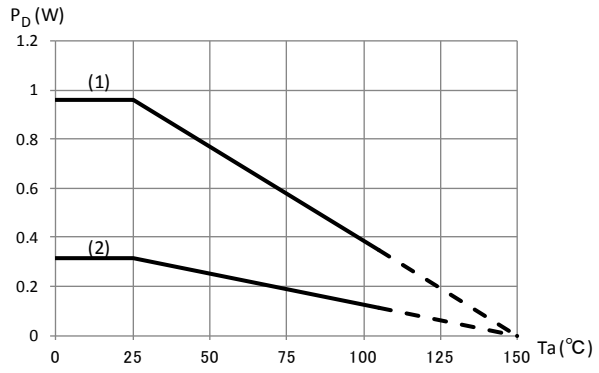
Note 2: Voltages of OUT1N and OUT2N are generated in the IC. Do not apply the voltage from external.

Note 3: TC78B006FNG/AFNG/BFNG/CFNG when mounted on a glass epoxy board, (40mm×30mm×1.6mm, 2-layer FR-4 board)

Note 4: TC78B006FTG/AFTG/BFTG/CFTG when mounted on a glass epoxy board, (74mm×74mm×1.6mm, 4-layer FR-4 board)

Package Power Dissipation

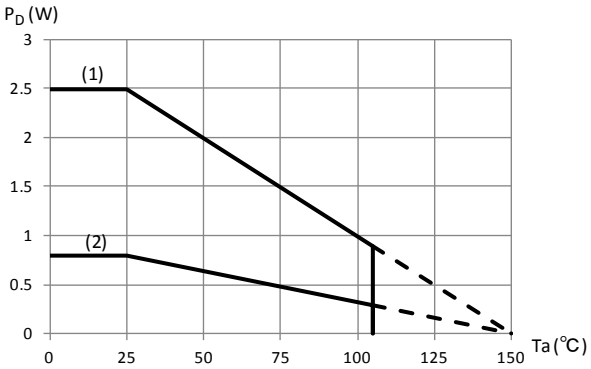
TC78B006FNG/AFNG/BFNG/CFNG



(1) When mounted on the board, Rth(j-a)=130°C/W
(40mm×30mm×1.6mm 2-layer FR-4 board)

(2) IC only
Rth(j-a)=400°C/W

TC78B006FTG/AFTG/BFTG/CFTG



(1) When mounted on the board, Rth(j-a)=50°C/W
(74mm×74mm×1.6mm 4-layer FR-4 board)

(2) When mounted on the board, Rth(j-a)=160°C/W
(Φ40mm×1.6mm 1-layer FR-4 board)

Operating Ranges (Ta = 25°C)

Characteristics		Symbol	Min	Typ.	Max	Unit
VM power supply voltage		VM_{opr1}	5.5	12	30	V
VM power supply for low voltage operation		VM_{opr2}	3.5	—	5.5	V
VREG power supply voltage		V_{REG1}	4.5	5	5.5	V
VREG power supply for low voltage operation		V_{REG2}	3.3	—	5.5	V
Input PWM frequency		$f_{TSP\ IN}$	1	—	100	kHz
Input voltage	VMI, VSOFT, CT, SS	V_{IN}	-0.3	—	V_{REG}	V
	TSP, VSP		-0.3	—	5.5	

Note: In low-voltage operation, electrical characteristics are not covered under guarantee because the variation of the characteristics becomes large.

Electrical Characteristics (Ta = 25°C, V_M = 12V, unless otherwise specified.)

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Power supply current		I_{VM}	V_M=12 V, V_{REG}=OPEN Hall input=100Hz, output OPEN	—	4.5	6	mA
		$I_{VM\ ST}$	Standby mode	—	0.5	1	mA
Hall signal input	Common phase input voltage range	V_{CMRH}	(Design target value) (Note 1)	0	—	V_{REG} -1.5	V
	Input voltage swing	V_H		40	—	—	mV
	Input current	I_H	$\|V_{HP}-V_{HM}\| \geq 100mV$	—	—	1	μA
	Hysteresis+ Voltage	V_{HHYS+}	(Design target value) (Note 1)	—	10	—	mV
	Hysteresis- Voltage	V_{HHYS-}	(Design target value) (Note 1)	—	-10	—	mV
VREG pin voltage		V_{REG}	I_{VREG}=-10mA	4.5	5	5.5	V
Maximum voltage of ADC convertor		V_{ADC}	(Design target value) (Note 1)	—	V_{REG} -0.75	—	V
TSP pin	Input voltage	$V_{TSP\ (L)}$	Low voltage	-0.3	—	1.0	V
		$V_{TSP\ (H)}$	High voltage	2.0	—	5.5	
	Input current	I_{TSP}	Input voltage 0V to V_{REG}	—	—	1	μA
	Input frequency	f_{TSP}		1	—	100	kHz
	full Duty detection term	T_{full}		1.1	1.6	2.1	ms
	Stop command detection term	T_{stop}		70	100	130	ms
VSP pin	Input voltage	$V_{VSP(L)}$	Threshold voltage of stopping output	1.35	1.5	1.65	V
		$V_{VSP(H)}$	Threshold voltage of full output	3.3	3.6	3.9	V
	Input current	I_{VSP}	In normal operation, Input voltage 0V to V_{REG}	—	—	1	μA
	Response time	T_{VSP}	(Design target value) (Note 1)	—	—	10	ms
Standby mode	Transition voltage	$V_{STBY(L)}$	TSP, VSP pins	1	—	—	V
	Recover voltage	$V_{STBY(H)}$	TSP, VSP pins	—	—	1.3	
FG/RDO pin	Output Low voltage	$V_{OUT(L)}$	$I_{FG/RDO}$=5mA	—	—	0.3	V
	Output leakage current	$I_{OUT(H)}$	$V_{FG/RDO}$=5V	—	—	1	μA
Pin input current		I_{IN}	VSOFT,SS pins Input voltage 0V to V_{REG}	—	—	1	μA
			VMI pin Input voltage 0V to V_{REG}	—	—	2	
			CT pin Input voltage=0V	-130	-100	-70	
			CT pin Input voltage=V_{REG}	70	100	130	
High side output current		$I_{OUTP(L)}$	V_{OUTP}=12V	9	11	13	mA
High side output leakage current		$I_{OUTP(H)}$	V_{OUTP}=12V	—	—	1	μA
High voltage of low side output		$V_{OUTN(H)}$	I_{OUTN}=-5mA	9	10	11	V
Low voltage of low side output		$V_{OUTN(L)}$	I_{OUTN}=5mA	—	0.5	0.75	V
Internal oscillation frequency		f_{OSC}	Measured by internal divided frequency	7	10	13	MHz
Output PWM frequency		f_{PWM}		28	40	52	kHz
Current limit detecting voltage for OC pin		V_{OC}		135	150	165	mV
Masking time of current limit circuit		T_{MASK}	(Design target value) (Note 1)	—	2	—	μs
Voltage for VM low voltage detection		V_{UVLO}	Operation voltage (Design target value) (Note 1)	2.6	2.9	3.2	V
		V_{PORRL}	Recover voltage (Design target value) (Note 1)	2.9	3.2	3.5	V

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Operating temperature of thermal shutdown circuit	T_{SD}	Junction temperature (Design target value) (Note 1)	—	165	—	°C
Hysteresis of thermal shutdown circuit	ΔT_{SD}	(Design target value) (Note 1)	—	40	—	°C

As for current items, current flowing to the IC is indicated “plus” and that flowing from the IC is indicated “minus”.

Note 1: Toshiba does not implement testing before shipping.

Reference Data

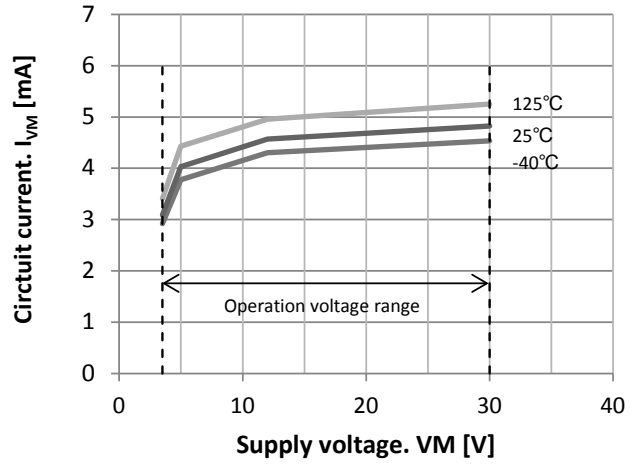


Fig.1 Power supply current

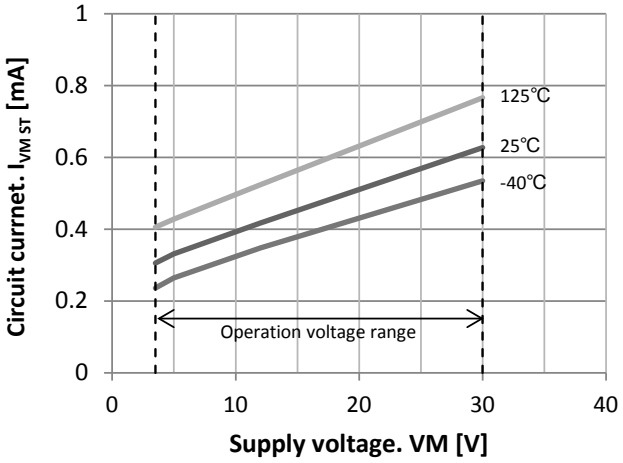


Fig.2 Power supply current (Standby mode)

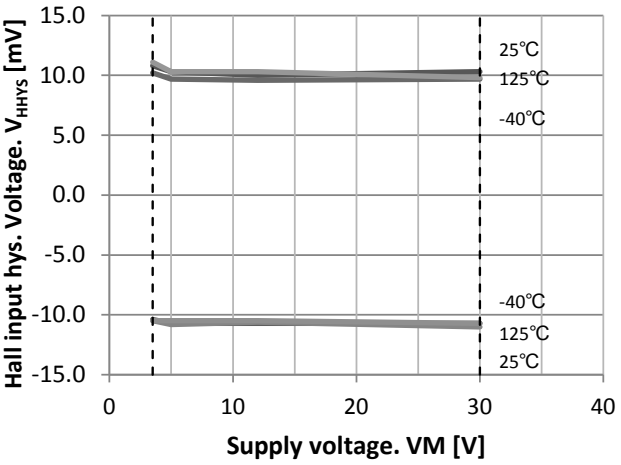


Fig.3 Hall input hysteresis voltage

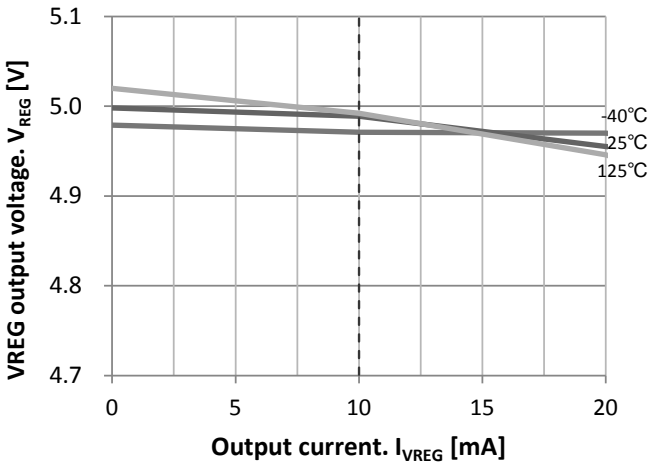


Fig.4 Voltage of VREG pin (VM=12V)

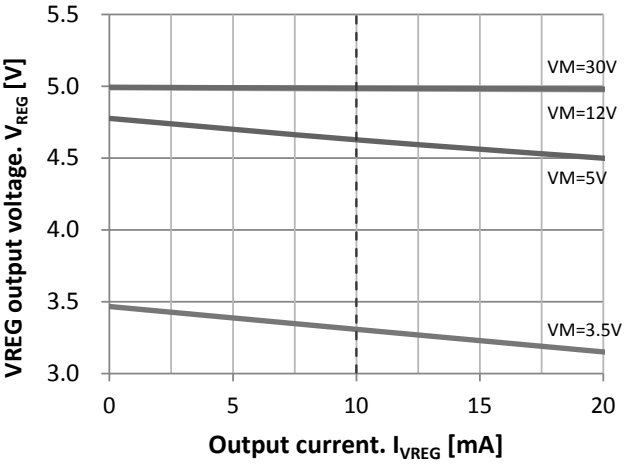


Fig.5 Voltage of VREG pin (Ta=25°C)

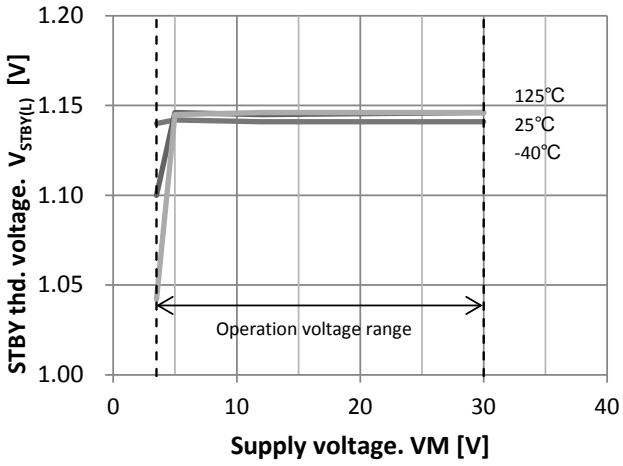


Fig.6 Transition voltage of standby mode

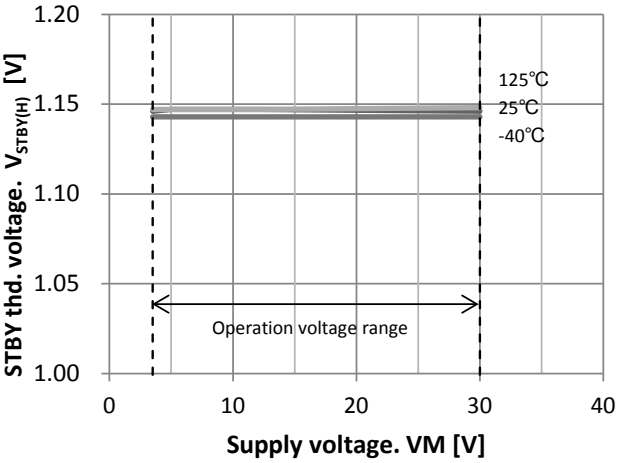


Fig.7 Recover voltage of standby mode

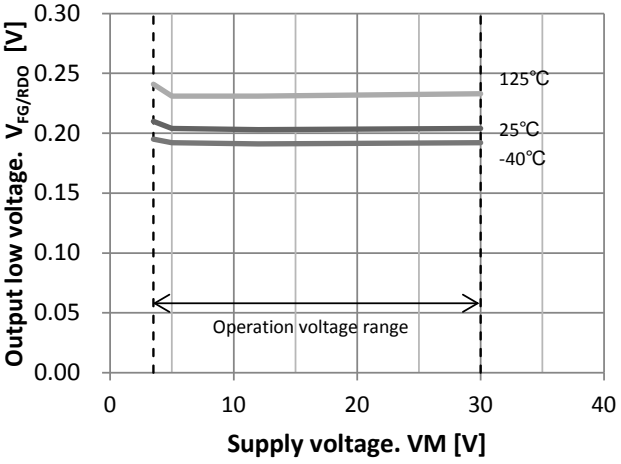


Fig.8 Output low voltage of FG/RDO pin ($I_{FG/RDO}$=-5mA)

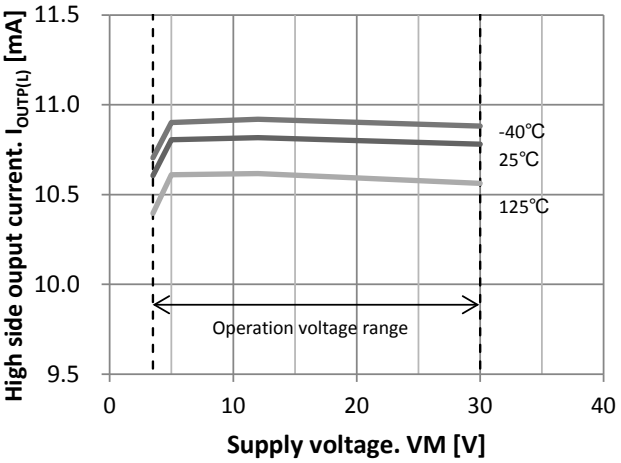


Fig.9 High side output current

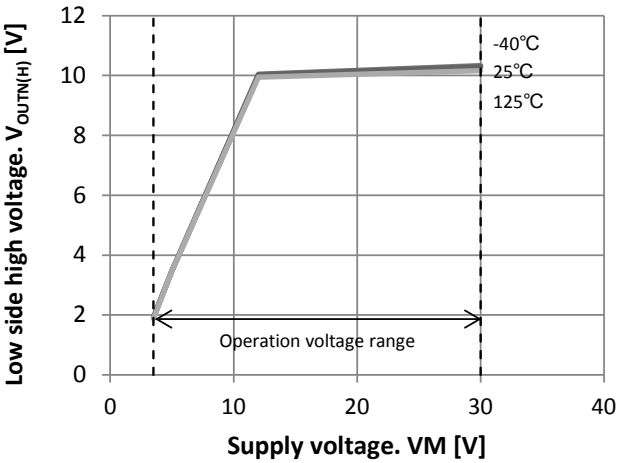


Fig.10 High voltage of low side output (I_{OUTN}=-5mA)

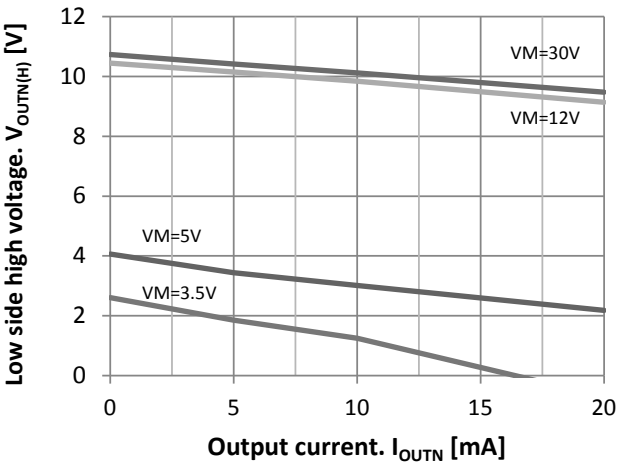


Fig.11 High voltage of low side output (Ta=25°C)

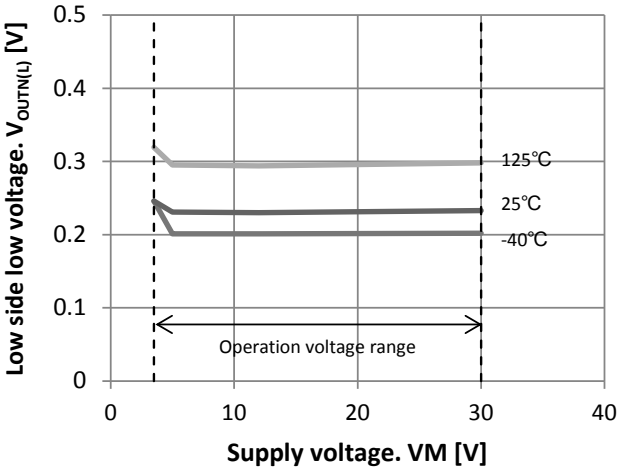


Fig.12 Low voltage of low side output (I_{OUTN}=5mA)

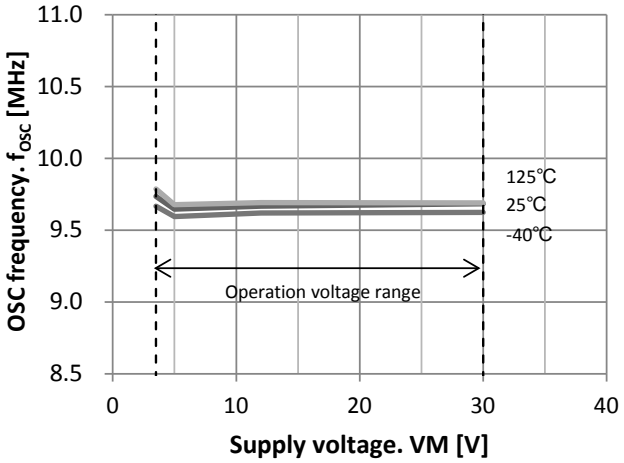


Fig.13 Internal oscillation frequency

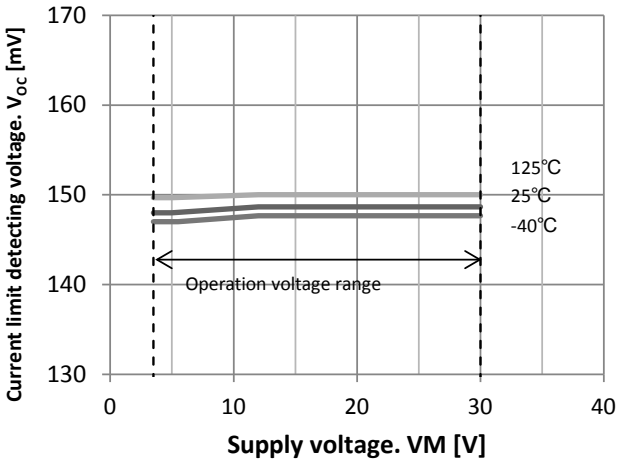
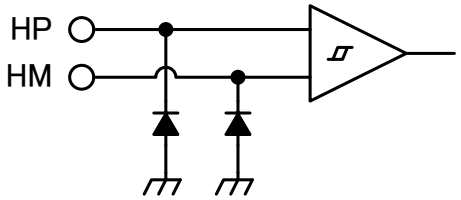
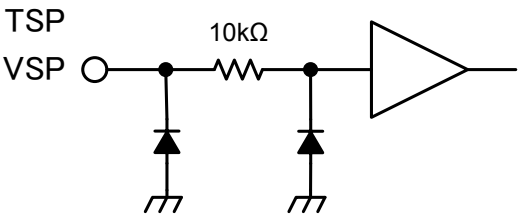
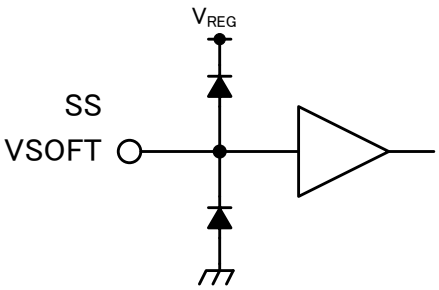
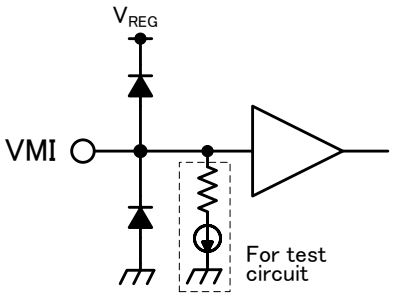
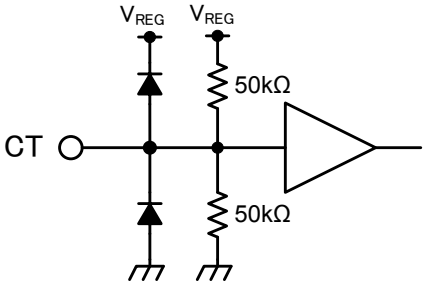
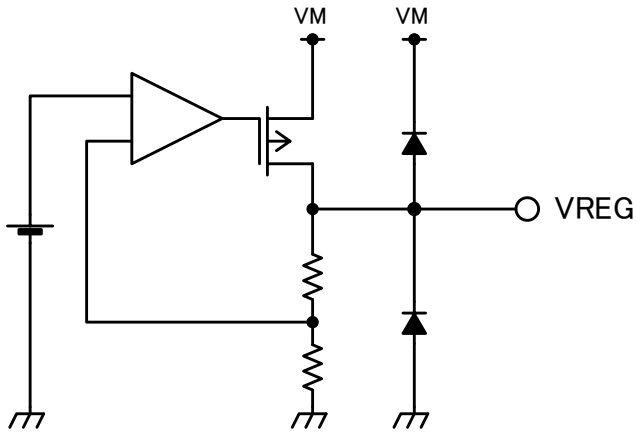
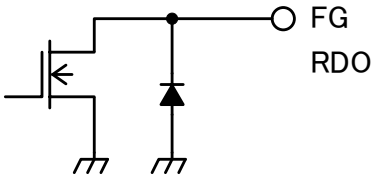
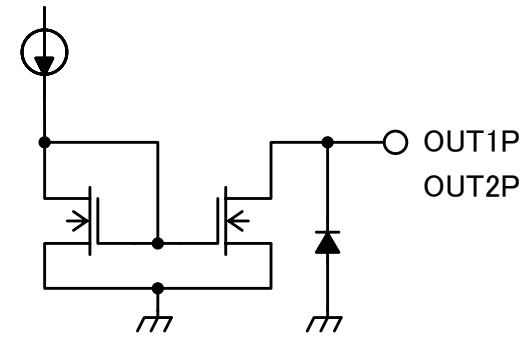
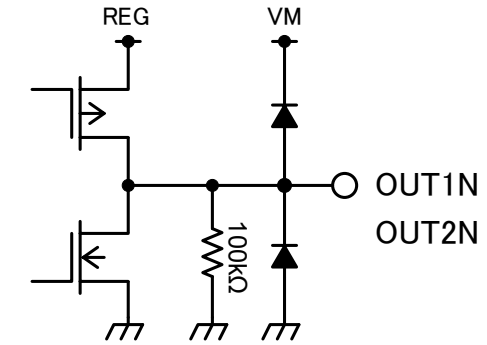
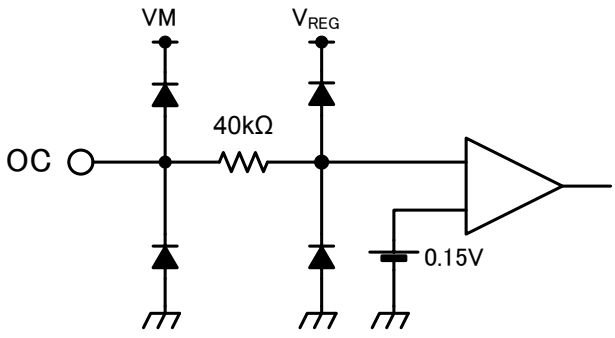


Fig.14 Current limit detection voltage of OC pin

I/O Equivalent Circuits

Pin name	I/O signal	Equivalent circuit
HP HM	Hall signal input pin Common phase input voltage range 0V to V_{REG}-1.5V	
TSP VSP	Control voltage input pin	
SS VSOFT	Control voltage input pin	
VMI	Control voltage input pin	
CT	Control voltage input pin	

Pin name	I/O signal	Equivalent circuit
VREG	Voltage output pin V_{REG} = 5V (typ.)	
FG RDO	Digital output pin Open drain output The output pin should pull-up externally to output high level	
OUTxP	High side output pin	
OUTxN	Low side output pin	
OC	Current limit detection pin	

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Timing charts may be simplified for explanatory purposes.

1. Basic operation

At startup, the motor is driven by a square-wave drive by determining the conducting phase with hall input signal.

When hall signal frequency reaches 10Hz (typ.) or more, the motor is driven by the conducting pattern which is generated by estimating the next conducting timing from the hall input signal.

When hall signal frequency (f_{Hall}) falls 5Hz (typ.) or less, the motor operation returns to the square-wave drive.

<I/O function table>

HP	HM	OUT1P	OUT1N	OUT2P	OUT2N	FG	RDO	Mode
H	L	OFF	H	PWM	L	OFF	L	Rotating (Note 1)
L	H	PWM	L	OFF	H	L	L	
H	L	OFF	H	OFF	L	OFF	—	Current limit drive (Note 2)
L	H	OFF	L	OFF	H	L	—	
—	—	OFF	L	OFF	L	—	OFF	Lock protection (Note 3)
—	—	OFF	L	OFF	L	—	—	Thermal shutdown
—	—	OFF	L	OFF	L	OFF	OFF	Standby mode

Note 1: FG signal is outputted according to the phase-switching. Output modulation waveform generates data of 360° at the next rising timing of hall signal ((FG=L→OFF)). And it switches the phase of output based on the result of the internal calculation.

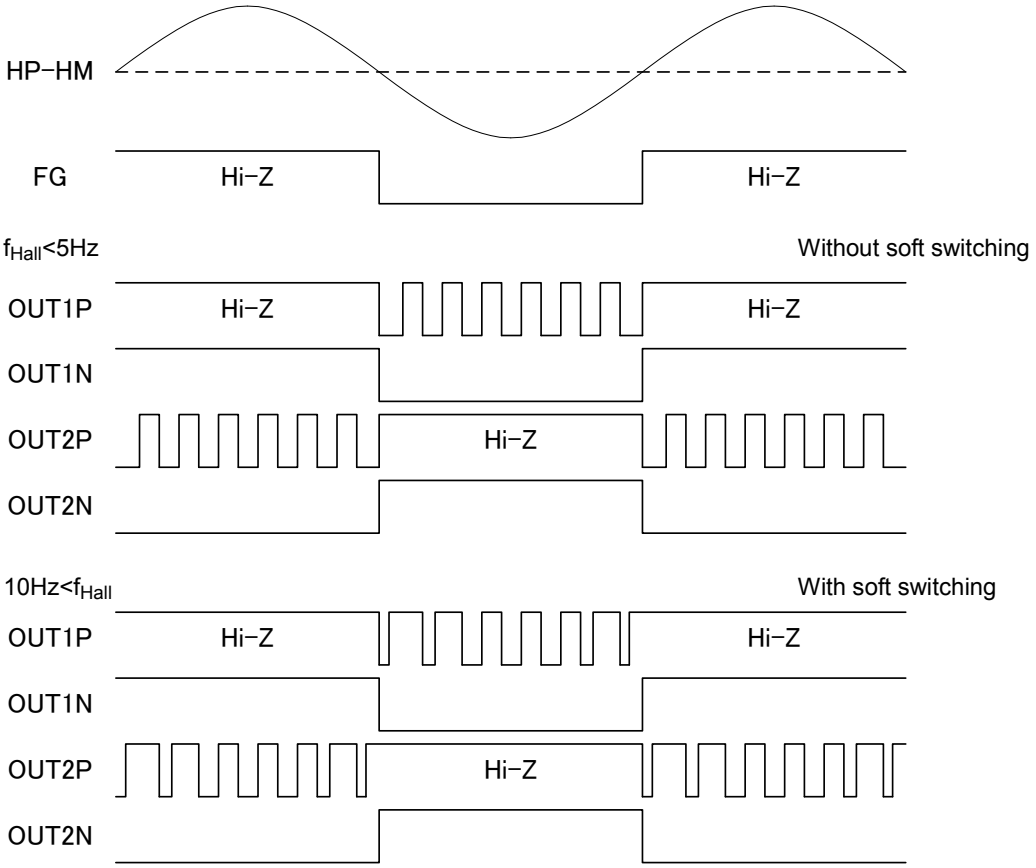
Note 2: High side FET is turned off during current limitation. It recovers automatically every PWM frequency.

Note 3: High side FET is turned off after lock protection. Low side FET is turned off after a certain period of time. FG output changes depending on the rotor position in the lock protection mode the same as rotating mode.

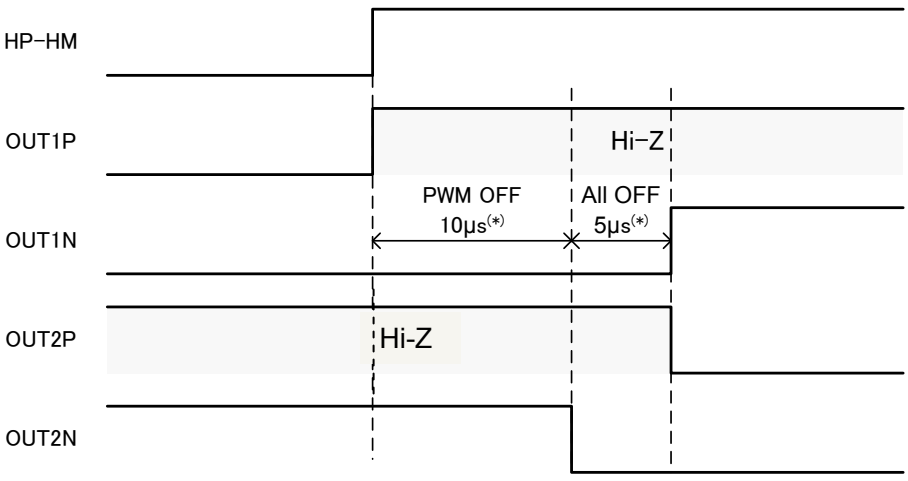
2. PWM drive

In PWM drive, Pch-FET of the external FET is turned on and off repeatedly.

	HP	HM	OUT1P	OUT1N	OUT2P	OUT2N
PWM ON	H	L	OFF	H	L	L
	L	H	L	L	OFF	H
PWM OFF	H	L	OFF	H	OFF	L
	L	H	OFF	L	OFF	H
All OFF	—	—	OFF	L	OFF	L



In switching phase, the output operates in below order. (Hall signal is 10Hz or more in case of full duty.)

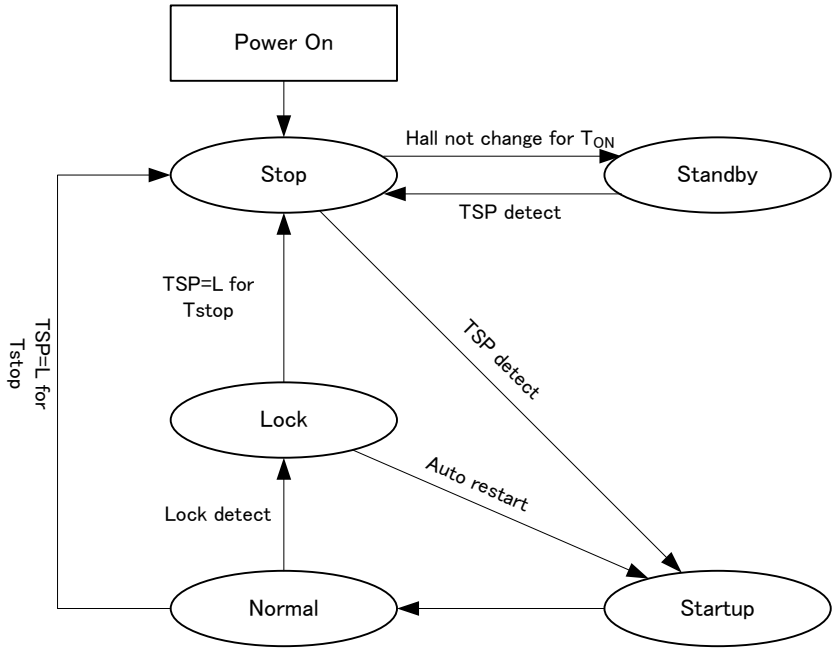


(*) Design target value

3. Transition of IC state and timing chart

State transition

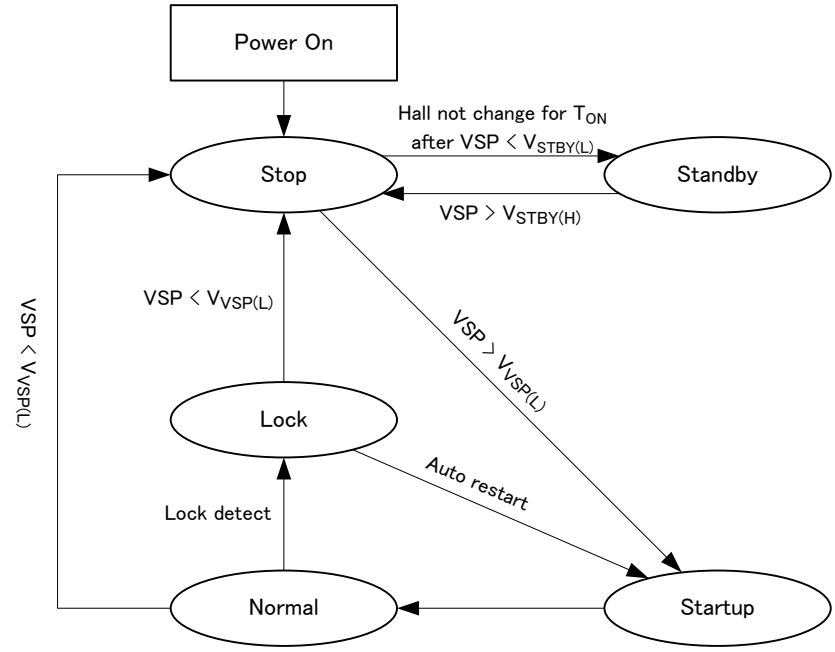
TSP signal input



Note: When minimum output duty is configured by VMI pin,

- the operation moves to the startup sequence from the initial detection regardless of TSP signal.
- the operation does not move to the stop mode even if TSP outputs low level.

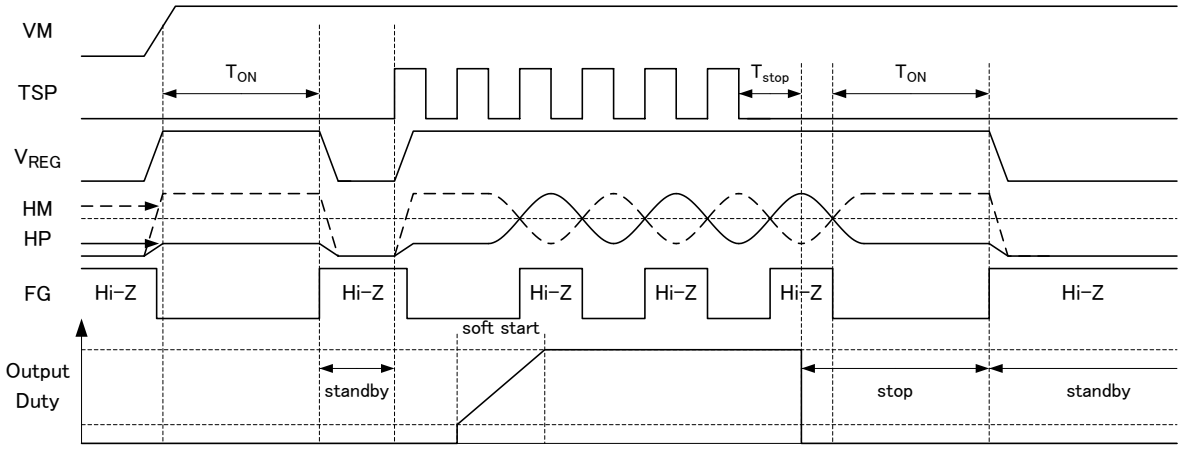
VSP signal input



Note: When minimum output duty is configured by VMI pin,

- the operation moves to the startup sequence from the initial detection regardless of VSP signal.
- the operation does not move to the stop mode even if VSP < $V_{VSP(L)}$.

Detailed description of each state (TSP input)



・Stop mode

After the power supply is applied, the operation moves to the stop mode. If input signal of TSP pin is low for T_{stop} in normal rotating or lock protection, the operation moves to the stop mode. When the operation moves from the normal rotating mode to the stop mode, output keeps PWM OFF until switching of hall signal is detected 3 times or its frequency is detected 5Hz or less. After that, all of external FETs are turned off. In the stop mode, FG signal is outputted by detecting switching of hall signal continually.

When minimum output duty is configured by VMI pin, the operation does not move to the stop mode.

In case startup duty is configured by VMI pin, the operation moves to the stop mode when duty of TSP equals startup duty or less.

When PWM input of TSP pin is detected during the stop mode, the operation moves to the startup sequence.

・Startup sequence

In startup sequence, it starts output when duty of TSP equals the startup duty or more.

Output starts with a 20% duty. The soft start operation changes output duty gradually according to SS pin setting. Finally, the output duty will reach the duty configured by input signal of TSP pin.

In startup, it starts from the square-wave drive. As for the switching of the hall signal, soft switching starts when the frequency of 10Hz or more is detected two cycles or more. In the square-wave drive, in order to reduce the regenerative current to the power supply in phase switching, the PWM OFF term of 1ms is inserted after output phase switching.

・Normal rotating

In normal rotating, output duty is controlled by the duty of PWM input signal of TSP pin.

The output duty changes at the slew rate which is configured by the voltage of SS pin.

In rotating, in case that the hall signal switching frequency is detected more than 10Hz for two cycles or more in, soft switching enables.

In case that the hall signal switching frequency is detected less than 5Hz, soft switching becomes invalid. And PWM OFF term of 1ms is inserted after the output phase switches.

・Lock protection

It monitors the motor rotation by the hall signal and operates when the zero cross of the hall signal cannot be detected for a certain term (T_{ON}) or more. When lock protection operates, the high side external FET is turned off for T_{ON} and then all external FETs are turned off. The motor drive resumes automatically certain term (T_{OFF}) after the lock protection operates.

Lock protection term (T_{ON}) and auto restart term (T_{OFF}) can be configured by CT pin.

FG is outputted by the hall signal even while the lock protection is operating.

In case the zero cross of the hall signal is detected twice in re-startup, the lock protection is cleared and the RDO signal outputs low again.

When TSP input is low level during T_{stop} after lock protection, the operation moves to the stop mode and ready for quick start.

・Standby mode

When switching of hall signal is not detected for T_{ON} in the stop mode, the operation moves the standby mode.

In standby mode, FG pin and RDO pin are OFF (Hi-Z).

When TSP input signal is detected during standby mode, the standby mode is cleared and the operation moves to the startup sequence.

Detailed description of each state (VSP input)

・Stop mode

After the power supply is applied, the operation moves to the stop mode. If the voltage of VSP pin is $V_{VSP\,(L)}$ or less in normal rotating or lock protection, the operation moves to the stop mode. However, the voltage of VSP pin should be kept for T_{VSP} or more because it is detected by AD convertor circuit. When the operation moves from the normal rotating mode to the stop mode, output keeps PWM OFF until switching of hall signal is detected 3 times or its frequency is detected 5Hz or less. After that, all of external FETs are turned off. In the stop mode, FG signal is outputted by detecting switching of hall signal continually.

When minimum output duty is configured by VMI pin, the operation does not move to the stop mode.

In case startup duty is configured by VMI pin, the operation moves to the stop mode when the voltage of VSP pin falls to the threshold of startup voltage or less.

When the voltage of VSP pin is $V_{VSP\,(L)}$ or more is detected during the stop mode, the operation moves to the startup sequence.

・Startup sequence

In startup sequence, it starts output when the voltage of VSP pin is the threshold of startup voltage or more.

Output starts with a 20% duty. The soft start operation changes output duty gradually according to SS pin setting. Finally, the output duty will reach the duty configured by input voltage of VSP pin.

In startup, it starts from the square-wave drive. As for the switching of the hall signal, soft switching starts when the frequency of 10Hz or more is detected two cycles or more. In the square-wave drive, in order to reduce the regenerative current to the power supply in phase switching, the PWM OFF term of 1ms is inserted after output phase switching.

・Normal rotating

In normal rotating, output duty is controlled by the voltage of VSP pin.

The output duty changes at the slew rate which is configured by the voltage of SS pin.

In rotating, in case that the hall signal switching frequency is detected more than 10Hz for two cycles or more in, soft switching enables.

In case that the hall signal switching frequency is detected less than 5Hz, soft switching becomes invalid. And PWM OFF term of 1ms is inserted after the output phase switches.

・Lock protection

It monitors the motor rotation by the hall signal and operates when the zero cross of the hall signal cannot be detected for a certain term (T_{ON}) or more. When lock protection operates, the high side external FET is turned off for T_{ON} and then all external FETs are turned off. The motor drive resumes automatically certain term (T_{OFF}) after the lock protection operates.

Lock protection term (T_{ON}) and auto restart term (T_{OFF}) can be configured by CT pin.

FG is outputted by the hall signal even while the lock protection is operating.

In case the zero cross of the hall signal is detected twice in re-startup, the lock protection is cleared and the RDO signal outputs low again.

When the level of VSP input is $V_{VSP(L)}$ or less after lock protection, the operation moves to the stop mode and can start quickly.

・Standby mode

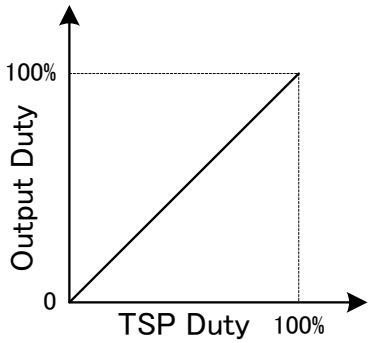
When the voltage of VSP pin is detected $V_{STBY\,(L)}$ or less and switching of hall signal is not detected for T_{ON} in the stop mode, the operation moves the standby mode.

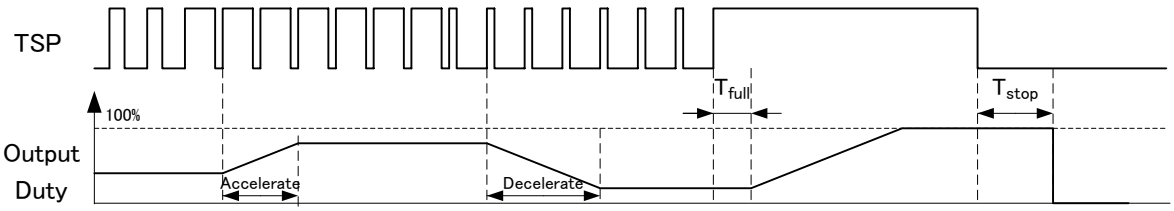
In standby mode, FG pin and RDO pin are OFF (Hi-Z).

When the voltage of VSP exceeds $V_{STBY(H)}$ during standby mode, the standby mode is cleared and the operation moves to the startup sequence.

4. TSP/ VMI input pin

Output duty is configured by duty of PWM signal which is inputted to TSP pin.





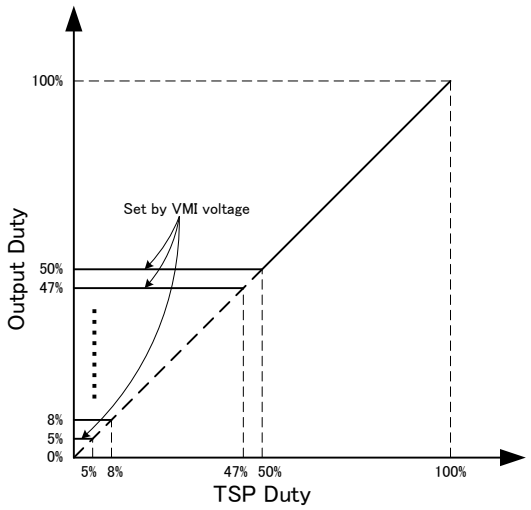
To detect the duty in startup, 3 pulses of PWM signal are necessary. When the duty of input PWM signal changes in the normal rotating state, 1 pulse of PWM signal is required to detect the duty.

To detect the input PWM signal duty of 100%, high level should be kept for T_{full} (1.6ms (typ.)) from the rising edge.

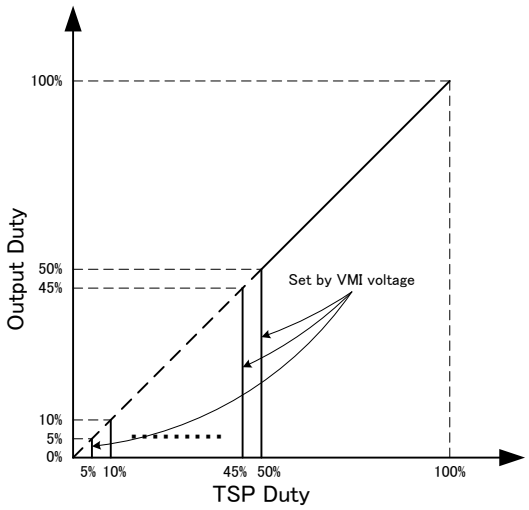
To detect the input PWM signal duty of 0%, low level should be kept for T_{stop} (100ms (typ.)) from the falling edge.

When output duty changes, it changes at the slew rate which is configured by the voltage of SS pin.

Minimum of output duty and startup duty can be configured by the voltage of VMI pin.



In case of setting minimum of output duty



In case of setting threshold of startup duty

The relation of the voltage of VMI pin, minimum of output duty, and threshold of startup duty is as follows;

Step	VMI [V]	Minimal Duty	Startup threshold Duty	Step	VMI [V]	Minimal Duty	Startup threshold Duty	Step	VMI [V]	Minimal Duty	Startup threshold Duty
1	0.00	0%	0%	12	1.46	35%	0%	23	2.92	0%	5%
2	0.13	5%	0%	13	1.59	38%	0%	24	3.05	0%	10%
3	0.27	8%	0%	14	1.73	41%	0%	25	3.19	0%	15%
4	0.40	11%	0%	15	1.86	44%	0%	26	3.32	0%	20%
5	0.53	14%	0%	16	1.99	47%	0%	27	3.45	0%	25%
6	0.66	17%	0%	17	2.13	50%	0%	28	3.59	0%	30%
7	0.80	20%	0%	18	2.26	50%	0%	29	3.72	0%	35%
8	0.93	23%	0%	19	2.39	50%	0%	30	3.85	0%	40%
9	1.06	26%	0%	20	2.52	0%	0%	31	3.98	0%	45%
10	1.20	29%	0%	21	2.66	0%	0%	32	4.12	0%	50%
11	1.33	32%	0%	22	2.79	0%	0%				

(Minimum of output duty indicates the value of output peak because this circuit has a soft switching function.)

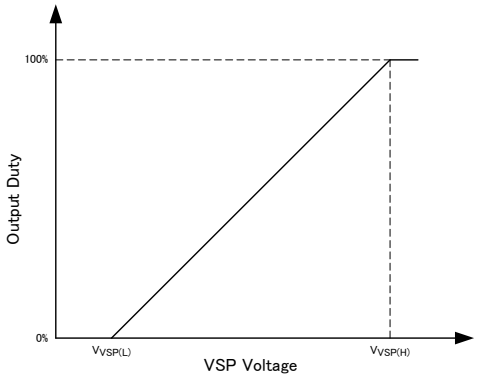
When minimum of output duty is configured by VMI pin, standby mode is disenabled.
When startup duty is configured by VMI pin, the condition of moving to the standby mode is that the hall signal is not switched for T_{ON} since the operation moves to the stop mode.

In using the function of VMI pin, configure the voltage by the resistance voltage divider from V_{REG}.
When the function of VMI pin is not used, connect the pin to the GND.

5. VSP/ VMI pin

Output starts when the voltage of VSP pin exceeds $V_{VSP\ (L)}$. Output turns off when the voltage of VSP pin falls to $V_{VSP\ (L)}$ or less. Output duty is full when the voltage of VSP pin rises to $V_{VSP\ (H)}$ or more.

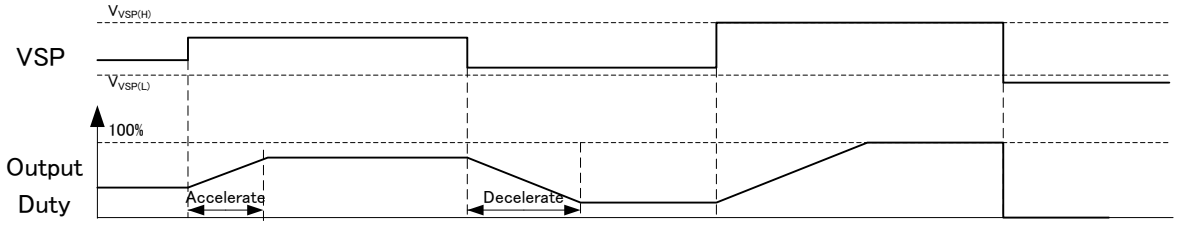
The relation of the voltage of VSP pin and the output PWM duty is as follows.



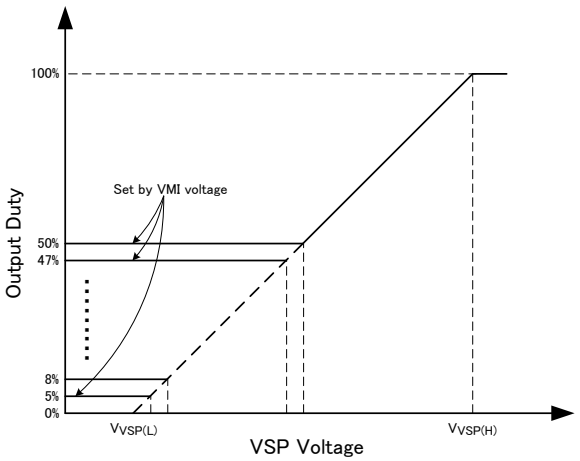
0V	≤ VSP ≤	$V_{VSP(L)}$	→	Duty = 0%
$V_{VSP(L)}$	< VSP ≤	$V_{VSP(H)}$	→	Left figure (90/255 to 217/255)
$V_{VSP(H)}$	< VSP ≤	V_{REG}	→	Duty = 100% (218/255 to 255/255)

$V_{VSP\ (L)}$ = 1.5V (typ.)
$V_{VSP\ (H)}$ = 3.6V (typ.)

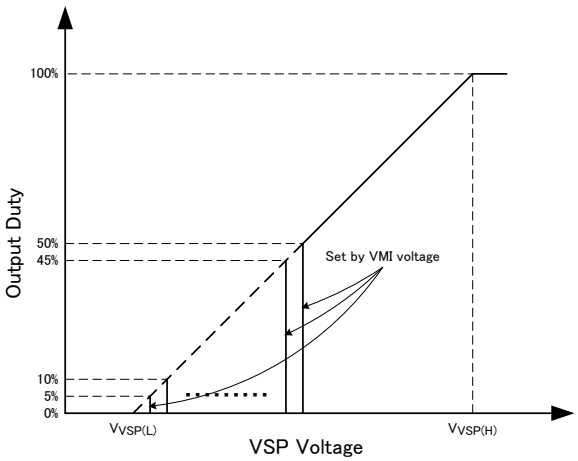
When output duty changes, it changes at the slew rate which is configured by the voltage of SS pin.



Minimum of output duty and the startup duty can be configured by the voltage of VM I pin.



In case of setting minimum of output duty



In case of setting threshold of startup voltage

The relation of the voltage of VMI pin, minimum of output duty, and threshold of startup voltage is as follows.

Step	VMI [V]	Minimal Duty	Startup threshold Voltage [V]	Step	VMI [V]	Minimal Duty	Startup threshold Voltage [V]	Step	VMI [V]	Minimal Duty	Startup threshold Voltage [V]
1	0.00	0%	1.5	12	1.46	35%	0	23	2.92	0%	1.61
2	0.13	5%	0	13	1.59	38%	0	24	3.05	0%	1.71
3	0.27	8%	0	14	1.73	41%	0	25	3.19	0%	1.83
4	0.40	11%	0	15	1.86	44%	0	26	3.32	0%	1.93
5	0.53	14%	0	16	1.99	47%	0	27	3.45	0%	2.03
6	0.66	17%	0	17	2.13	50%	0	28	3.59	0%	2.14
7	0.80	20%	0	18	2.26	50%	0	29	3.72	0%	2.24
8	0.93	23%	0	19	2.39	50%	0	30	3.85	0%	2.36
9	1.06	26%	0	20	2.52	0%	1.5	31	3.98	0%	2.46
10	1.20	29%	0	21	2.66	0%	1.5	32	4.12	0%	2.56
11	1.33	32%	0	22	2.79	0%	1.5				

(Minimum of output duty indicates the value of output peak because this circuit has a soft switching function.)

When minimum of output duty is configured by VMI pin, standby mode is disenabled.

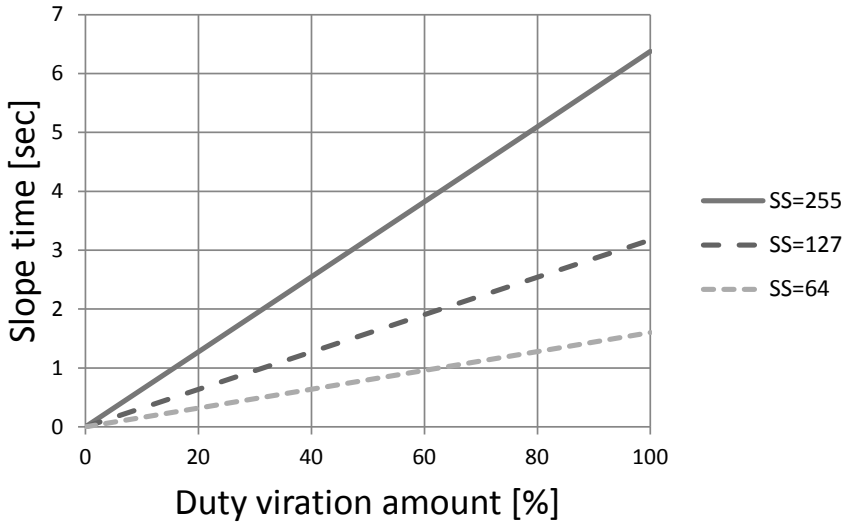
When startup duty is configured by VMI pin, the condition of moving to the standby mode is that the hall signal is not switched for T_{ON} under the condition that the voltage of VSP pin is $V_{STBY\,(L)}$ or less.

In using the function of VMI pin, configure the voltage by the resistance voltage divider from V_{REG}.

When the function of VMI pin is not used, connect the pin to the GND.

6. SS input pin

Analog voltage iputted to the voltge of SS pin is converted by 8-bit AD convertor and the rate of acceleration and deceleration is controlled.



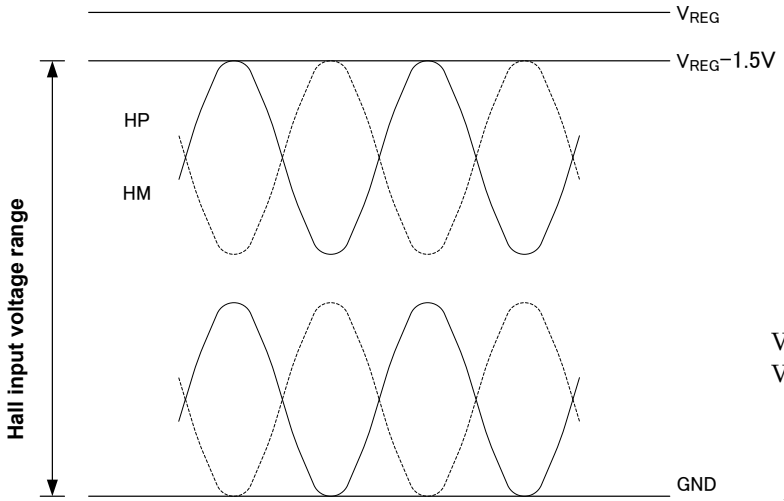
Digital value of SS pin, which is gained after AD conversion, changes 0.4% of the output duty every $4\times N_{SS}$ pulses of the output PWM in N_{SS}.

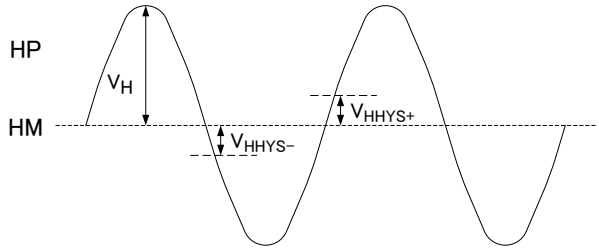
For example, when the output duty changes from 20% to 100% (Amount of duty change: 80%)

- When digital value is 100 after conversion, acceleration and deceleration term is 2s.
- When digital value is 255 after conversion, acceleration and deceleration term is 5.1s.

7. Hall input signal

Below characteristics can be inputted to the hall input pin.



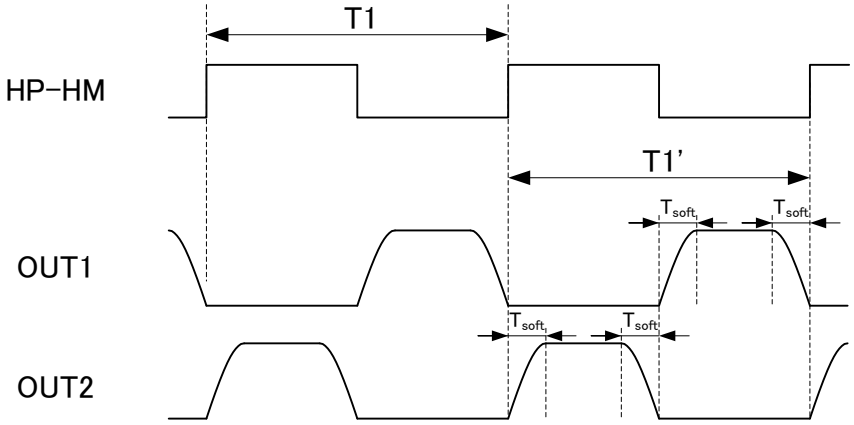


V_H=40mV or more
V_{HHYS+}=10mV, V_{HHYS-}=-10mV

*Hall amplifier operates when the input voltage is 40mVor more. To stabilize the time range, take the amplitude range wide.(Setting 200mV or more is recommended.)

8. Soft switching

Soft switching is performed by changing the output PWM duty gradually when conducting phase switches.



Term of soft switching (T_{soft}) is determined by the time of prior hall signal (360°) and the voltage of VSOFT pin.

In soft switching after conducting phase switch, the output PWM duty changes gradually from 0% to 100% of the output PWM duty determined by TSP/VSP signal by 32 steps in maximum. In soft switching before conducting phase switch, the output PWM duty changes gradually from 100% to 0% of the output PWM duty determined by TSP/VSP signal by 32 steps in maximum.

In case that soft switching term is 22.5°or less, the number of steps of duty change becomes less than 32.

<Relation of the voltage of VSOFT pin and the operation term of soft switching>

VSOFT = 0V → 0°

VSOFT = V_{ADC} → 90° (In case the voltage of V_{ADC} or more is inputted, it is recognized as 90°)

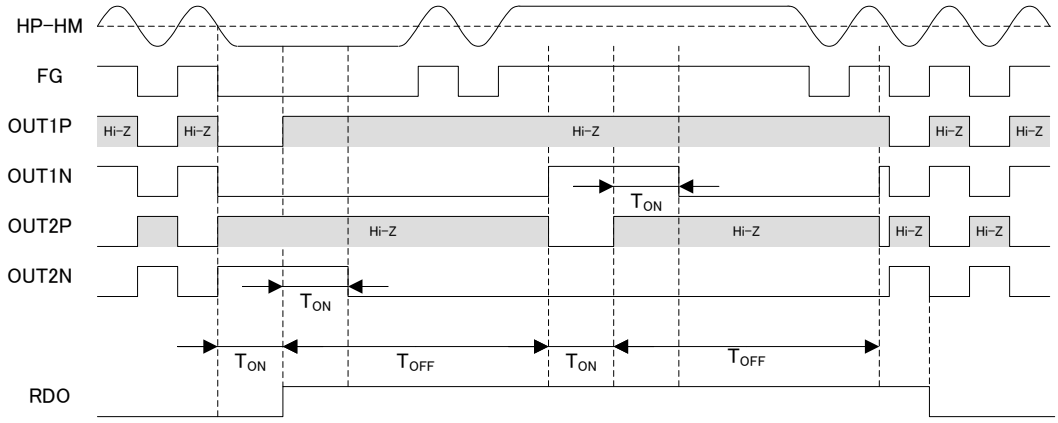
Step	VSOFT (V)	term (°)	Step	VSOFT (V)	term (°)	Step	VSOFT (V)	term (°)
1	0.00	0.0	12	1.46	31.9	23	2.92	63.9
2	0.13	2.9	13	1.59	34.8	24	3.05	66.8
3	0.27	5.8	14	1.73	37.7	25	3.19	69.7
4	0.40	8.7	15	1.86	40.6	26	3.32	72.6
5	0.53	11.6	16	1.99	43.5	27	3.45	75.5
6	0.66	14.5	17	2.13	46.5	28	3.59	78.4
7	0.80	17.4	18	2.26	49.4	29	3.72	81.3
8	0.93	20.3	19	2.39	52.3	30	3.85	84.2
9	1.06	23.2	20	2.52	55.2	31	3.98	87.1
10	1.20	26.1	21	2.66	58.1	32	4.12	90.0
11	1.33	29.0	22	2.79	61.0			

When next rising edge does not occur though term of T1' passes, last output state continues. When the frequency of 5Hz or less is detected, the operation moves to the square-wave drive mode.

Conducting pattern is reset in synchronization with the rising edge of the hall signal. So, waveform indicates non-contiguous every reset in acceleration and deceleration mode.

9. Lock protection

Lock protection monitors motor rotation by the hall signal and operates when the zero cross of the hall signal cannot be detected for a certain term (T_{ON}) or more. When lock protection operates, the high side FET is turned off in the term of T_{ON} and then all FET are turned off. The motor drive resumes certain term (T_{OFF}) after the lock protection operates.



FG is outputted by the hall signal even while the lock protection is operating.

In case the zero cross of the hall signal is detected twice in re-startup, the lock protection is cleared and the RDO signal outputs low again.

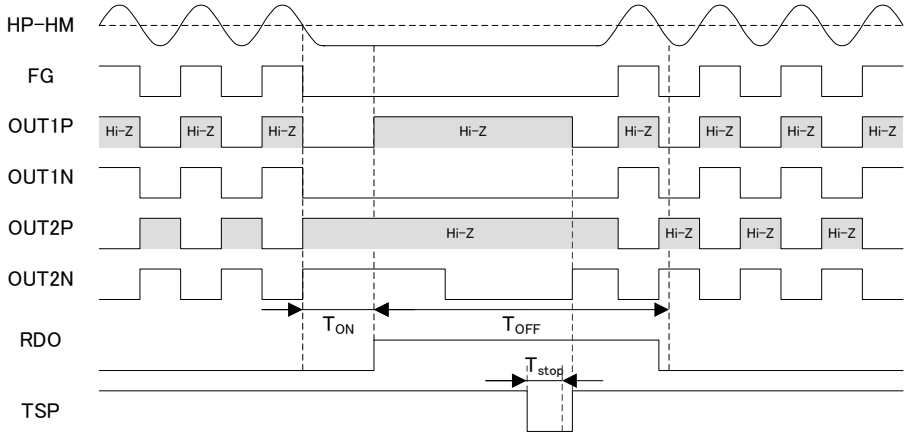
Lock protection term (T_{ON}) and auto restart term (T_{OFF}) are determined by the setting of CT pin. Standby mode can be invalid depending on the setting of CT pin.

Setting of CT pin		T_{ON} term [s]	T_{OFF} term [s]	Standby mode
Voltage range	Recommended setting			
3.73V to V_{REG}	Short to VREG	0.3	3.0	Invalid
3.20V to 3.72V	Pull-up to VREG with a resistor of 39kΩ	0.6	6.0	Invalid
2.67V to 3.18V	Pull-up to VREG with a resistor of 120kΩ	0.6	6.0	Valid
2.13V to 2.65V	Open	0.3	3.0	Valid
1.60V to 2.12V	Pull-down with a resistor of 75kΩ	0.3	6.0	Valid
0.55V to 1.58V	Pull-down with a resistor of 18kΩ	0.3	4.5	Valid
0V to 0.52V	Short to GND	Lock protection is invalid		Invalid

Note: Use the external resistor whose accuracy is 5%.

10. Quick start (TSP)

During T_{OFF} of lock protection, lock protection is cleared when the voltage of TSP pin is set to low level for T_{stop} (100ms (typ.)). When the duty signal is applied to the TSP pin again, the motor restarts operating quickly without waiting for OFF term (the end of T_{OFF}).

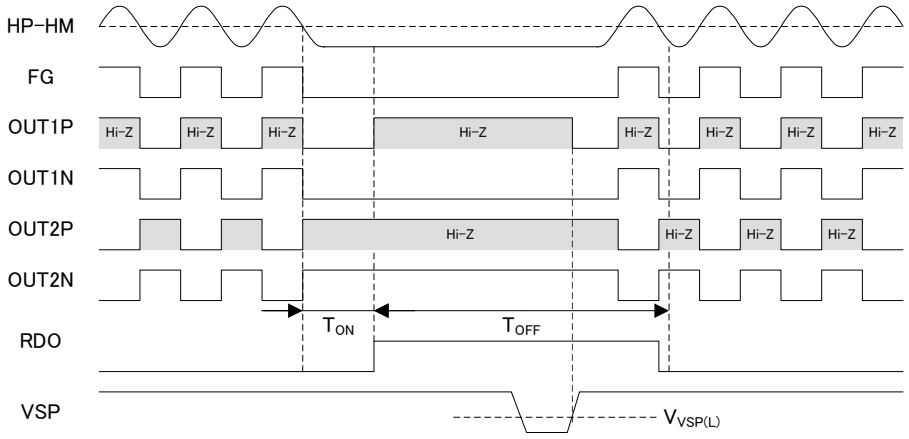


Quick start is disabled when minimum of output duty is set by VMI pin.

When the threshold of the startup duty is set by VMI pin, quick start is enabled after the threshold of the startup duty or less is kept for T_{stop} (100ms (typ.)).

11. Quick start (VSP)

During T_{OFF} of lock protection, lock protection is cleared when the voltage of VSP pin is set to $V_{VSP\,(L)}$ or less for T_{VSP} (10ms (typ.)). When the voltage of $V_{VSP\,(L)}$ or more is applied to the VSP pin again, the motor restarts operating quickly without waiting for the end of the T_{OFF} term.



Quick start is disabled when minimum of output duty is set by VMI pin.

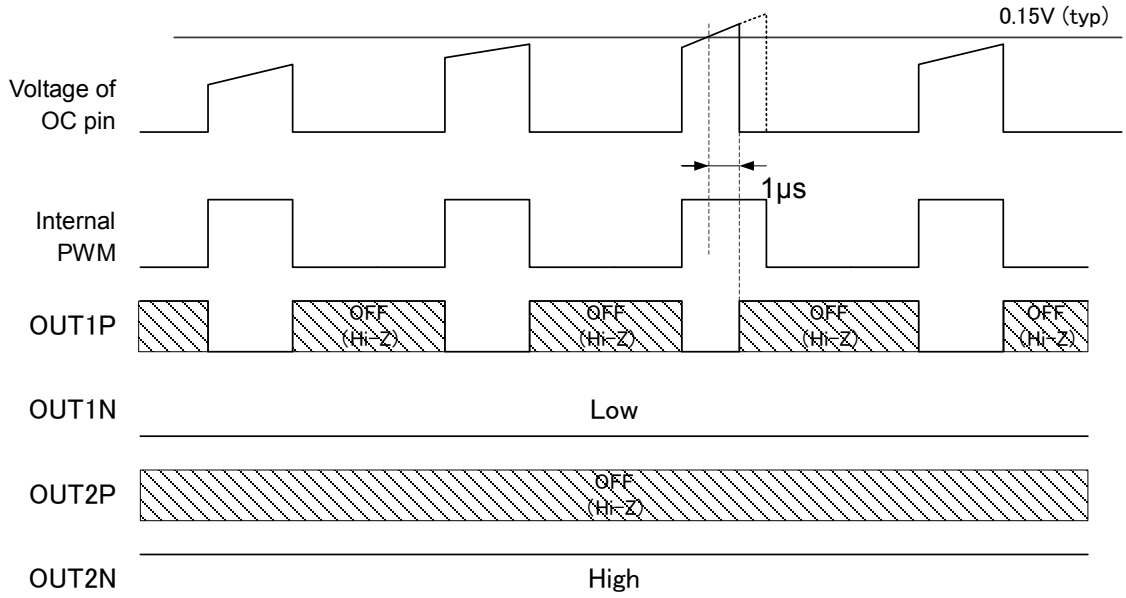
When the threshold of the startup voltage is set by VMI pin, quick start is enabled after the threshold of the startup voltage or less is kept for T_{VSP} (10ms (typ.)).

12. Current limit

This function operates when the current is detected by the shunt resistor (R_S) and the output voltage reaches the current limit detection voltage (V_{OC} = 0.15 V (typ.)).

During the current limit operation, the operation mode is moved to PWM OFF state by turning off the high side FET. The operation resumes at the next PWM ON timing.

Digital filter of 1μs is configured to avoid malfunction by noise.



(HP = L, HM = H)

13. Thermal shutdown circuit (TSD)

This IC has a thermal shutdown circuit (TSD).

It operates when T_j rises 165°C (typ.) or more. PWM is turned off until switching of hall signal is detected 3 times or its frequency is detected 5Hz or less. After that, all of external FETs are turned off. It has a hysteresis of 40°C(typ.). The operation resumes automatically when the temperature falls to 125°C(typ.) or less.

14. Under voltage lockout protection (UVLO)

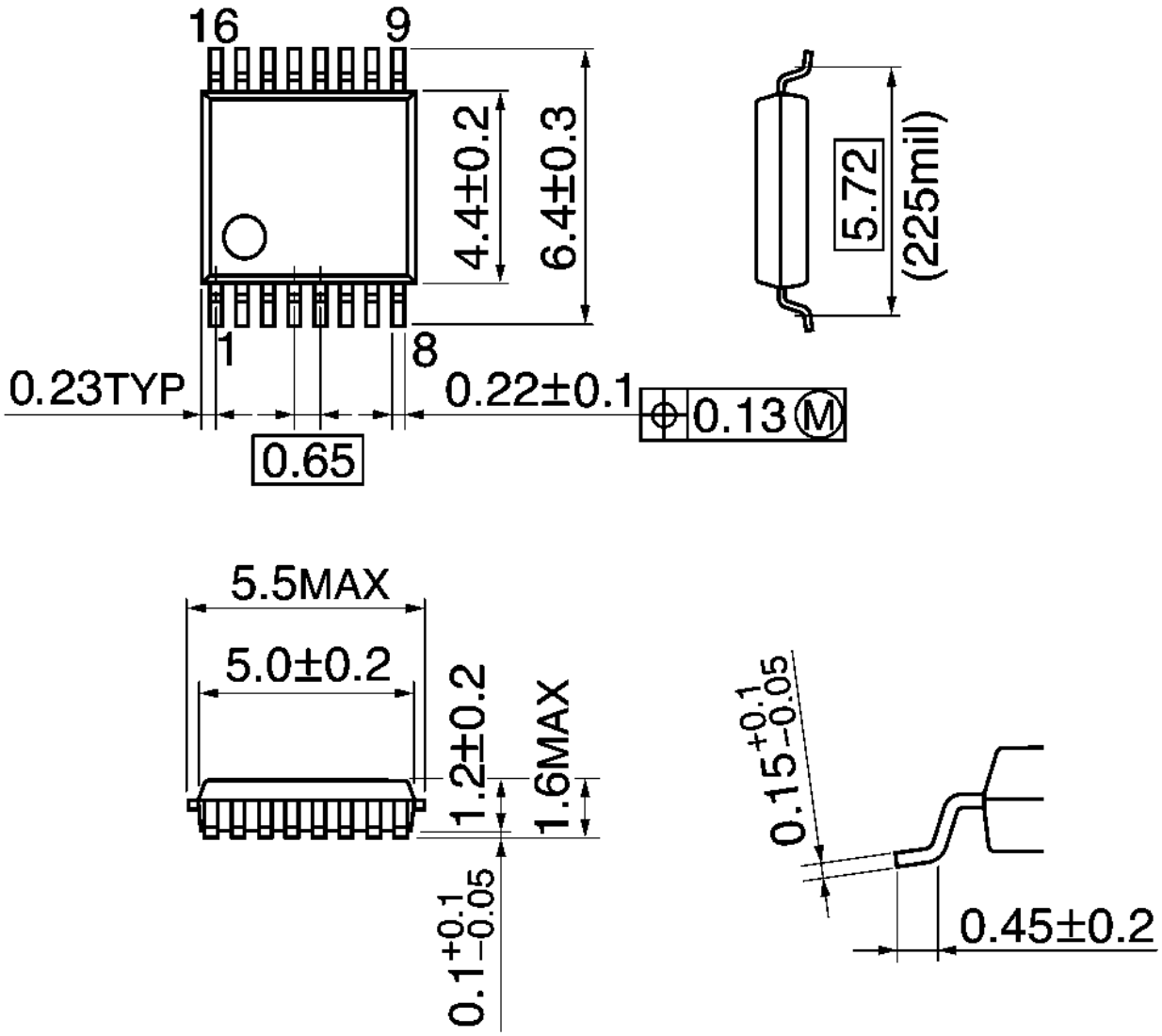
This IC has an under voltage lockout protection (UVLO).

The power supply voltage of VM is always monitored. When it falls to 2.9 V (typ.) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when the voltage recovers to 3.2V (typ.) or more.

In normal operation, the voltage of VREG is also monitored. When it falls to 2.75V (typ.) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when the voltage recovers to 2.95V (typ.) or more.

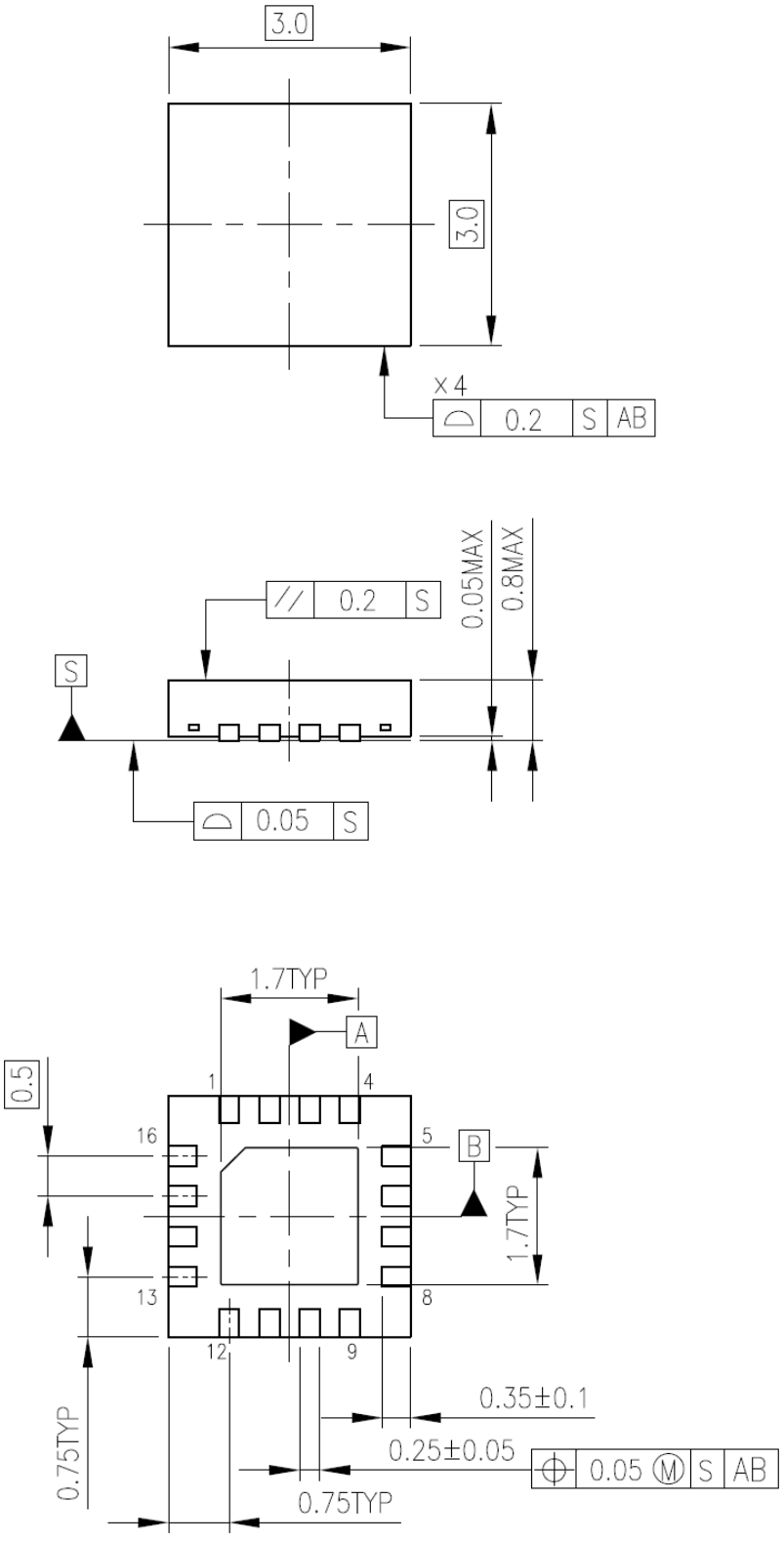
Package Dimensions

SSOP16-P-225-0.65B Unit: mm



Weight: 0.07g (typ.)

P-WQFN16-0303-0.50-003 Unit: mm



Weight: 0.02g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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