CMOS Digital Integrated Circuits Silicon Monolithic

TC7MBL3253CFK

1. Functional Description

- Dual 1-of-4 FET Multiplexer/Demultiplexer

2. General

The TC7MBL3253CFK is a low-voltage/low-capacitance CMOS dual 1-of-4 Multiplexer/Demultiplexer. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

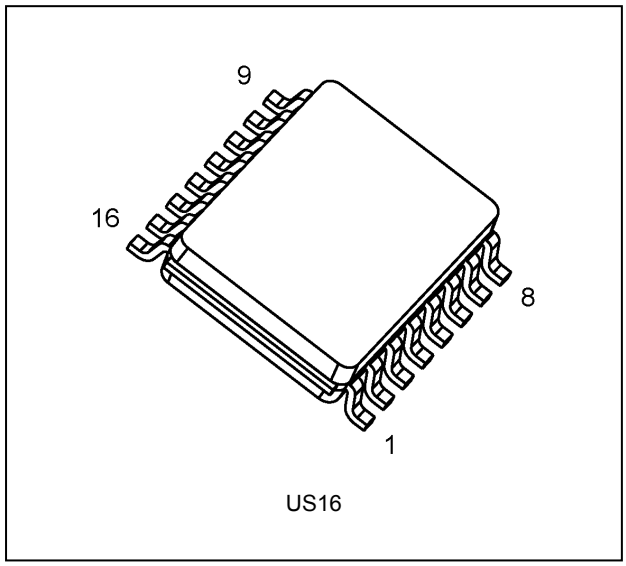
This device consists of two individual four-inputs multiplexer/demultiplexer with common select input (S1, S0) and output enable ($\overline{OE}$). The A input is connected to the B1 to B4 outputs as determined by the combination of both the select input (S1, S0) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held at "H" level, the switches are open regardless of the state of the select inputs, and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

3. Features

(1) Operating voltage: V_{CC} = 1.65 to 3.6 V
(2) ON capacitance: $C_{I/O}$ = 13 pF Switch On (typ.) @V_{CC} = 3.0 V
(3) ON resistance: R_{ON} = 9 Ω (typ.) @V_{CC} = 3.0 V, V_{IS} = 0 V
(4) Power-down protection for inputs ($\overline{OE}$, S1, S0 and I/O)
(5) Package: VSSOP16 (US16)

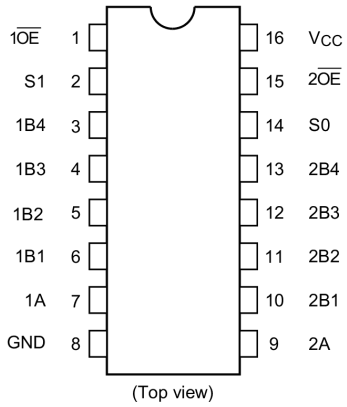
4. Packaging



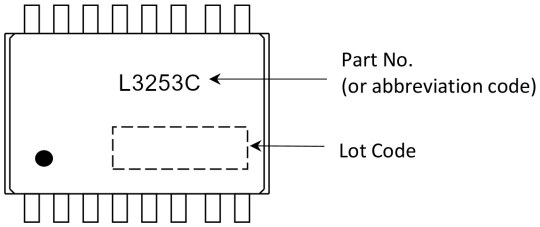
US16

Start of commercial production
2008-06

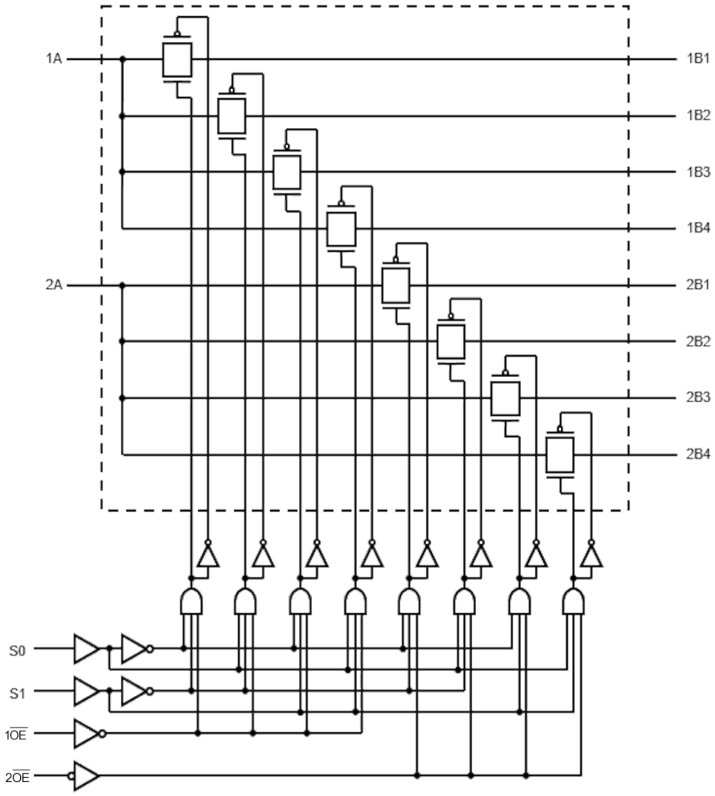
5. Pin Assignment



6. Marking



7. System Diagram



8. Truth Table

Inputs $\overline{OE}$	Inputs S1	Inputs S0	Function
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

X: Don't care

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}			-0.5 to 4.6	V
Input voltage ($\overline{OE}$, S1, S0)	V_{IN}			-0.5 to 4.6	V
Switch I/O voltage	V_S		V_{CC} = 0 V or Switch = Off	-0.5 to 4.6	V
			Switch = On	-0.5 to V_{CC} +0.5	
Clamp diode current	I_{IK}			-50	mA
Switch I/O current	I_S			50	mA
Power dissipation	P_D			180	mW
V_{CC}/ground current	I_{CC}/I_{GND}			±100	mA
Storage temperature	T_{stg}			-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}			1.65 to 3.6	V
Input voltage ($\overline{OE}$, S1, S0)	V_{IN}			0 to 3.6	V
Switch I/O voltage	V_S		V_{CC} = 0 V or Switch = Off	0 to 3.6	V
			Switch = On	0 to V_{CC}	
Operating temperature	T_{opr}			-40 to 85	°C
Input rise time	dt/dv			0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage ($\overline{OE}$, S1, S0)	V_{IH}		—	1.65 to 3.6	0.7 × V_{CC}	—	—	V
Low-level input voltage ($\overline{OE}$, S1, S0)	V_{IL}		—	1.65 to 3.6	—	—	0.3 × V_{CC}	V
Input leakage current ($\overline{OE}$, S1, S0)	I_{IN}		V_{IN} = 0 to 3.6 V	1.65 to 3.6	—	—	±1.0	μA
Power-OFF leakage current	I_{OFF}		$\overline{OE}$, S, A, B = 0 to 3.6 V	0	—	—	10	μA
Switch OFF-state leakage current	I_{SZ}		A, B = 0 V to V_{CC}, $\overline{OE}$ = V_{CC}	1.65 to 3.6	—	—	±1.0	μA
ON-resistance	R_{ON}	(Note 1), (Note 2)	V_{IS} = 0 V, I_{IS} = 30 mA	3.0	—	9	13	Ω
			V_{IS} = 3.0 V, I_{IS} = 30 mA	3.0	—	18	24	
			V_{IS} = 2.4 V, I_{IS} = 15 mA	3.0	—	20	28	
			V_{IS} = 0 V, I_{IS} = 24 mA	2.3	—	10	15	
			V_{IS} = 2.3 V, I_{IS} = 24 mA	2.3	—	23	32	
			V_{IS} = 2.0 V, I_{IS} = 15 mA	2.3	—	25	35	
			V_{IS} = 0 V, I_{IS} = 4 mA	1.65	—	12	18	
			V_{IS} = 1.65 V, I_{IS} = 4 mA	1.65	—	29	40	
Quiescent supply current	I_{CC}		V_{IN} = V_{CC} or GND, I_{OUT} = 0 A	3.6	—	—	10	μA

Note 1: All typical values are at T_a = 25 °C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A or B) pins.

11.2. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output enable time ($\overline{OE}$ to bus)	t_{PZL},t_{PZH}	See Fig. 11.4., 11.5.1, Table 11.4.1	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output enable time (S1, S0 to bus)	t_{PZL},t_{PZH}	See Fig. 11.4., 11.5.1, Table 11.4.1	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output disable time ($\overline{OE}$ to bus)	t_{PLZ},t_{PHZ}	See Fig. 11.4., 11.5.1, Table 11.4.1	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output disable time (S1, S0 to bus)	t_{PLZ},t_{PHZ}	See Fig. 11.4., 11.5.1, Table 11.4.1	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	

11.3. Capacitive Characteristics (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance ($\overline{OE}$, S1, S0)	C_{IN}	V_{IN} = 0 V	3.0	5	pF
Switch terminal OFF-capacitance (Bn)	$C_{I/O}$	$\overline{OE}$ = V_{CC}, V_{IS} = 0 V	3.0	4	pF
Switch terminal OFF-capacitance (A)	$C_{I/O}$	$\overline{OE}$ = V_{CC}, V_{IS} = 0 V	3.0	9	pF
Switch terminal ON-capacitance (Bn)	$C_{I/O}$	$\overline{OE}$ = GND, V_{IS} = 0 V	3.0	13	pF
Switch terminal ON-capacitance (A)	$C_{I/O}$	$\overline{OE}$ = GND, V_{IS} = 0 V	3.0	13	pF

Note: Parameter guaranteed by design.

11.4. AC Test Circuits

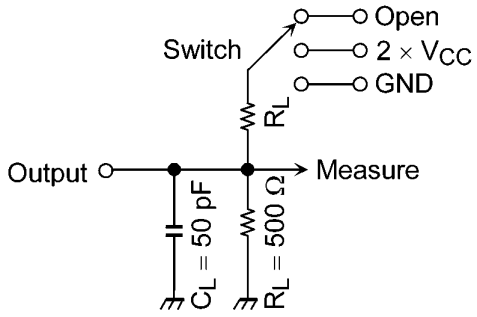


Table 11.4.1 Parameter for AC Test Circuit

Parameter	Switch
t_{PLZ}, t_{PZL}	2 × V_{CC}
t_{PHZ}, t_{PZH}	GND

11.5. AC Waveform

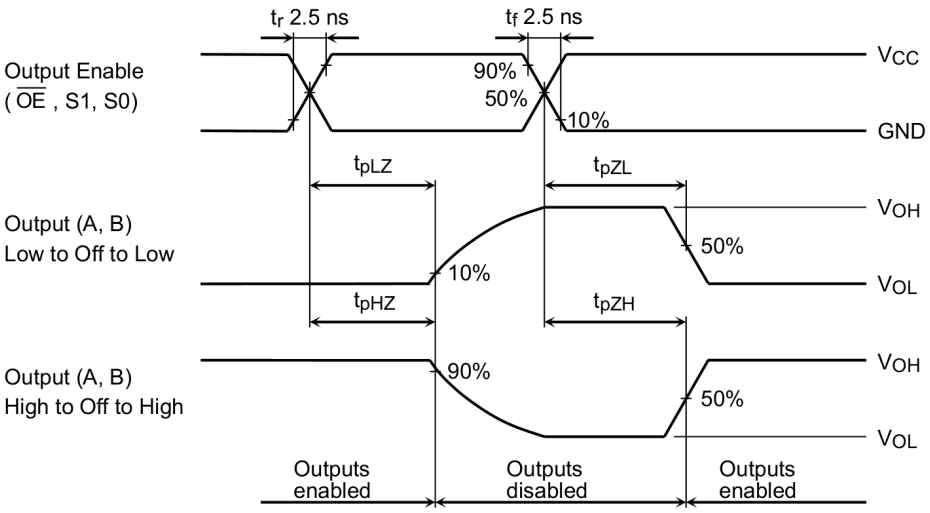


Fig. 11.5.1 AC Waveform t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

12. Rise and Fall Time (t_r/t_f)

The $t_{r(out)}$ and $t_{f(out)}$ values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the $t_{r(out)}$ and $t_{f(out)}$ values are also affected by the circuit's capacitance and resistance components other than those of the TC7MBL3253CFK.

The $t_{r(out)}/t_{f(out)}$ values can be approximated as follows. (Fig. 12.1, Table 12.1 shows the calculation circuit.)

$t_{r(out)}/t_{f(out)}$ (approx) = - $(C_{I/O} + C_L)$ · $(R_{DRIVE} + R_{ON})$ · ln $(((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL}))$

Where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$t_{r(out)}$ (approx) = - (13 + 15) E - 12 · (120 + 9) · ln (((3.0 - 0) - 1.5) / (3.0 - 0)) ≈ 2.5 ns

Calculation conditions:

V_{CC} = 3.0 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 1.5 V (V_{CC}/2)

Output of the previous IC = digital (i.e., high-level voltage = V_{CC}, low-level voltage = GND)

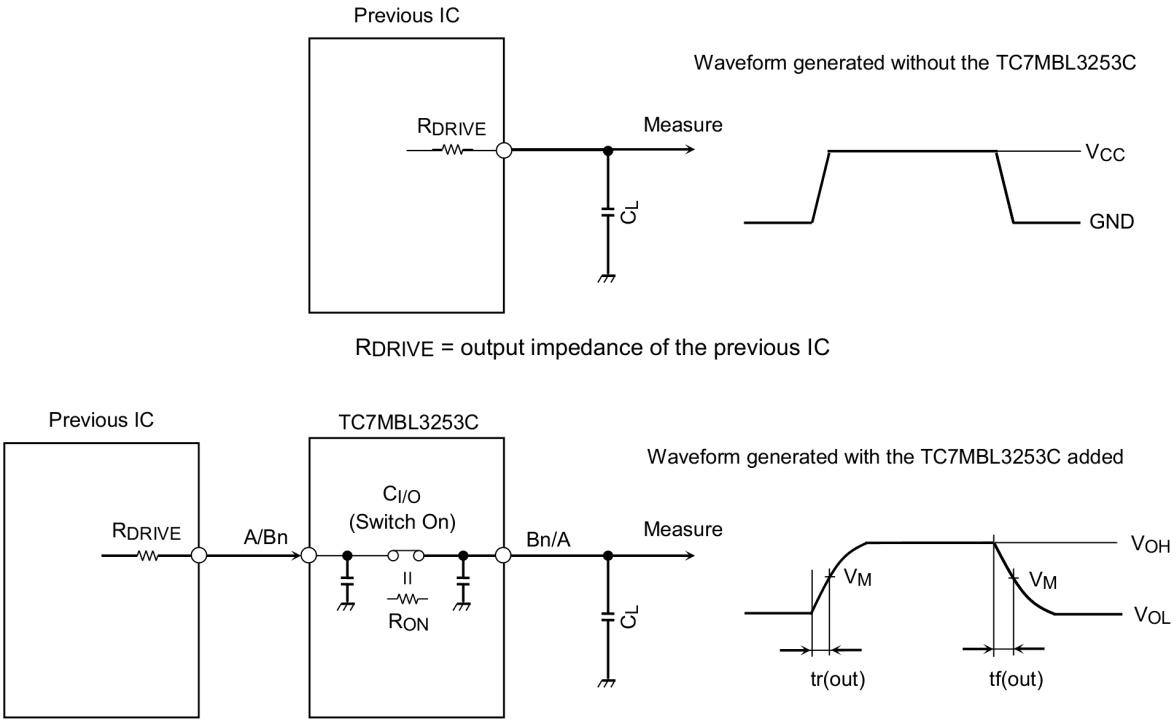


Fig. 12.1 Calculation Circuit

Table 12.1 Calculation Circuit

Characteristics	V_{CC} = 3.3 ± 0.3 V	V_{CC} = 2.5 ± 0.2 V	V_{CC} = 1.8 ± 0.15 V
V_M	V_{CC}/2	V_{CC}/2	V_{CC}/2

13. Characteristics Curves (Note)

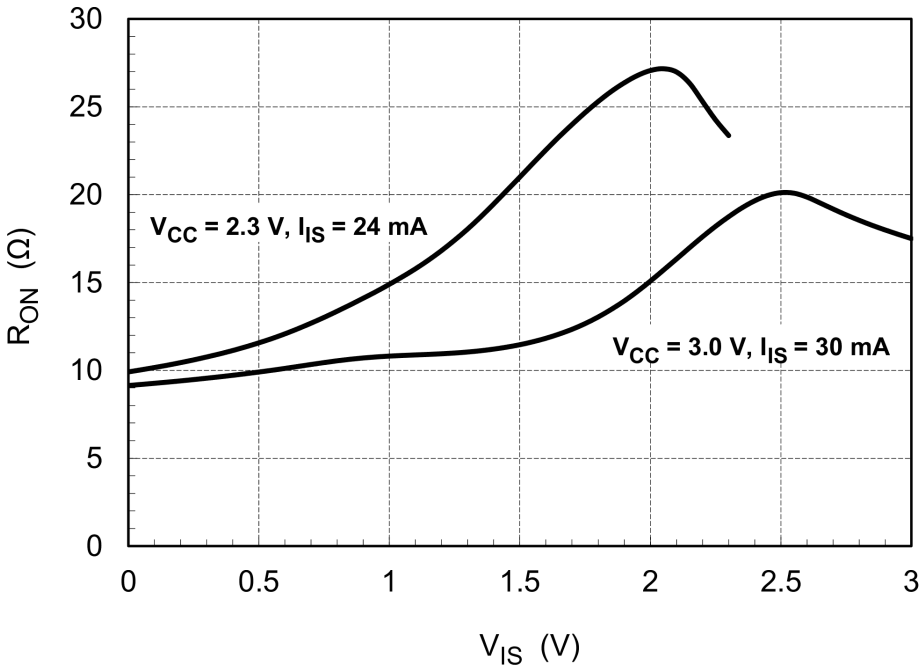
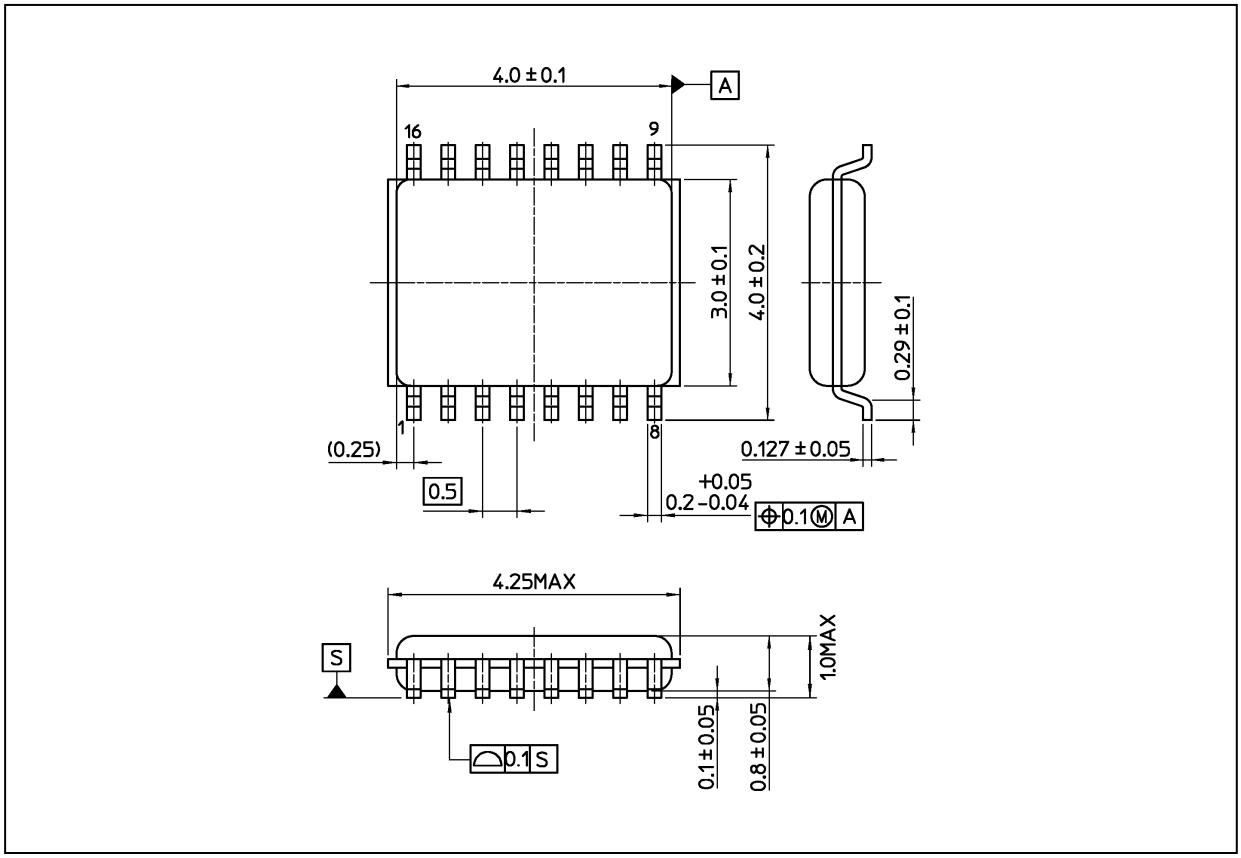


Fig. 13.1 R_{ON} - V_{IS} (tpy.) (T_a = 25 °C)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.02 g (typ.)

Package Name(s)
Nickname: US16

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