CMOS Digital Integrated Circuits Silicon Monolithic

# TC7MPB9326FT,TC7MPB9327FT

## 1. Functional Description

- Low-Voltage, Low-Power Dual SPDT Supply Bus Switch

## 2. General

The TC7MPB9326FT and TC7MPB9327FT are CMOS dual multiplexer/demultiplexer bus switches that can provide an interface between two nodes at different voltage levels. These devices can be connected to two independent power supplies. $V_{CCA}$ supports 1.8 V, 2.5 V and 3.3 V power supplies, whereas $V_{CCB}$ supports 2.5 V, 3.3 V and 5.0 V power supplies.

Bidirectional level-shifting is possible by simply adding external pull-up resistors between the A/Bn data lines and the $V_{CCA}$ / $V_{CCB}$ supplies. There is no restriction on the relative magnitude of the A and Bn voltages; both the 1A/2A and 1B1/1B2 ,2B1/2B2 data lines can be pulled up to the arbitrary power supplies.

The Output Enable pin (OE) can be used to disable the device so that the bus lines are effectively isolated.

This device consists of dual individual two-inputs multiplexer/demultiplexer with a common select input (S) and an output enable (OE:TC7MPB9326FT, $\overline{OE}$:TC7MPB9327FT). The 1A/2A inputs are connected to 1B1/1B2 and 2B1/2B2 outputs based on the combination of select input and output enable.

For TC7MPB9326FT, it has an active high Output Enable (OE) : When OE is High, the switch is on; When Low, the switch is turned off. For the TC7MPB9327FT, it has an active low Output Enable ($\overline{OE}$) : When $\overline{OE}$ is Low, the switch is turned on; When $\overline{OE}$ is High, the switch is off.

The TC7MPB9326FT and TC7MPB9327FT supports power-down protection at the $\overline{OE}$, OE input, with $\overline{OE}$, OE being 5.5 V tolerant.

The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.

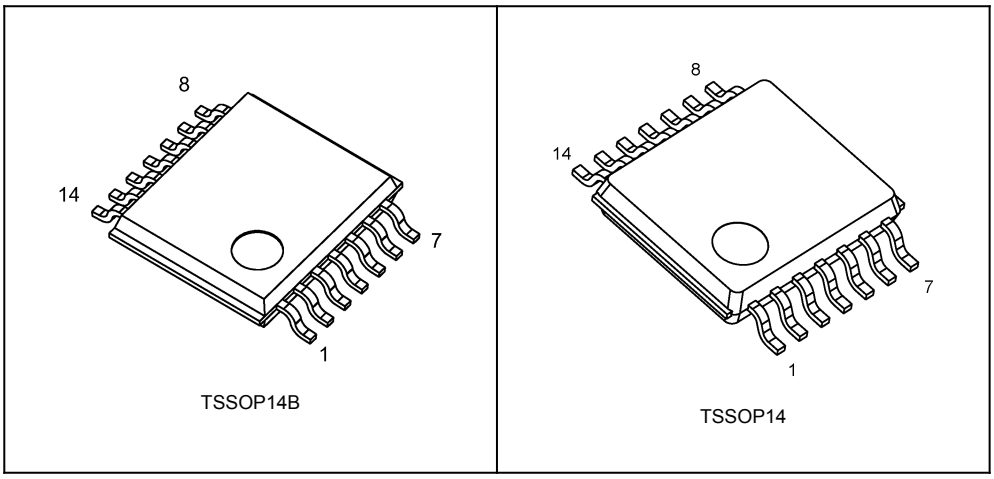
## 3. Features

(1) AEC-Q100 (rev.H) Grade 1 qualified (Note 1)
(2) Wide operating temperature range: $T_{opr}$ = -40 to 125 °C (Note 2)
(3) Operating voltage: 1.8 V to 2.5 V / 1.8 V to 3.3 V / 1.8 V to 5.0 V / 2.5 V to 3.3 V / 2.5 V to 5.0 V / 3.3 V to 5.0 V bidirectional interface
(4) Operating voltage: $V_{CCA}$ = 1.65 to 5.0 V, $V_{CCB}$ = 2.3 to 5.5 V
(5) Low ON-resistance: $R_{ON}$ = 5.0 Ω (typ.) @ $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA, $V_{CCA}$ = 3.0 V, $V_{CCB}$ = 4.5 V
(6) 5.5 V tolerance and power-down protection at the Output Enable input.
(7) Packages: TSSOP14, TSSOP14B

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.
Note 2: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

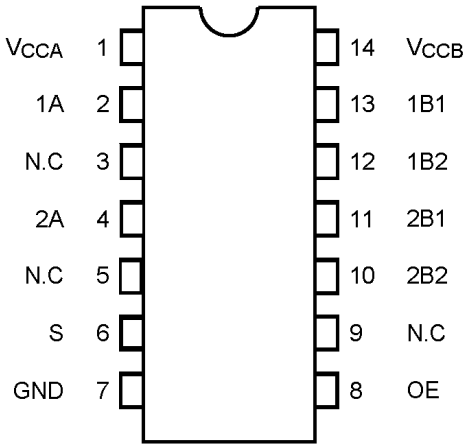
Start of commercial production
2009-09

## 4. Packaging

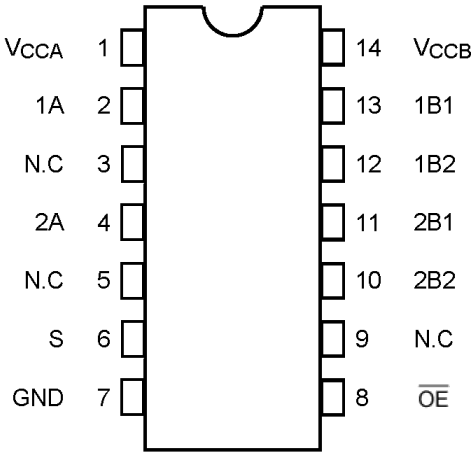



## 5. Pin Assignment

TC7MPB9326FT




TC7MPB9327FT



## 6. Marking

TC7MPB9326FT

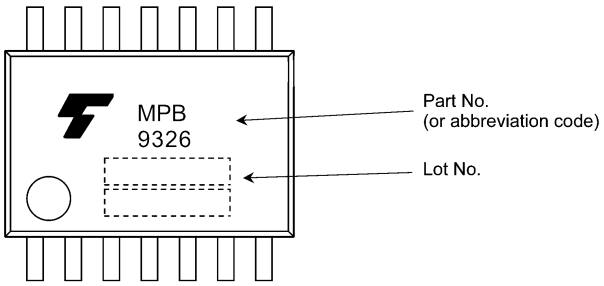



Fig. 6.1 TSSOP14B

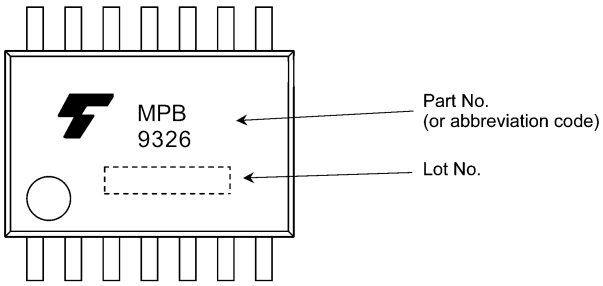



Fig. 6.2 TSSOP14

TC7MPB9327FT

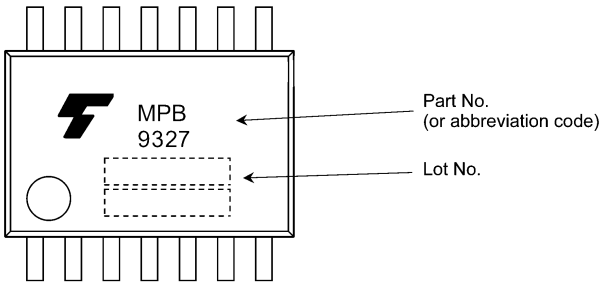



Fig. 6.3 TSSOP14B

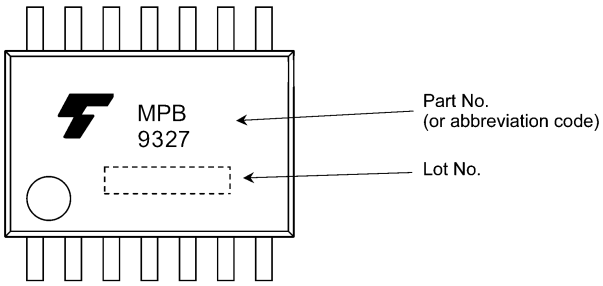
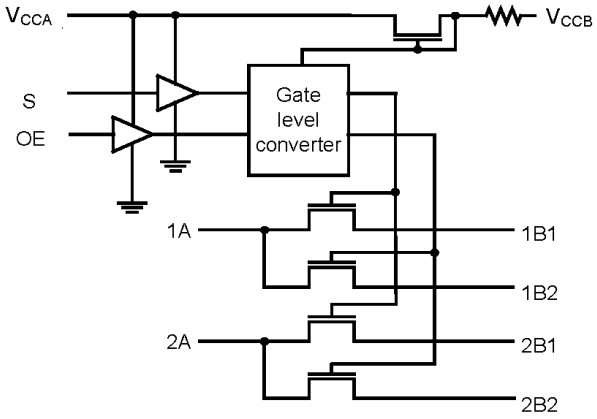


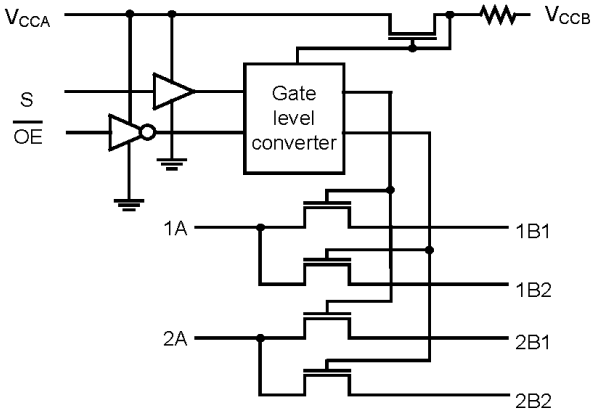

Fig. 6.4 TSSOP14

## 7. Block Diagram

TC7MPB9326FT




TC7MPB9327FT




## 8. Truth Table

| Inputs (9326) OE | Inputs (9327) $\overline{OE}$ | Inputs S | Function |
|---|---|---|---|
| H | L | L | A = B1 |
| H | L | H | A = B2 |
| L | H | X | Disconnect |

## 9. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CCA}$ | | -0.5 to 7.0 | V |
| | $V_{CCB}$ | | -0.5 to 7.0 | |
| Input voltage | $V_{IN}$ | | -0.5 to 7.0 | V |
| Switch I/O voltage | $V_S$ | | -0.5 to 7.0 | V |
| Clamp diode current | $I_{IK}$ | | -50 | mA |
| Switch I/O current | $I_S$ | | 64 | mA |
| $V_{CC}$/ground current per supply pin | $I_{CCA}$ | | ±25 | mA |
| | $I_{CCB}$ | | ±25 | |
| Power dissipation | $P_D$ | (Note 1) | 180 | mW |
| Storage temperature | $T_{stg}$ | | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of $T_a$ = -40 to 85. From $T_a$ = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

## 10. Operating Ranges (Note)

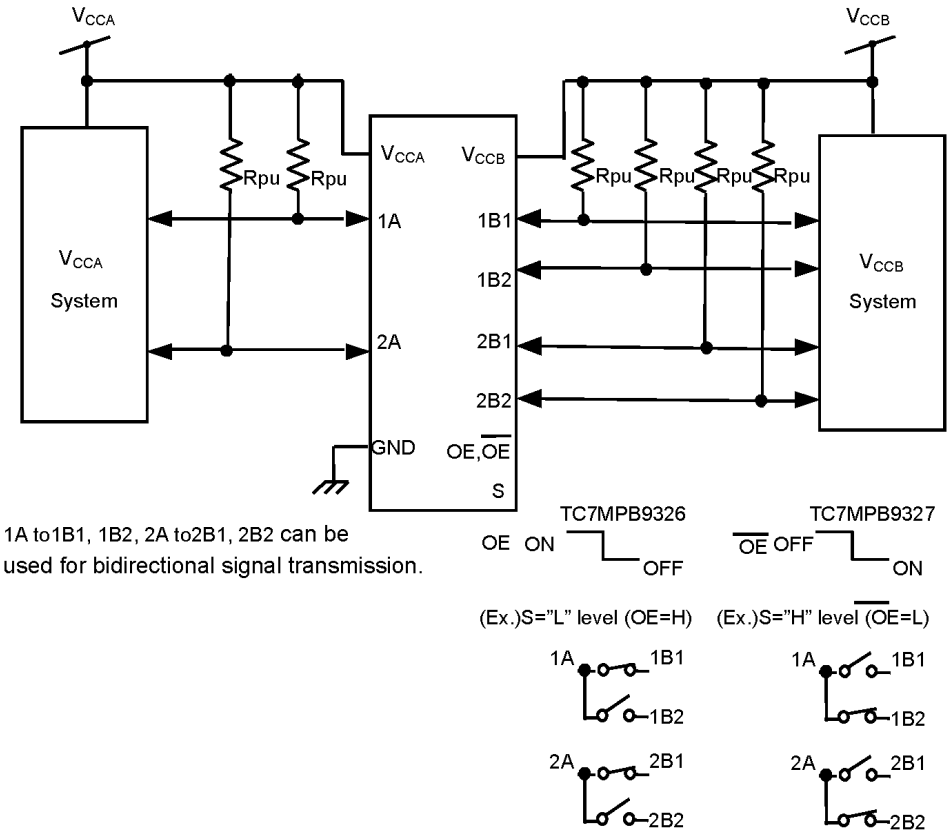
| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CCA}$ | (Note 1) | 1.65 to 5.0 | V |
| | $V_{CCB}$ | | 2.3 to 5.5 | |
| Input voltage | $V_{IN}$ | | 0 to 5.5 | V |
| Switch I/O voltage | $V_S$ | | 0 to 5.5 | V |
| Operating temperature | $T_{opr}$ | (Note 2) | -40 to 125 | °C |
| Input rise time | dt/dv | | 0 to 10 | ns/V |
| Input fall time | dt/dv | | 0 to 10 | |

Note : The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either $V_{CCA}$ or GND.

Note 1: The $V_{CCA}$ voltage must be lower than the $V_{CCB}$ voltage.

Note 2: Operating Ranges of $T_a$ = -40 °C to 125 °C are only applicable for products which manufactured from April 2020 onward.

## 11. Application Circuit (Note)




Note: The $V_{CCA}$ < $V_{CCB}$ voltage must be lower than the $V_{CCB}$ voltage.

Note: Level-shifting functionality is enabled by adding pull-up resistors from An to $V_{CCA}$ or $V_{CCB}$ and from Bn to $V_{CCB}$ or $V_{CCA}$, respectively.

## 12. Electrical Characteristics

### 12.1. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage ($\overline{OE}$/OE, S) | $V_{IH}$ | | — | $1.65 \le V_{CCA} < 2.3$ | $V_{CCA}$ to 5.5 | $0.8 \times V_{CCA}$ | — | V |
| | | | | $2.3 \le V_{CCA} < 5.0$ | $V_{CCA}$ to 5.5 | $0.7 \times V_{CCA}$ | — | |
| Low-level input voltage ($\overline{OE}$/OE, S) | $V_{IL}$ | | — | $1.65 \le V_{CCA} < 2.3$ | $V_{CCA}$ to 5.5 | — | $0.2 \times V_{CCA}$ | V |
| | | | | $2.3 \le V_{CCA} < 5.0$ | $V_{CCA}$ to 5.5 | — | $0.3 \times V_{CCA}$ | |
| ON-resistance | $R_{ON}$ | (Note 1) | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA See Figure 13.1 | 1.65 | 2.3 | — | 16.0 | Ω |
| | | | | 2.3 | 3.0 | — | 11.0 | |
| | | | | 3.0 | 4.5 | — | 8.0 | |
| Power-OFF leakage current | $I_{OFF}$ | | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V (per circuit) | 0 | 0 | — | ±1.0 | μA |
| Switch OFF-state leakage current | $I_{SZ}$ | | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V OE = GND, $\overline{OE}$ = $V_{CCA}$ | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±1.0 | μA |
| Input leakage current | $I_{IN}$ | | OE, $\overline{OE}$, S = 0 to 5.5 V | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±1.0 | μA |
| Leakage current form $V_{CCB}$ to $V_{CCA}$ | $I_{CCBA}$ | | OE, $\overline{OE}$ = GND or $V_{CCA}$ $V_{CCB} \rightarrow V_{CCA}$ | 3.3 | 5.0 | — | 20.0 | μA |
| Quiescent supply current | $I_{CCA1}$ | | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 4.0 | μA |
| | $I_{CCB1}$ | | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 4.0 | |
| | $I_{CCA2}$ | | $V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±4.0 | |
| | $I_{CCB2}$ | | $V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±4.0 | |

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

## 12.2. DC Characteristics (Note) (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage (OE/$\overline{OE}$, S) | $V_{IH}$ | | — | 1.65 ≤ $V_{CCA}$ < 2.3 | $V_{CCA}$ to 5.5 | 0.8 × $V_{CCA}$ | — | V |
| | | | | 2.3 ≤ $V_{CCA}$ < 5.0 | $V_{CCA}$ to 5.5 | 0.7 × $V_{CCA}$ | — | |
| Low-level input voltage (OE/$\overline{OE}$, S) | $V_{IL}$ | | — | 1.65 ≤ $V_{CCA}$ < 2.3 | $V_{CCA}$ to 5.5 | — | 0.2 × $V_{CCA}$ | V |
| | | | | 2.3 ≤ $V_{CCA}$ < 5.0 | $V_{CCA}$ to 5.5 | — | 0.3 × $V_{CCA}$ | |
| ON-resistance | $R_{ON}$ | (Note 1) | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA See Figure 13.1 | 1.65 | 2.3 | — | 25.0 | Ω |
| | | | | 2.3 | 3.0 | — | 16.0 | |
| | | | | 3.0 | 4.5 | — | 12.0 | |
| Power-OFF leakage current | $I_{OFF}$ | | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V (per circuit) | 0 | 0 | — | ±4.0 | μA |
| Switch OFF-state leakage current | $I_{SZ}$ | | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V OE = GND, $\overline{OE}$ = $V_{CCA}$ | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±4.0 | |
| Input leakage current | $I_{IN}$ | | OE, $\overline{OE}$, S = 0 to 5.5 V | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±4.0 | μA |
| Leakage current form $V_{CCB}$ to $V_{CCA}$ | $I_{CCBA}$ | | OE, $\overline{OE}$ = GND or $V_{CCA}$ $V_{CCB}$ → $V_{CCA}$ | 3.3 | 5.0 | — | 40.0 | μA |
| Quiescent supply current | $I_{CCA1}$ | | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 20.0 | |
| | $I_{CCB1}$ | | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 20.0 | |
| | $I_{CCA2}$ | | $V_{CCA}$ ≤ OE, $\overline{OE}$ ≤ 5.5 V, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±20.0 | |
| | $I_{CCB2}$ | | $V_{CCA}$ ≤ OE, $\overline{OE}$ ≤ 5.5 V, $I_{IS}$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±20.0 | |

Note: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

## 12.3. Level Shift Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input/Output characteristics (translating up) | $V_{OHU}$ | (Note 1) | 1A, 2A = $V_{IN}$ SW = ON See Fig. 15.1. | 1.65 | 3.0 to 5.5 | 1.4 | — | V |
| | | | | 2.3 | 4.5 to 5.5 | 2.05 | — | |
| | | | | 3.0 | 4.5 to 5.5 | 2.7 | — | |
| Input/Output characteristics (translating down) | $V_{OHD}$ | (Note 2) | 1A, 2A = $V_{CCA}$ SW = ON See Fig. 16.1. | 1.65 | 3.3 to 5.5 | 1.3 | 1.65 | V |
| | | | | 2.3 | 4.5 to 5.5 | 1.95 | 2.3 | |
| | | | | 3.0 | 4.5 to 5.5 | 2.6 | 3.0 | |

Note 1: The Input/Output characteristics for translating up indicate the input voltages required to provide $V_{CCA}$ + 0.5 V on the outputs when measured using the test circuitry shown in Fig. 15.1.

Note 2: The Input/Output characteristics for translating down indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Fig. 16.1.

## 12.4. Level Shift Characteristics (Note) (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Note | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$(V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input/Output characteristics (translating up) | $V_{OHU}$ | (Note 1) | 1A, 2A = $V_{IN}$ SW = ON See Fig. 15.1. | 1.65 | 3.0 to 5.5 | 1.4 | — | V |
| | | | | 2.3 | 4.5 to 5.5 | 2.05 | — | |
| | | | | 3.0 | 4.5 to 5.5 | 2.7 | — | |
| Input/Output characteristics (translating down) | $V_{OHD}$ | (Note 2) | 1A, 2A = $V_{CCA}$ SW = ON See Fig. 16.1. | 1.65 | 3.3 to 5.5 | 1.3 | 1.65 | V |
| | | | | 2.3 | 4.5 to 5.5 | 1.95 | 2.3 | |
| | | | | 3.0 | 4.5 to 5.5 | 2.6 | 3.0 | |

Note: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: The Input/Output characteristics for translating up indicate the input voltages required to provide $V_{CCA}$ + 0.5 V on the outputs when measured using the test circuitry shown in Fig. 15.1.

Note 2: The Input/Output characteristics for translating down indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Fig. 16.1.

## 12.5. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

### 12.5.1. $V_{CCA}$ = 3.3 ± 0.3 V, $V_{CCB}$ = 5.0 ± 0.5 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.3 | ns |
| | $t_{PHL}$ | | | — | 1.2 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 9.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 11.0 | ns |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### 12.5.2. $V_{CCA}$ = 2.5 ± 0.2 V, $V_{CCB}$ = 5.0 ± 0.5 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.35 | ns |
| | $t_{PHL}$ | | | — | 1.8 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 13.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 15.0 | ns |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### 12.5.3. $V_{CCA}$ = 2.5 ± 0.2 V, $V_{CCB}$ = 3.3 ± 0.3 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.45 | ns |
| | $t_{PHL}$ | | | — | 2.2 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 17.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 19.0 | ns |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## 12.6. AC Characteristics (Note) (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

### 12.6.1. $V_{CCA}$ = 3.3 ± 0.3 V, $V_{CCB}$ = 5.0 ± 0.5 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.5 | ns |
| | $t_{PHL}$ | | | — | 1.4 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 13.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 15.0 | ns |

Note: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### 12.6.2. $V_{CCA}$ = 2.5 ± 0.2 V, $V_{CCB}$ = 5.0 ± 0.5 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.55 | ns |
| | $t_{PHL}$ | | | — | 2.0 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 17.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 19.0 | ns |

Note: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### 12.6.3. $V_{CCA}$ = 2.5 ± 0.2 V, $V_{CCB}$ = 3.3 ± 0.3 V

| Characteristics | Symbol | Note | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (bus to bus) | $t_{PLH}$ | (Note 1) | See Fig. 14.1, 14.3 | — | 0.65 | ns |
| | $t_{PHL}$ | | | — | 2.4 | |
| Output enable time | $t_{PZL}$ | | See Fig. 14.2, 14.4 | — | 21.0 | ns |
| Output disable time | $t_{PLZ}$ | | | — | 23.0 | ns |

Note: Operating Range spec of $T_{opr}$ = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## 12.7. Capacitive Characteristics (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Symbol | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Typ. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance (OE/$\overline{OE}$, S) | $C_{IN}$ | — | 3.3 | 3.3 | 3 | pF |
| Switch terminal ON-capacitance (1A, 2A) | $C_{I/O}$ | SW = ON (A, B) | 3.3 | 3.3 | 14 | pF |
| Switch terminal OFF-capacitance (1A, 2A) | | SW = OFF (A) | 3.3 | 3.3 | 7 | pF |
| Switch terminal OFF-capacitance (1B1, 1B2, 2B1, 2B2) | | SW = OFF (B) | 3.3 | 3.3 | 7 | |

## 13. DC Test Circuit

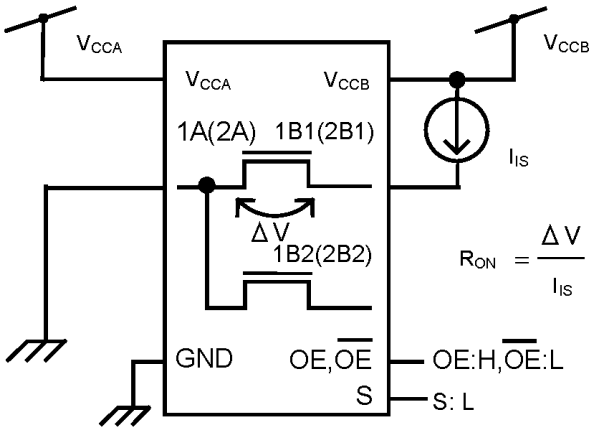



Fig. 13.1 ON-resistance Test Circuits

## 14. AC Test Circuits/Waveform

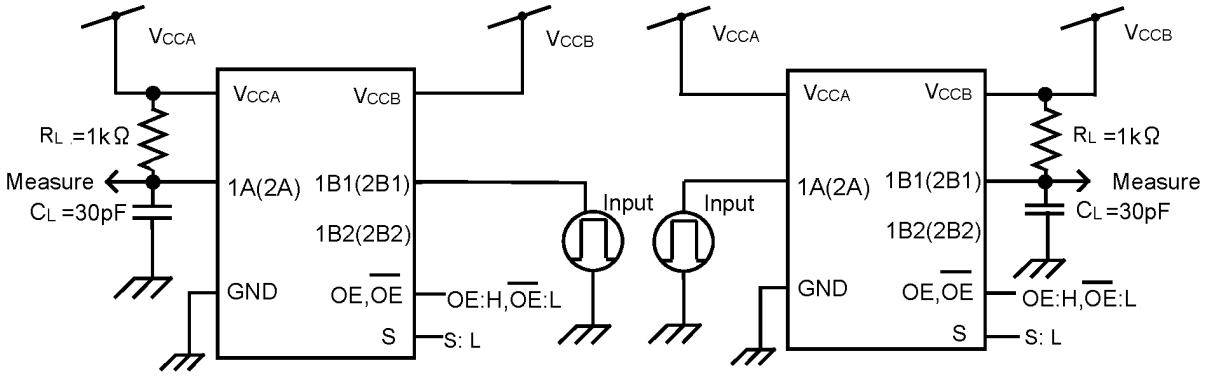



Fig. 14.1 $t_{PLH}$, $t_{PHL}$ Test Circuits

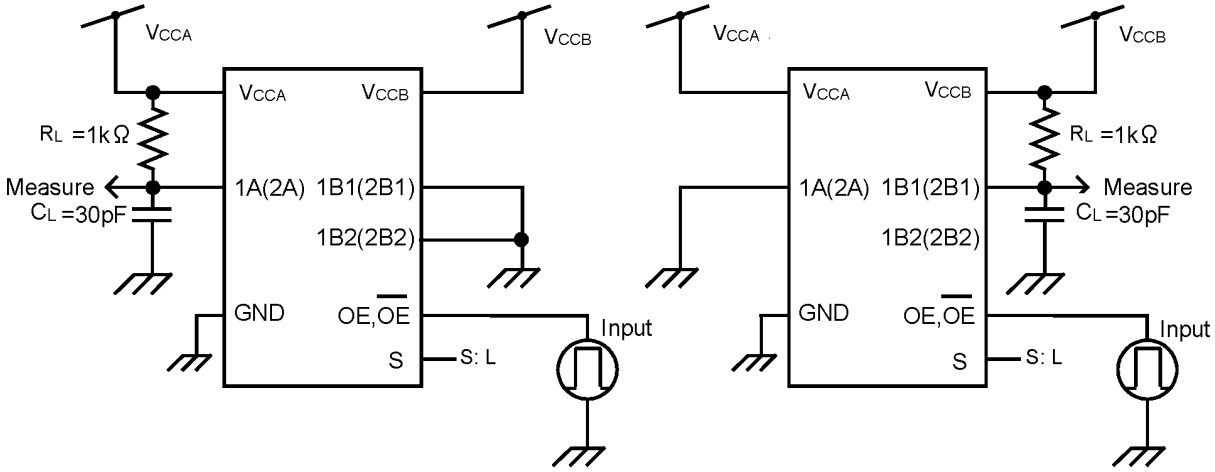



Fig. 14.2 $t_{PLZ}$, $t_{PZL}$ Test Circuits

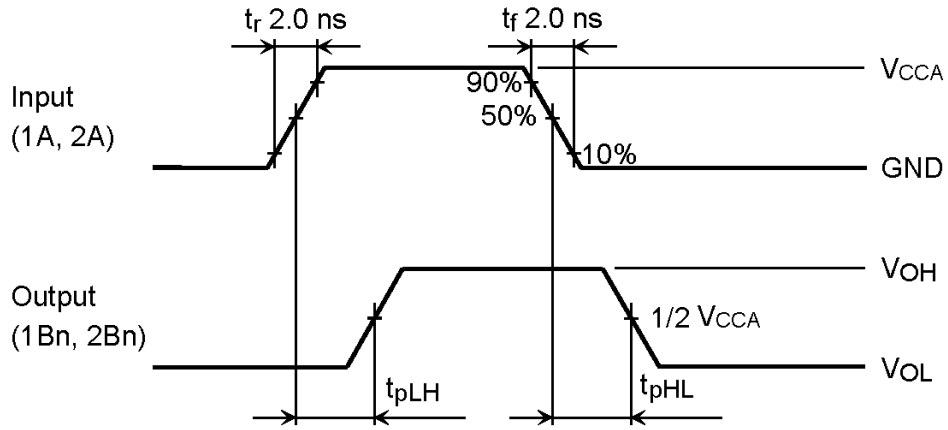



**Fig. 14.3 AC Waveform of $t_{PLH}$, $t_{PHL}$**

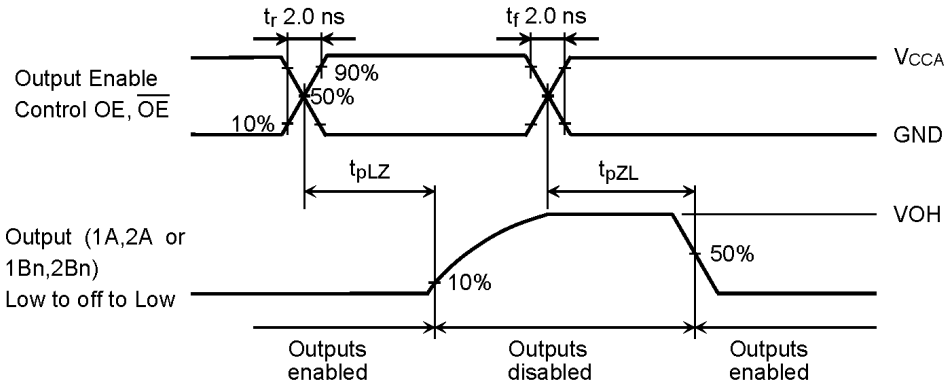



**Fig. 14.4 AC Waveform of $t_{PLZ}$, $t_{PZL}$**

## 15. Level Shift Function (Used Pull-up Resistance)

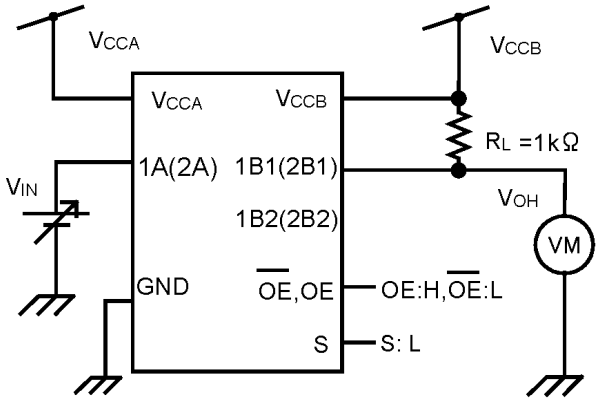



**Fig. 15.1 Test Circuit**

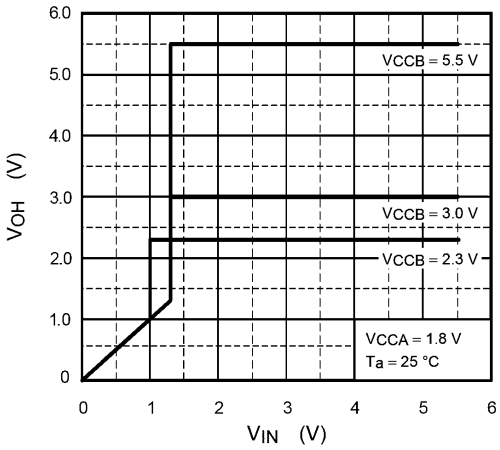



**Fig. 15.2 Input/Output Characteristics (Typ.)**
**$V_{CCA}$ = 1.8 V, $T_a$ = 25 °C**

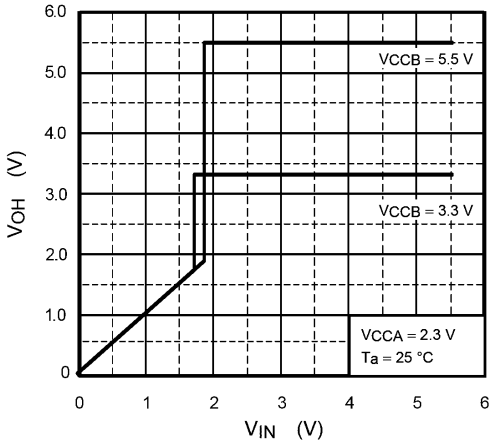



**Fig. 15.3 Input/Output Characteristics (Typ.)**
**$V_{CCA}$ = 2.3 V, $T_a$ = 25 °C**

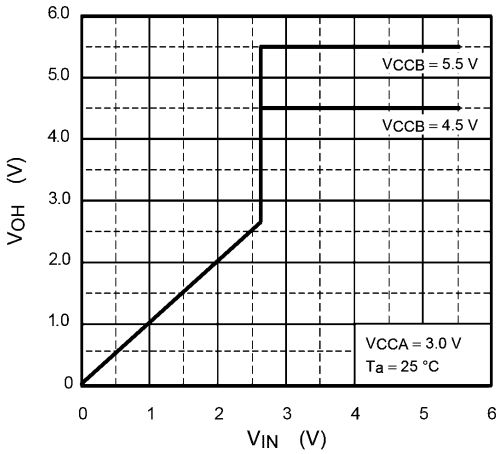



**Fig. 15.4 Input/Output Characteristics (Typ.)**
**$V_{CCA}$ = 3.0 V, $T_a$ = 25 °C**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 16. Level Shift Function (Unused Pull-up Resistance)

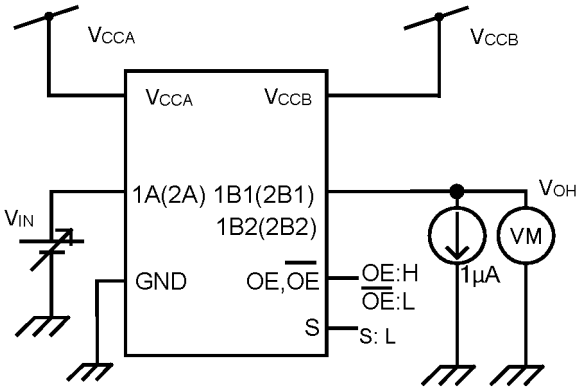



Fig. 16.1 Test Circuit

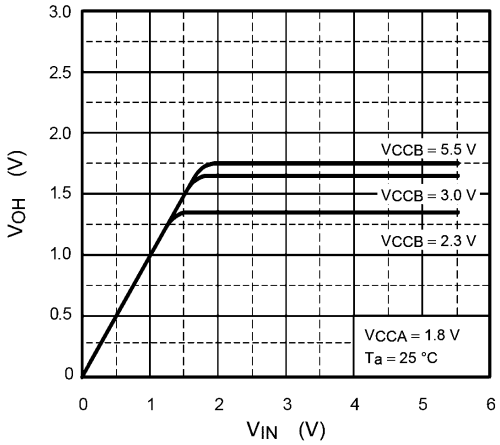



Fig. 16.2 Input/Output Characteristics (Typ.)
$V_{CCA}$ = 1.8 V, $T_a$ = 25 °C

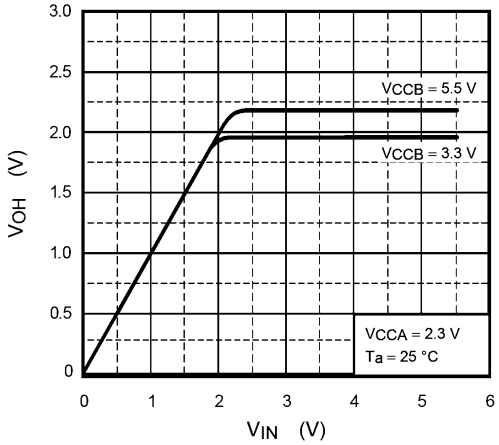



Fig. 16.3 Input/Output Characteristics (Typ.)
$V_{CCA}$ = 2.3 V, $T_a$ = 25 °C

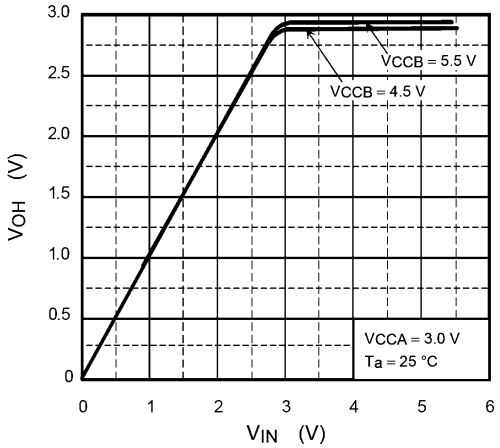
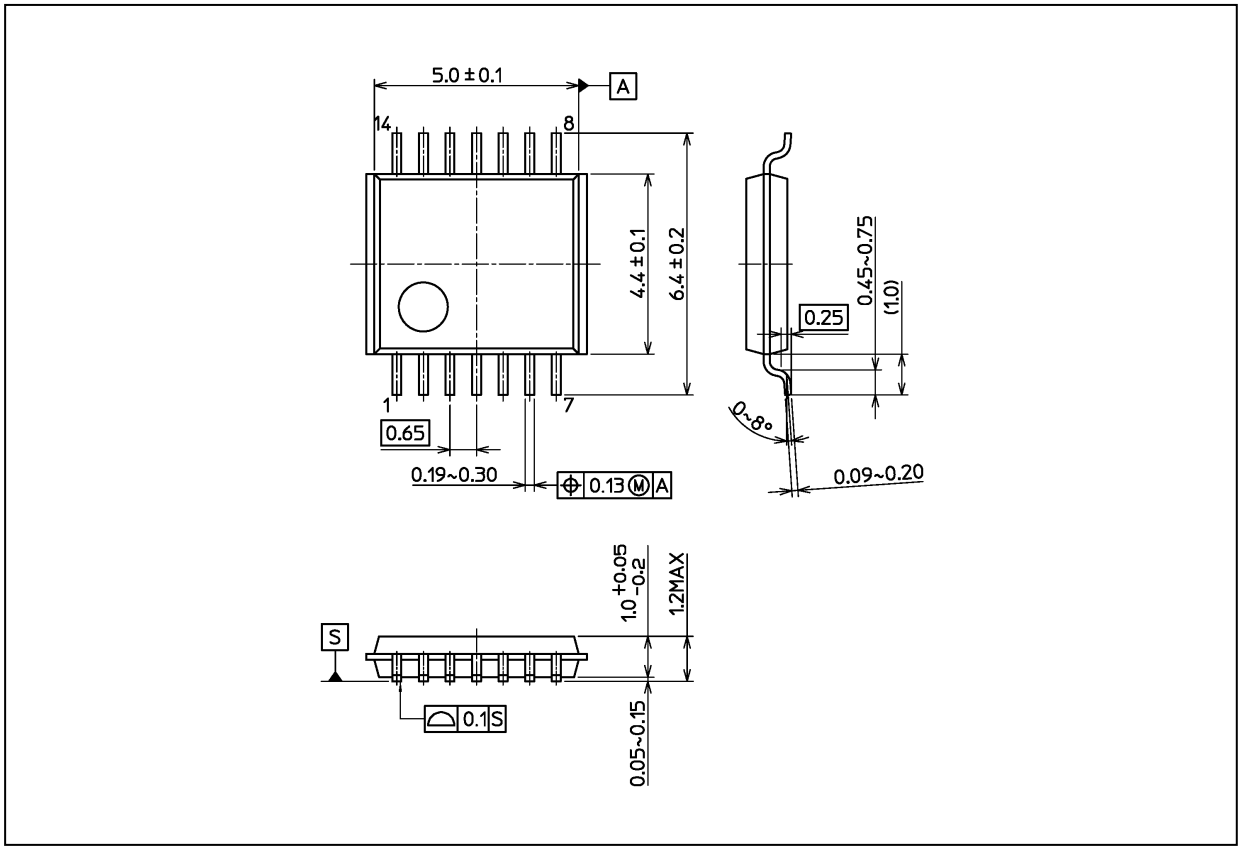



Fig. 16.4 Input/Output Characteristics (Typ.)
$V_{CCA}$ = 3.0 V, $T_a$ = 25 °C

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm

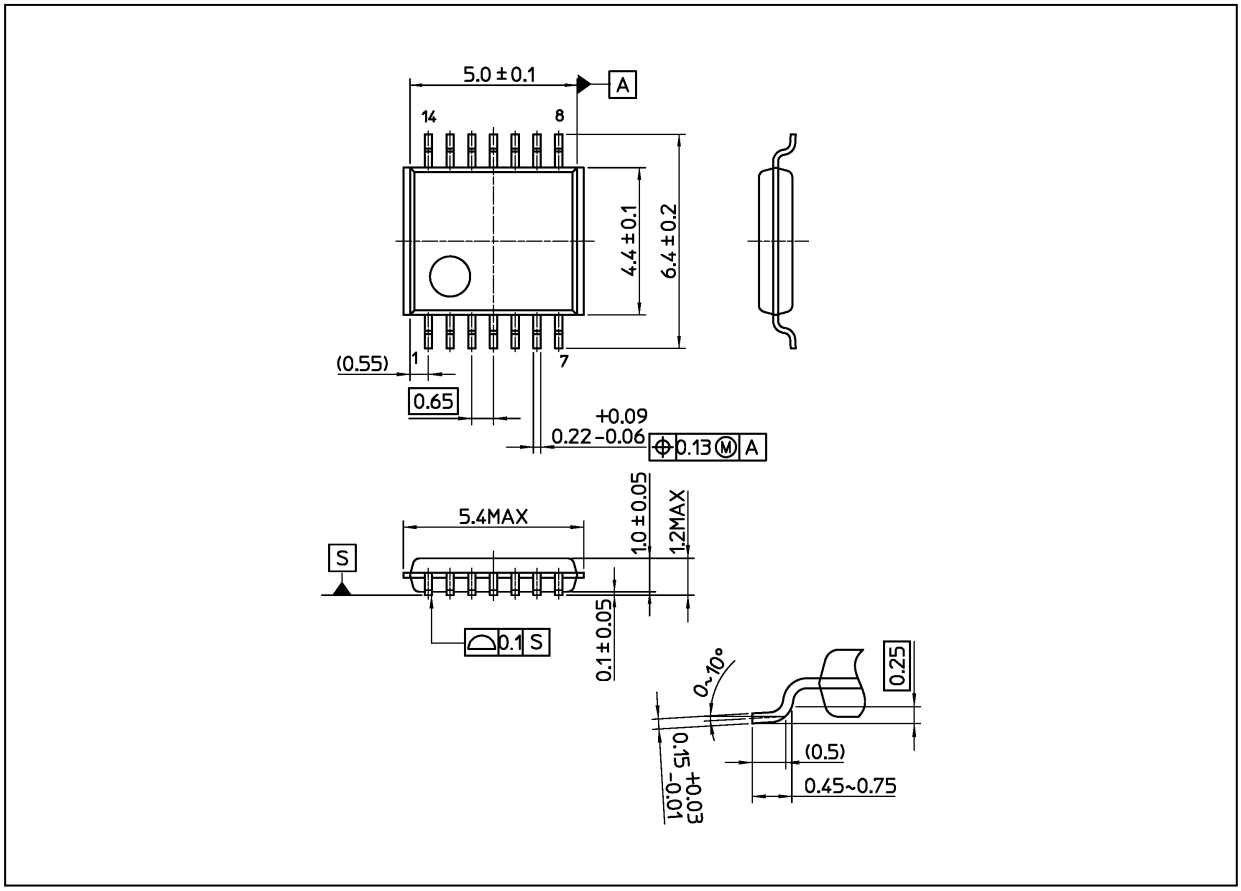



Weight: 0.054 g (typ.)

| Package Name(s) |
|---|
| TOSHIBA: P-TSSOP14-0044-0.65-001 |
| Nickname: TSSOP14B |

## Package Dimensions

Unit: mm




Weight: 0.06 g (typ.)

| Package Name(s) |
| --- |
| Nickname: TSSOP14 |

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