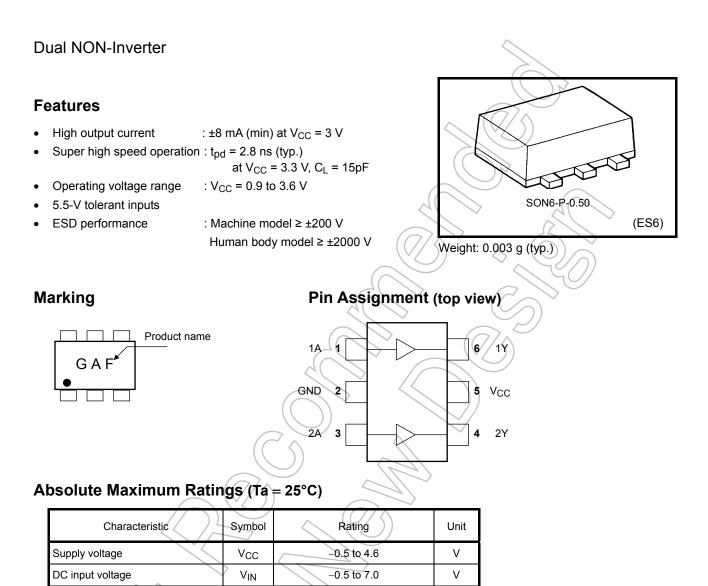
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7PG34AFE



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

-0.5 to V_{CC} + 0.5

-20

 ± 20

±25

±100

150

-65 to 150

Vout

ΙIK

lok

OUT

lcc

RD

T_{stg}

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

V

mΑ

mΑ

mΑ

mΑ

mW

°C

(Note 1)

Note 1:
$$V_{OUT} < GND$$
, $V_{OUT} > V_{CC}$

DC output voltage

Input diode current

Output diode current

DC V_{CC}/GND current

Storage temperature

DC output current

Power dissipation

Start of commercial production 2006-12

<u>TOSHIBA</u>

IEC Logic Symbol

Truth Table

	OUT Y	F	А	Y]
		F	L H	L H	-
		L	п		
perating Ranges					\sum
Characteristic	Symbol	Rati	ng	Unit	1
Supply voltage	V _{CC}	0.9 to	3.6	V	
nput voltage	V _{IN}	0 to	5.5	V Y V	
Dutput voltage	V _{OUT}	0 to \	/cc	V	
		±8.0) (N	ote 2)	
		±4.0		ote 3)	\sim
		±3.0	(N	ote 4)	YM
Dutput current	I _{OH} /I _{OL}	(±1.7	(N	ote 5) mA	
		±0.3	ξ (N	ote 6)	
		±0.0	2 (N	ote 7)	/
Operating temperature	T _{opr}	-40 to	o 85	0°C	
Input rise and fall time	dt/dv	0 to	10 (No	ote 8) ns/V	
Note 2: $V_{CC} = 3.0$ to 3.6 V	6				
Note 3: $V_{CC} = 2.3$ to 2.7 V					
Note 4: $V_{CC} = 1.65$ to 1.95 V	(P)		\ \		
Note 5: $V_{CC} = 1.4$ to 1.6 V	(\bigcirc)				
Note 6: $V_{CC} = 1.1$ to 1.3 V			$\langle \rangle$		
Note 7: $V_{CC} = 0.9 V$	(\mathcal{Q})		\geq		
Note 8: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} =$	3.0 V	$\langle (// 5) \rangle$			
\sim					
	\land	\checkmark			
	\triangleleft				
		>			
	(())				
	\searrow				

Electrical Characteristics

DC Characteristics

Characteristic	Symbol	Test Condition			$Ta = 25^{\circ}C$ $Ta = -40 \text{ to } 85^{\circ}C$				to 85°C	Unit
		Test Condition		V _{CC} (V)	Min	Тур.	Max	Min	Max	Onit
				0.9	V _{CC}	_	A	V _{CC}		V
	VIH			1.1 to 1.3	$V_{CC} \times 0.7$	_	$\left(\begin{array}{c} \\ \end{array} \right)$	V _{CC} × 0.7	_	
High-level input voltage				1.4 to 1.6	V _{CC} × 0.65	-((775	V _{CC} × 0.65	—	
				1.65 to 1.95	V _{CC} × 0.65		\bigcirc	V _{CC} × 0.65	_	
				2.3 to 2.7	1.7	(-)	2	1.7	—	
				3.0 to 3.6	2.0	\geq		2.0	_	
				0.9	4	\searrow	GND	A	GND	V
Low-level input voltage				1.1 to 1.3	775	>	V _{CC} × 0.3	57	V _{CC} × 0.3	
	V _{IL}			1.4 to 1.6		_	V _{CC} × 0.35	F D) V _{CC} × 0.35	
				1.65 to 1.95	<u> </u>	- (V _{CC} × 0.35	>_	$\begin{array}{c} V_{CC} \\ \times \ 0.35 \end{array}$	
		(2.3 to 2.7	_	\square	0.7		0.7	l
			20	3.0 to 3.6			0.8		0.8	
	V _{OH}	VIN = VIH	I _{OH} =-0.02 mA	0.9	0.75	$\langle - \rangle$	_	0.75	—	
High-level output voltage			I _{OH} = -0.3 mA	1.1 to 1.3	V _{CC} × 0.75	$) \rightarrow$		V _{CC} × 0.75	—	
			IOH = -1.7 mA	1.4 to 1.6	V _{CC} × 0.75	~	_	$V_{CC} \times 0.75$	_	V
			IOH = -3.0 mA	1.65 to 1.95	Vcc -0,45	—	—	V _{CC} -0.45	_	
			l _{OH} = -4.0 mA	2.3 to 2.7	2.0	—	—	2.0	_	
) >	I _{OH} = -8.0 mA	3.0 to 3.6	2.48	_	_	2.48	—	
Low-level output voltage	\leq		l _{OL} = 0.02 mA	0.9	_	_	0.1	—	0.1	
	VOL		I _{OL} = 0.3 mA	1.1 to1.3	_	_	$\begin{array}{c} V_{CC} \\ \times \ 0.25 \end{array}$		$\begin{array}{c} V_{CC} \\ \times \ 0.25 \end{array}$	
		$V_{IN} = V_{IL}$	I _{OL} = 1.7 mA	1.4 to 1.6	_	_	V _{CC} × 0.25	_	V _{CC} × 0.25	, v
	\sim		loL = 3.0 mA	1.65 to 1.95	_	_	0.45	_	0.45	
)		l _{OL} = 4.0 mA	2.3 to 2.7	—	—	0.4	—	0.4	
		γ ((I _{OL} = 8.0 mA	3.0 to 3.6	—	—	0.4	—	0.4	
Input leakage current	IIN	$V_{IN} = 0$ to 5.5V		0 to 3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current	Icc	V _{IN} = V _{CC} or GND		3.6	_	_	1.0		10.0	μA

AC Characteristics (unless otherwise specified, Input: $t_r = t_f = 3 \text{ ns}$)

Characteristic	Symbol	Toot Condition		Ta = 25°C		Ta = -40	to 85°C	L Incid	
Characteristic		Test Condition	V _{CC} (V)	Min	Тур.	Max	Min	Max	Unit
Propagation delay time	t _{pLH} t _{pHL}	$C_L = 10 \text{ pF},$ $R_L = 1 \text{ M}\Omega$	0.9	_	27.2		—	—	
			1.1 to 1.3	_	12.2	23.2	1.0	42.6	ns
			1.4 to 1.6		6.5	10.2	1.0	12.0	
			1.65 to 1.95		4.7	7.0	1,0	7.6	
			2.3 to 2.7	_	3.1	4.4	1.0	4.9	
			3.0 to 3.6	- <	2.4	3.5	1.0	4.1	
		$C_L = 15 \text{ pF},$ $R_L = 1 \text{ M}\Omega$	0.9	_	29.8		—	—	
			1.1 to 1.3	_	13.5	26.0	1.0	44.5	
			1.4 to 1.6	76	7.2	11.4	1.0	13.6	
			1.65 to 1.95	4	5.2	7.5	1.0	7.7	
			2.3 to 2.7		3.4	4.8	21.0	5.5	
			3.0 to 3.6	//-5)	2.8	3.8((1.0	4.4	
		$C_L = 30 \text{ pF},$ $R_L = 1 \text{ M}\Omega$	0.9		40.7		~~/	/ _	
			1.1 to 1.3	\rightarrow	17.8	33.9	1.0	64.1	
			1.4 to 1.6	_	9.1	14.3	1.0	17.4	
			1.65 to 1,95	_	6.6	9.8	1.0	10.2	
			2.3 to 2.7		4.1	6.2	1.0	6.6	
			3.0 to 3.6	/	3.3	4.8	1.0	5.2	
Input capacitance	C _{IN}		3.6	X	3	—	—	—	pF
Power dissipation capacitance	C _{PD}	(Note 9)	0.9 to 3.6		6	—	—	—	pF

Note 9: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

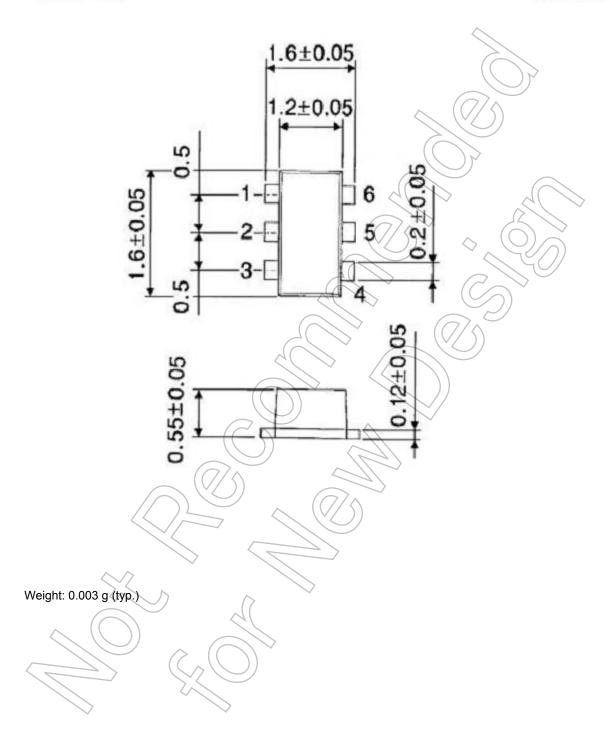
Average operating current can be obtained by the equation:

 $I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$

Package Dimensions

SON6-P-0.50

Unit : mm



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