

TC7USB40FT

1. Functional Description

- Dual SPDT USB Switch

2. General

The TC7USB40FT is high-speed CMOS dual 1-2 multiplexer/demultiplexer. The low ON-resistance and the low capacitance of the switch allow connections to USB2.0 (480Mbps) application.

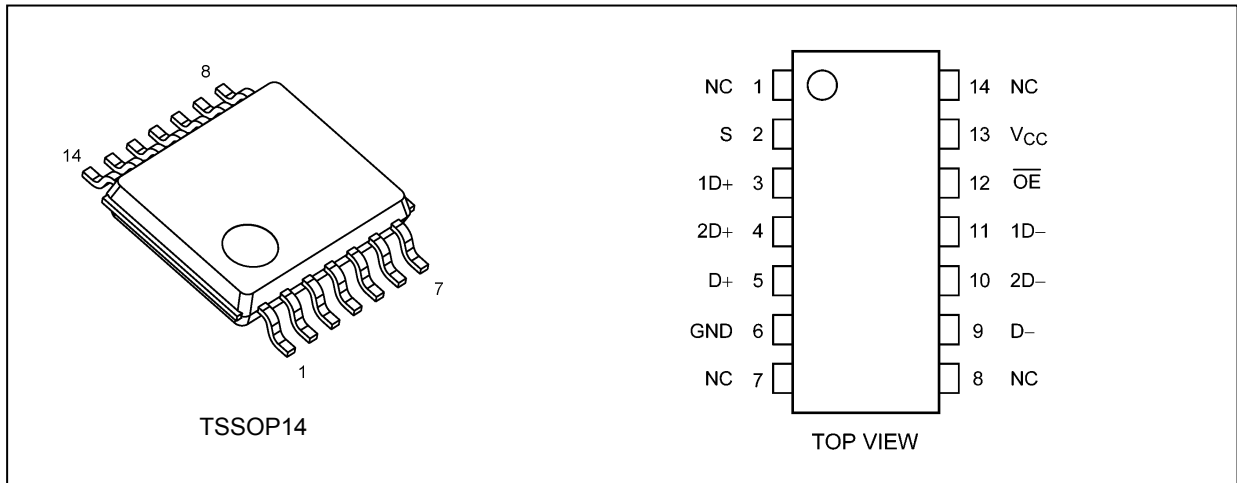
This device consists of dual individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable (\overline{OE}). The D+/D- inputs is connected to the 1D+/1D- or 2D+/2D- outputs determined by the combination both the select input (S) and output enable (\overline{OE}). When the output enable (\overline{OE}) input is held high level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

3. Features

- (1) Supply voltage: $V_{CC} = 2.3$ to 4.3 V
- (2) Switch terminal ON-capacitance: $C_{I/O} = 5$ pF Switch ON (typ.) @ $V_{CC} = 3.3$ V
- (3) ON-resistance: $R_{ON} = 4.5 \Omega$ (typ.) @ $V_{CC} = 3$ V, $V_{IS} = 0$ V
- (4) R_{ON} flatness: $R_{ON(Flat)} = 1.3 \Omega$ (typ.) @ $V_{CC} = 3$ V
- (5) Difference of ON-resistance between switches: $\Delta R_{ON} = 0.35 \Omega$ (typ.) @ $V_{CC} = 3$ V
- (6) ESD performance: Machine model $\geq \pm 200$ V, Human body model $\geq \pm 8000$ V
- (7) Power-down protection provided on all inputs and outputs.
- (8) Package: TSSOP14

4. Packaging and Pin Assignment



5. Marking

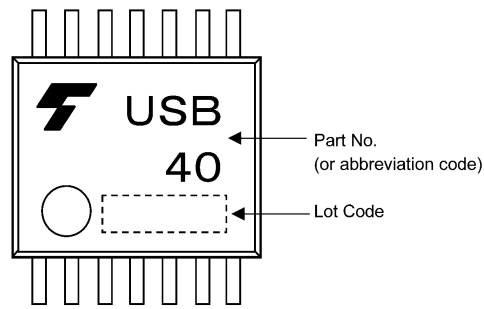


Fig. 5.1 Marking (Top view)

6. Block Diagram

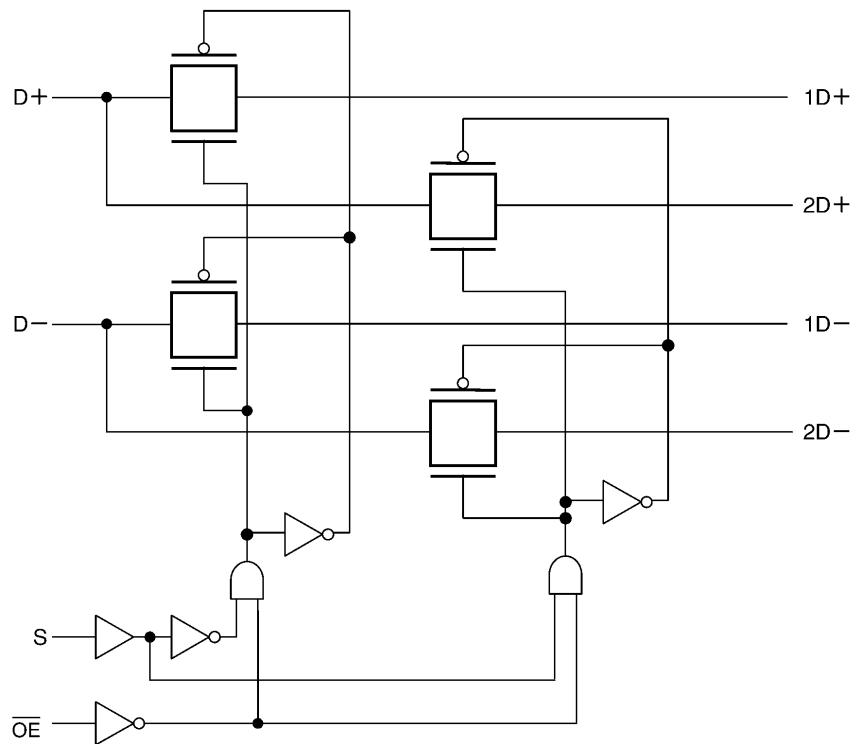


Fig. 6.1 Block Diagram

7. Principle of Operation

7.1. Truth Table

Input \overline{OE}	Input S	Function
L	L	D+ port = 1D+ port, D- Port = 1D- Port
L	H	D+ port = 2D+ port, D- Port = 2D- Port
H	X	Disconnect

X: Don't care

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	-0.5 to 4.6	V
Input voltage (\overline{OE} , S)	V_{IN}			-0.5 to 4.6	
Switch I/O voltage	V_S		$V_{CC} = 0$ V or Switch OFF	-0.5 to 4.6	
			Switch ON	0.5 to $V_{CC} + 0.5$	
Clamp diode current	I_{IK}		Control input	-50	mA
			Switch	± 50	
Switch I/O current	I_S		—	50	
Power dissipation	P_D			200	mW
V_{CC} /ground current	I_{CC}/I_{GND}			± 100	mA
Storage temperature	T_{stg}			-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	2.3 to 4.3	V
Input voltage (\overline{OE} , S)	V_{IN}			0 to 4.3	
Switch I/O voltage	V_S		$V_{CC} = 0$ V or Switch OFF	0 to 4.3	
			Switch ON	0 to V_{CC}	
Operating temperature	T_{opr}		—	-40 to 85	°C
Input rise time	dt/dv			0 to 10	ns/V
Input fall time				0 to 10	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

10. Electrical Characteristics

10.1. DC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage ($\overline{\text{OE}}$, S)	V_{IH}		—	2.3 to 3.0	$0.50 \times V_{CC}$	—	—	V
				3.0 to 4.3	$0.46 \times V_{CC}$	—	—	
Low-level input voltage ($\overline{\text{OE}}$, S)	V_{IL}		—	2.3 to 4.3	—	—	$0.25 \times V_{CC}$	
Input leakage current ($\overline{\text{OE}}$, S)	I_{IN}		$V_{IN} = 0$ to 4.3 V	2.3 to 4.3	—	—	± 1	μA
Power-OFF leakage current	I_{OFF}		$V_{IN} = V_{IS} = 0$ to 4.3 V, See Fig. 11.10	0	—	—	± 2	
Switch OFF-state leakage current	I_{SZ}		$V_{IS} = 0$ to 3.6V, $\overline{\text{OE}} = V_{CC}$, See Fig. 11.11	2.3 to 4.3	—	—	± 2	
ON-resistance	R_{ON}	(Note 1)	$V_{IS} = 0$ V, $I_{IS} = 30$ mA, See Fig. 11.9	3.0	—	4.5	6	Ω
			$V_{IS} = 0.4$ V, $I_{IS} = 30$ mA, See Fig. 11.9	3.0	—	4.8	6.7	
			$V_{IS} = 3.0$ V, $I_{IS} = 30$ mA, See Fig. 11.9	3.0	—	10	14	
Difference of ON-resistance between switches	ΔR_{ON}	(Note 1)	$V_{IS} = 0.4$ V, 1.0 V, $I_{IS} = 30$ mA	3.0	—	0.35	—	
ON-resistance flatness	$R_{ON(\text{flat})}$	(Note 1)	$V_{IS} = 0$ V to 1.0 V, $I_{IS} = 30$ mA	3.0	—	1.3	—	
Quiescent supply current	I_{CC}		$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ A	4.3	—	—	1	μA
	ΔI_{CC}		$V_{IN} = 2.6$ V (one input)	4.3	—	—	40	

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Note 1: Measured by the voltage drop between D+/D- and 1D+/1D-, 2D+/2D- pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two pins.

10.2. AC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Propagation delay time	t_{PLH}/t_{PHL}	(Note 1)	$C_L = 5$ pF, See Fig. 11.1	3.3 ± 0.3	—	0.25	—	ns
Turn-ON time (S, $\overline{\text{OE}}$ to output)	t_{on}		$R_L = 50 \Omega$, $C_L = 5$ pF, See Fig. 11.2		—	10	20	
Turn-OFF time (S, $\overline{\text{OE}}$ to output)	t_{off}				—	14	24	
Break before make	TBBM		$R_L = 50 \Omega$, $C_L = 5$ pF, See Fig. 11.3		2	—	7	
Skew of opposite transitions of the same output ($t_{PHL} - t_{PLH}$)	$t_{SK(P)}$	(Note 1)	$C_L = 5$ pF, See Fig. 11.4		—	0.1	—	
Output skew (center port to any other port)	$t_{SK(O)}$	(Note 1)	$C_L = 5$ pF, See Fig. 11.5		—	0.1	—	

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Note 1: Parameter guaranteed by design.

10.3. Analog Switch (Note) (Unless otherwise specified, $T_a = -40$ to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
OFF isolation (non-adjacent)	OIRR		$R_T = 50 \Omega$, $f = 240 \text{ MHz}$, See Fig. 11.6	3.3 ± 0.3	—	-24	—	dB
Crosstalk (non-adjacent)	Xtalk		$R_T = 50 \Omega$, $f = 240 \text{ MHz}$, See Fig. 11.7		—	-30	—	
-3dB Bandwidth	BW		$R_T = 50 \Omega$, $C_L = 0 \text{ pF}$, See Fig. 11.8		—	1500	—	MHz

Note: All typical values are at $T_a = 25^\circ\text{C}$.
Parameter guaranteed by design.

10.4. Capacitive Characteristics (Note) (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance (\overline{OE} , S)	C_{IN}		$V_{IN} = 0 \text{ V}$	3.3	3	pF
Switch terminal OFF-capacitance (D+, D-)	$C_{I/O}$		$\overline{OE} = V_{CC}$, $V_{IS} = 0 \text{ V}$		3	
Switch terminal OFF-capacitance (1D+, 1D-, 2D+, 2D-)					2	
Switch terminal ON-capacitance					5	

Note: Parameter guaranteed by design.

11. AC Test Circuits and Waveforms

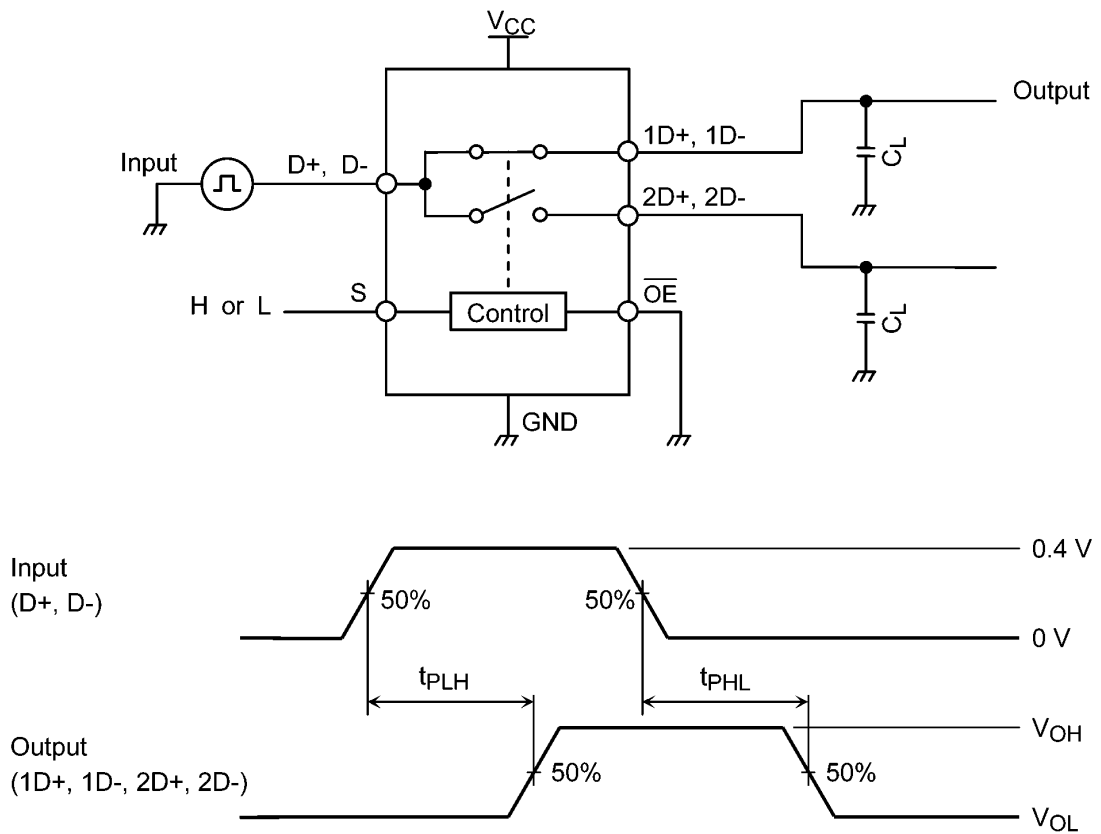


Fig. 11.1 Propagation Delay Time (t_{PLH}, t_{PHL})

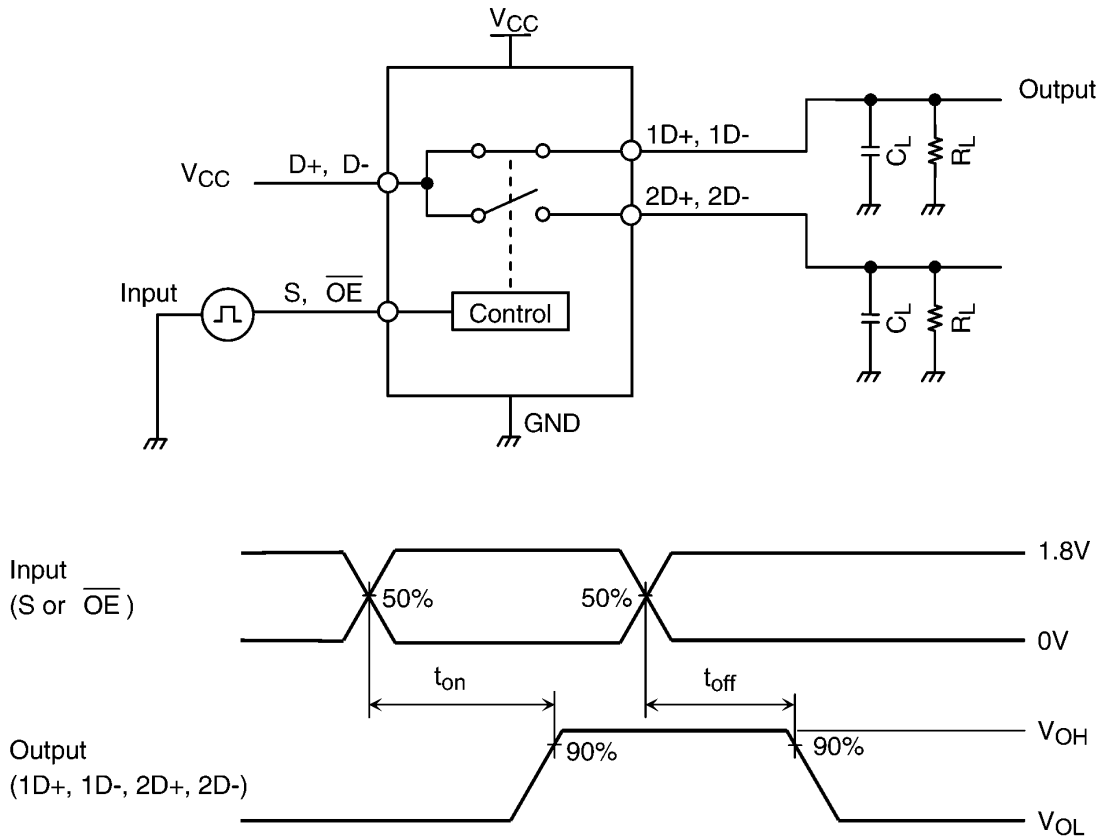


Fig. 11.2 Turn-ON and Turn-OFF Times (t_{on} , t_{off})

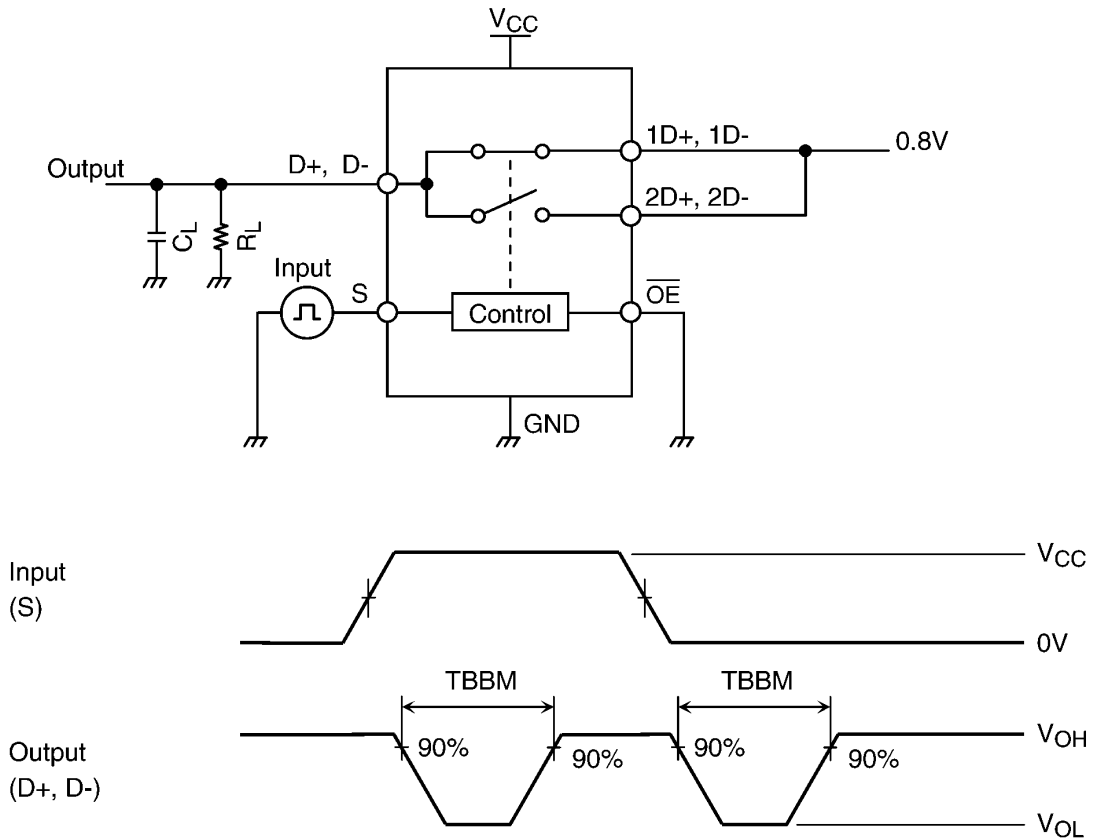


Fig. 11.3 Break Before Make (TBBM)

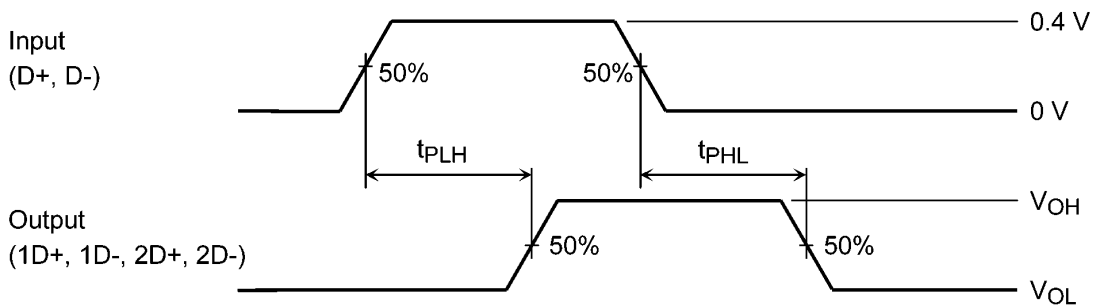
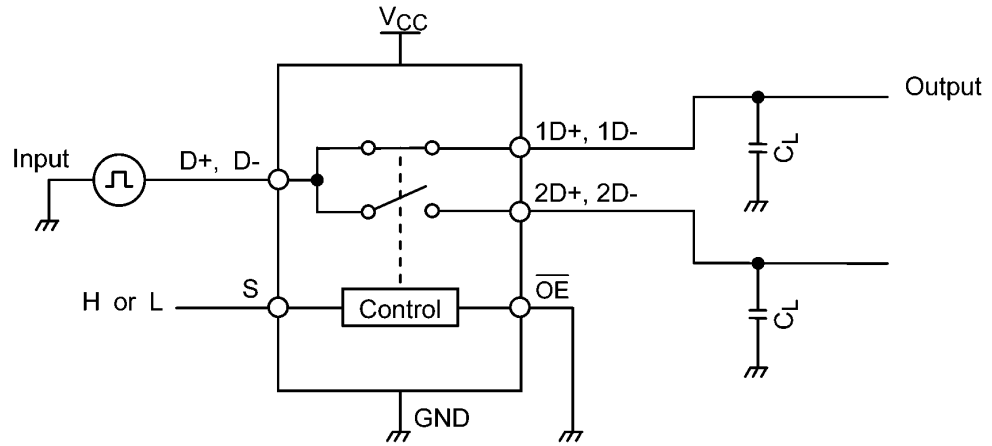


Fig. 11.4 Skew of opposite transitions of the same output ($t_{SK(P)} = |t_{PHL} - t_{PLH}|$)

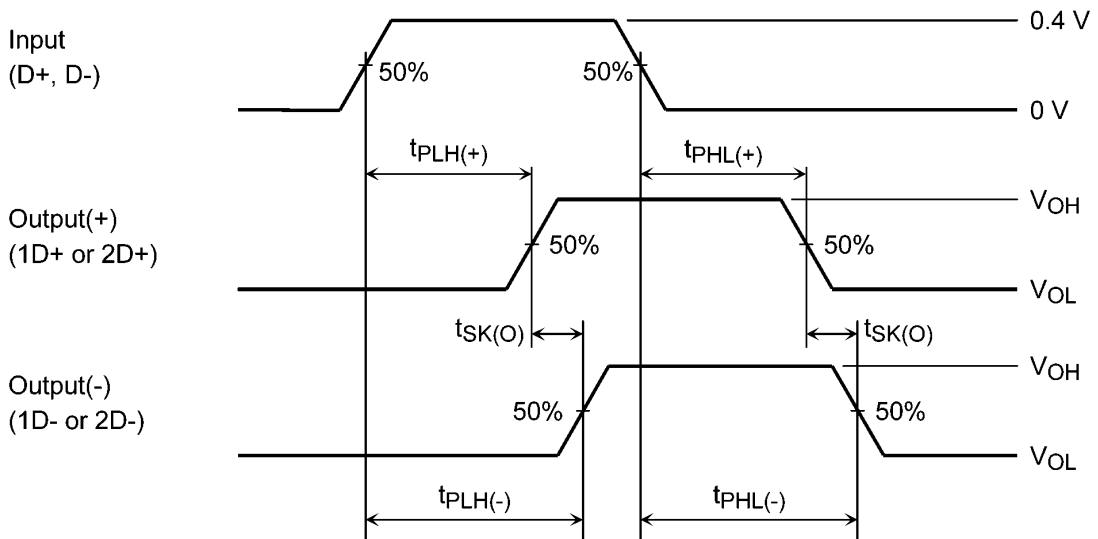


Fig. 11.5 Output Skew (center port to any other port)

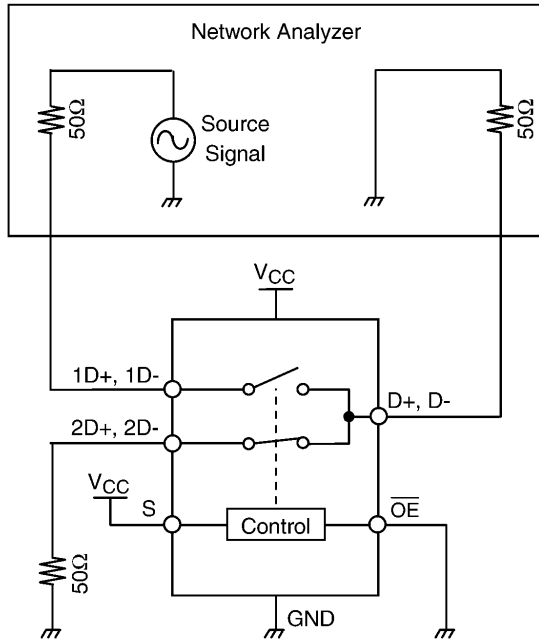


Fig. 11.6 OFF Isolation

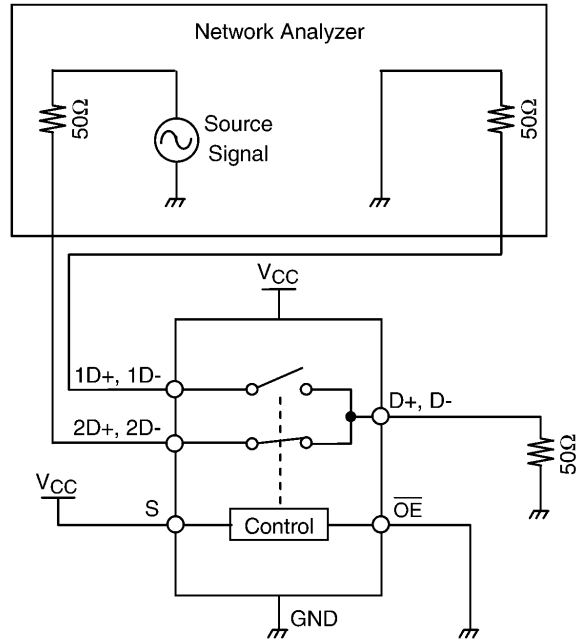


Fig. 11.7 Crosstalk

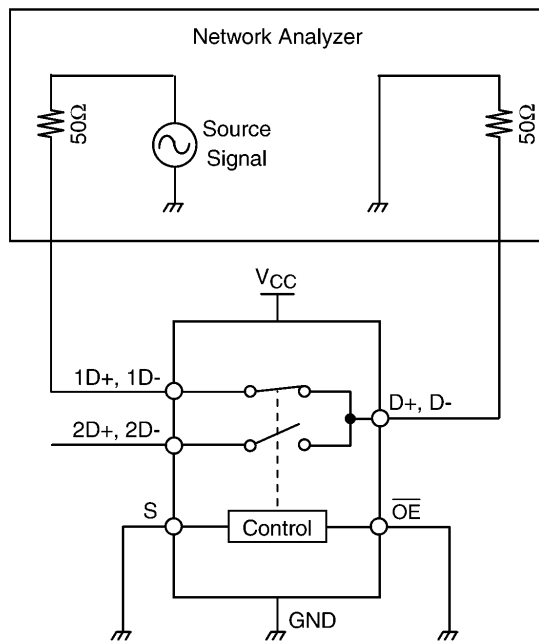


Fig. 11.8 -3dB Bandwidth

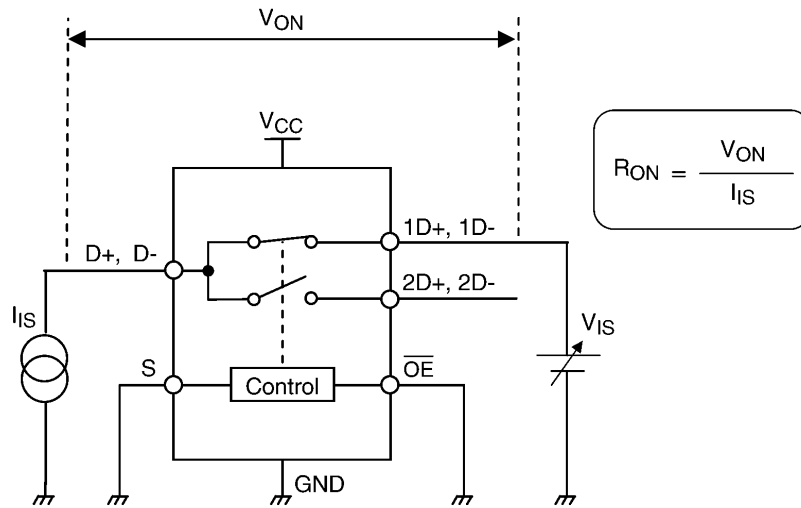


Fig. 11.9 ON-Resistance

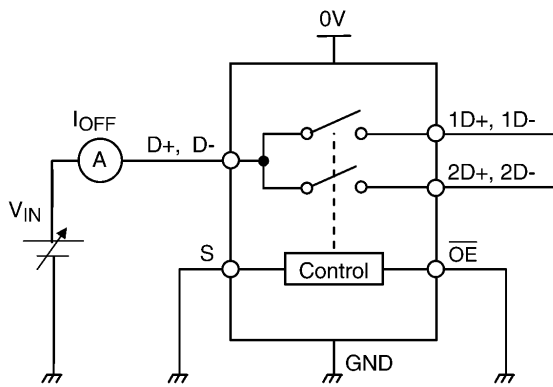


Fig. 11.10 Power-OFF Leakage Current

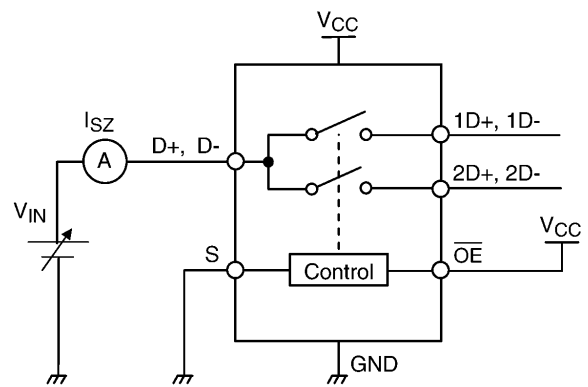
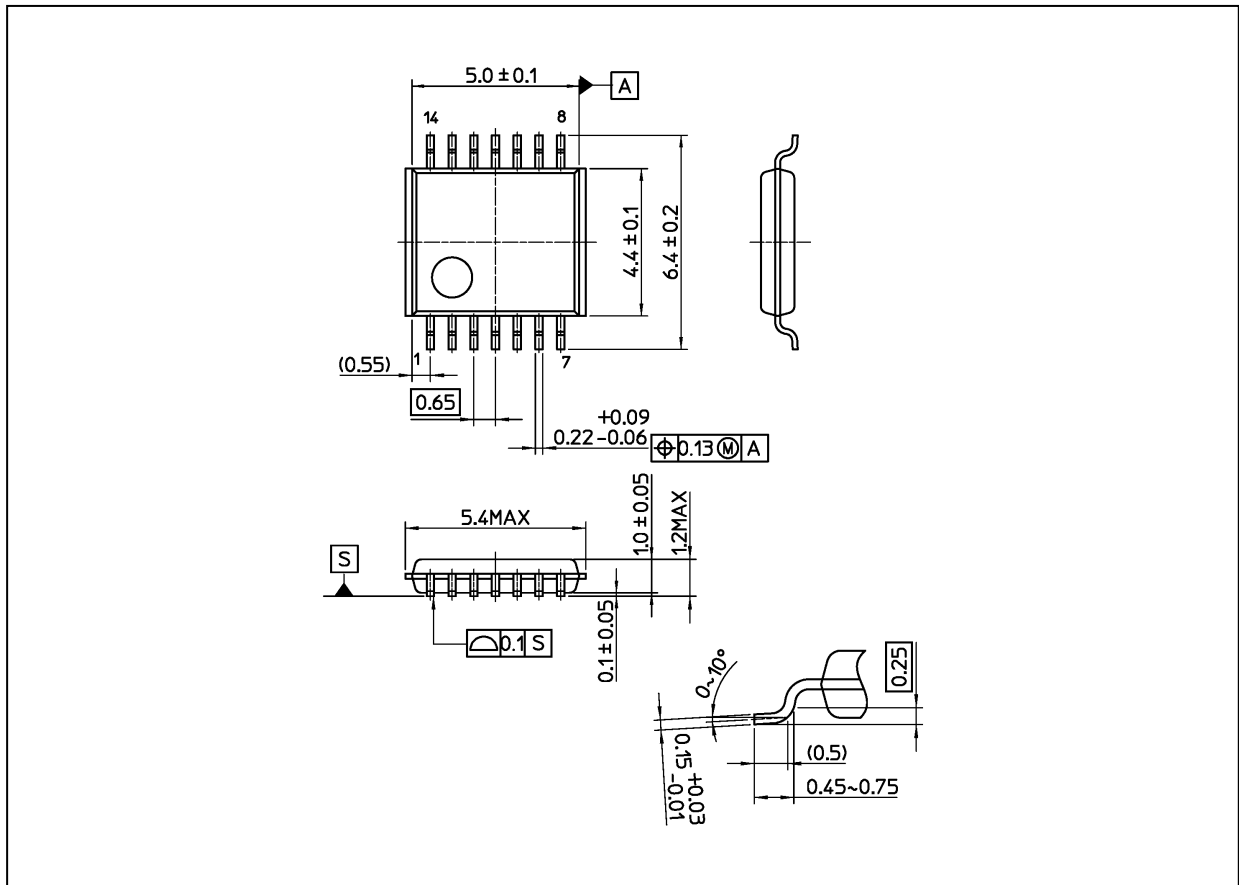


Fig. 11.11 Switch OFF-state leakage current

Package Dimensions

Unit: mm



Weight: 0.06 g (typ.)

Package Name(s)
TOSHIBA: TSSOP14-P-0044-0.65S
Nickname: TSSOP14

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