TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH123FU, TC7WH123FK

Monostable Multivibrator

The TC7WH123 is high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (t_r = t_f = 1 s) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (R_X, C_X). A low level at the $\overline{CLR}$ input breaks this state.

Limits for C_X and R_X are:

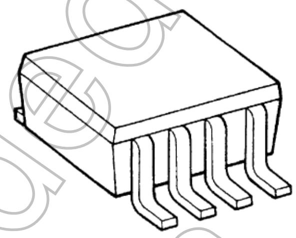
External capacitor, C_X: No limit

External resistor, R_X: V_{CC} = 2.0 V more than 5 kΩ

V_{CC} ≥ 3.0 V more than 1 kΩ

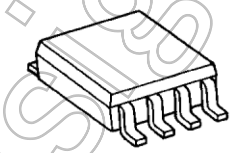
An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC7WH123FU



SSOP8-P-0.65 (SM8)

TC7WH123FK



SSOP8-P-0.50A (US8)

Weight

SSOP8-P-0.65 : 0.02 g (typ.)

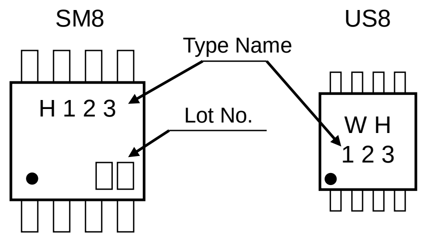
SSOP8-P-0.50A : 0.01 g (typ.)

Features

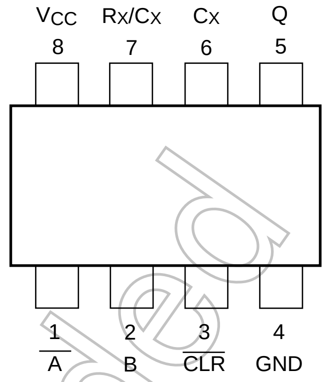
- High speed: t_{pd} = 8.1 ns (typ.) at V_{CC} = 5 V
- Low power dissipation
- Standby state: I_{CC} = 2 μA (max) at Ta = 25°C
- Active state : I_{CC} = 650 μA (max) at V_{CC} = 4.5 V
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is equipped with all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V

Start of commercial production
1998-08

Marking



Pin Assignment (top view)

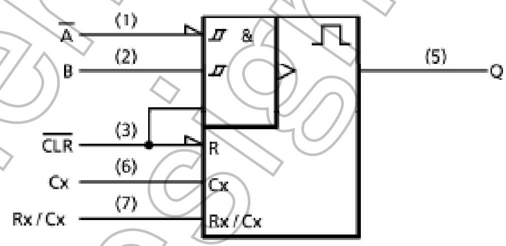


Truth Table

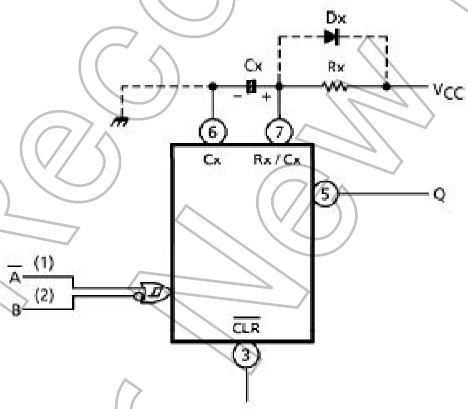
Inputs			Outputs	Note
$\overline{A}$	B	$\overline{CLR}$	Q	
↓	H	H	⊓	Output Enable
X	L	H	L	Inhibit
H	X	H	L	Inhibit
L	↑	H	⊓	Output Enable
L	H	↑	⊓	Output Enable
X	X	L	L	Reset

X: Don't care

IEC Logic Symbol



Block Diagram



Note: C_X, R_X, D_X are external capacitor, resistor, and diode, respectively.

Note: External clamping diode, D_X;

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.
If the supply voltage is turned off, C_X is discharges mainly through the internal (parasitic) diode. If C_X is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20 mA.
In the case of a large C_X, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (V_{CC} - 0.7) \cdot C_X / 20\ \text{mA}$$

(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC}.)

In the even a system does not satisfy the above condition, an external clamping diode (D_X) is needed to protect the IC from rush current.

Functional Description

(1) Standby state

The external capacitor (C_X) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the R_X/C_X node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C_1 and C_2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the R_X/C_X node drops. If the R_X/C_X voltage level falls to the internal reference voltage $V_{ref}L$, the output of C_1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C_1 stops but C_2 continues operating.

After Q_N turns off, the voltage at the R_X/C_X node starts rising at a rate determined by the time constant of external capacitor C_X and resistor R_X.

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of R_X/C_X changes from falling to rising. When R_X/C_X reaches the internal reference voltage $V_{ref}H$, the output of C_2 becomes low, the output Q goes low and C_2 stops its operation. That means, after triggering, when the voltage level of the R_X/C_X node reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

With large values of C_X and R_X, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, $t_{w\ OUT}$, is as follows:

$$t_{wOUT} = 1.0 \cdot C_X \cdot R_X$$

(3) Retrigger operation

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging C_X. The voltage level of the R_X/C_X node then falls to $V_{ref}L$ level again. Therefore the Q output stays high if the next trigger comes in before the time period set by C_X and R_X.

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, trr (min), depends on VCC and CX.

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_P turns on and C_X is charged rapidly to V_{CC}.

This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

Absolute Maximum Ratings (T_a = 25 °C) (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20 (Note 1)	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	300 (SM8)	mW
		200 (US8)	
Storage temperature	T_{stg}	-65 to 150	°C
Lead temperature (10 s)	T_L	260	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: V_{OUT}<GND, VOUT>V_{CC}

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V
External capacitor	C_X	No limitation (Note 1)	F
External resistor	R_X	≥ 5 k (V_{CC} = 2.0 V) (Note 1) ≥ 1 k (V_{CC} ≥ 3.0 V) (Note 1)	Ω

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 1: The maximum allowable values of C_X and R_X are a function of leakage of capacitor C_X, the leakage of TC7WH123FU/FK, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for R_X > 1 MΩ.

DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Input $t_r = t_f = 3$ ns)

CHARACTERISTIC		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0~5.5	V_{CC} ×0.7	—	—	V_{CC} ×0.7	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0~5.5	—	—	V_{CC} ×0.3	—	V_{CC} ×0.3	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				$I_{OH} = -4mA$	3.0	2.58	—	—	2.48	—	
				$I_{OH} = -8mA$	4.5	3.94	—	—	3.80	—	
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				$I_{OL} = 4mA$	3.0	—	—	0.36	—	0.44	
				$I_{OL} = 8mA$	4.5	—	—	0.36	—	0.44	
Control Input Current		I_{IN}	$V_{IN} = 5.5V$ or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Rx / Cx Terminal Off-State Current		I_{IN}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	±0.25	—	±0.25	μA
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	2.0	—	20.0	μA
		I_{CC}	$V_{IN} = V_{CC}$ or GND, Rx / Cx = $0.5V_{CC}$		3.0	—	160	250	—	280	
					4.5	—	380	500	—	650	
					5.5	—	560	750	—	975	

TIMING RECOMMENDATION (Input $t_r = t_f = 3$ ns)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width	t_w (L) t_w (H)		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Clear Width ($\overline{CLR}$)	t_w (L)		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Retrigger Time	t_{rr}	Rx = 1kΩ, Cx = 100pF	3.3 ± 0.3	60	—	—	ns
			5.0 ± 0.5	39	—	—	
		Rx = 1kΩ, Cx = 0.01μF	3.3 ± 0.3	1.5	—	—	μs
			5.0 ± 0.5	1.2	—	—	

AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Input t_r = t_f = 3 ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	CL (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (A , B-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	13.4	20.6	1.0	24.0	ns
				50	—	15.9	24.1	1.0	27.5	
			5.0 ± 0.5	15	—	8.1	12.0	1.0	14.0	
				50	—	9.6	14.0	1.0	16.0	
Propagation Delay Time ($\overline{CLR}$ trigger-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	14.5	22.4	1.0	26.0	
				50	—	17.0	25.9	1.0	29.5	
			5.0 ± 0.5	15	—	8.7	12.9	1.0	15.0	
				50	—	10.2	14.9	1.0	17.0	
Propagation Delay Time ($\overline{CLR}$-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	10.3	15.8	1.0	18.5	
				50	—	12.8	19.3	1.0	22.0	
			5.0 ± 0.5	15	—	6.3	9.4	1.0	11.0	
				50	—	7.8	11.4	1.0	13.0	
Output Pulse Width	t_{wOUT}	Cx = 28pF Rx = 2kΩ	3.3 ± 0.3	50	—	160	240	—	300	
			5.0 ± 0.5		—	133	200	—	240	
		Cx = 0.01μF Rx = 10kΩ	3.3 ± 0.3	50	90	100	110	90	110	μs
			5.0 ± 0.5		90	100	110	90	110	
		Cx = 0.1μF Rx = 10kΩ	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1	ms
			5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1	
Input Capacitance	C_{IN}					4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	73	—	—	—	

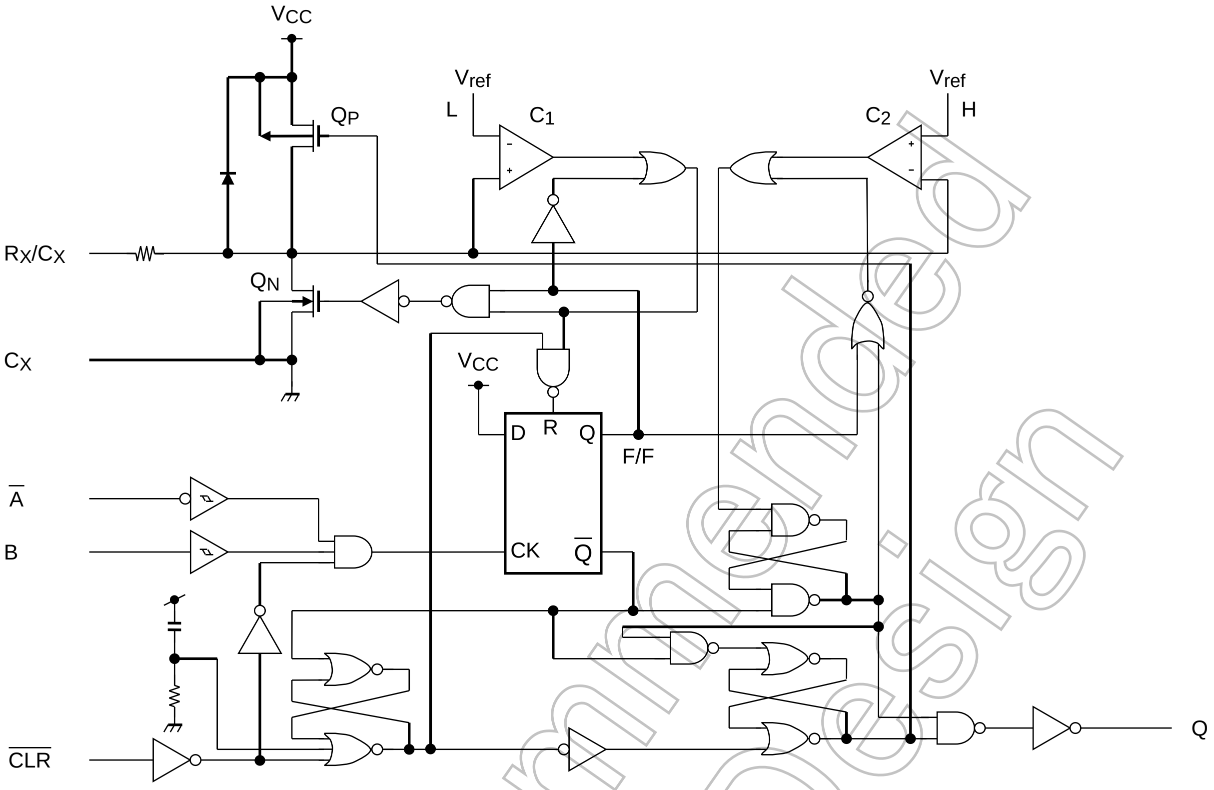
Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty / 100 + I_{CC}$

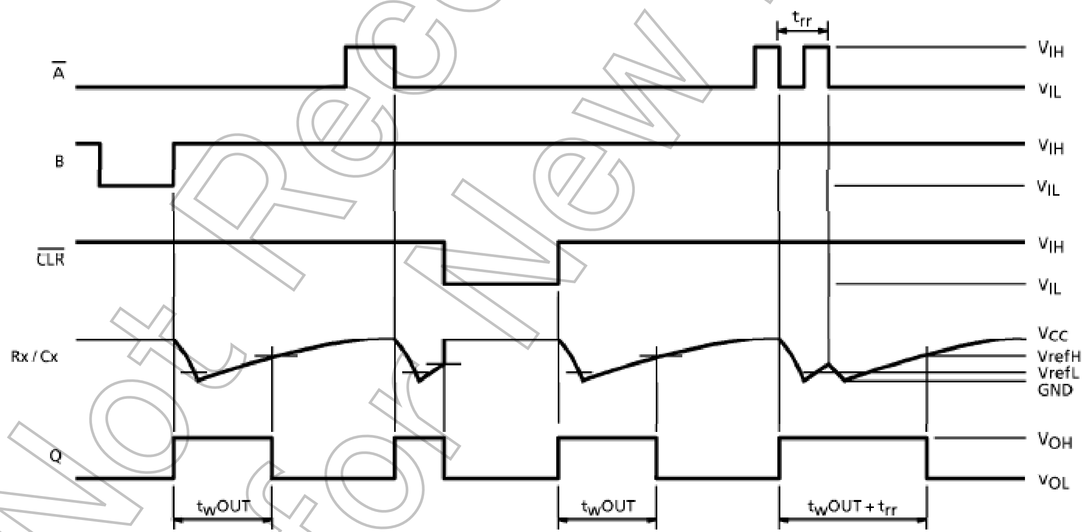
(I_{CC}' : Active Supply Current)

(Duty : %)

System Diagram

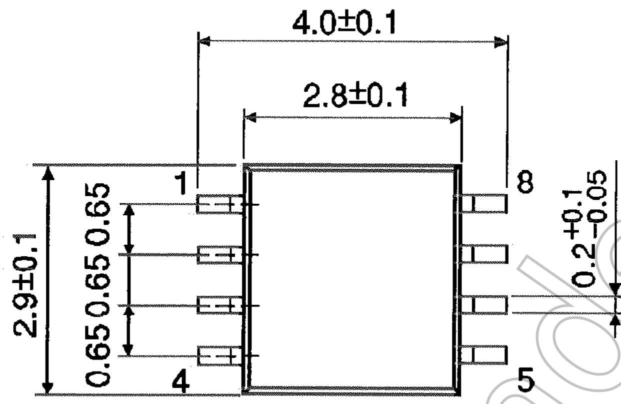


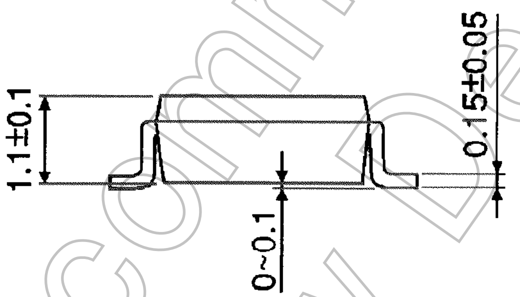
Timing Chart



Package Dimensions

SSOP8-P-0.65 Unit : mm

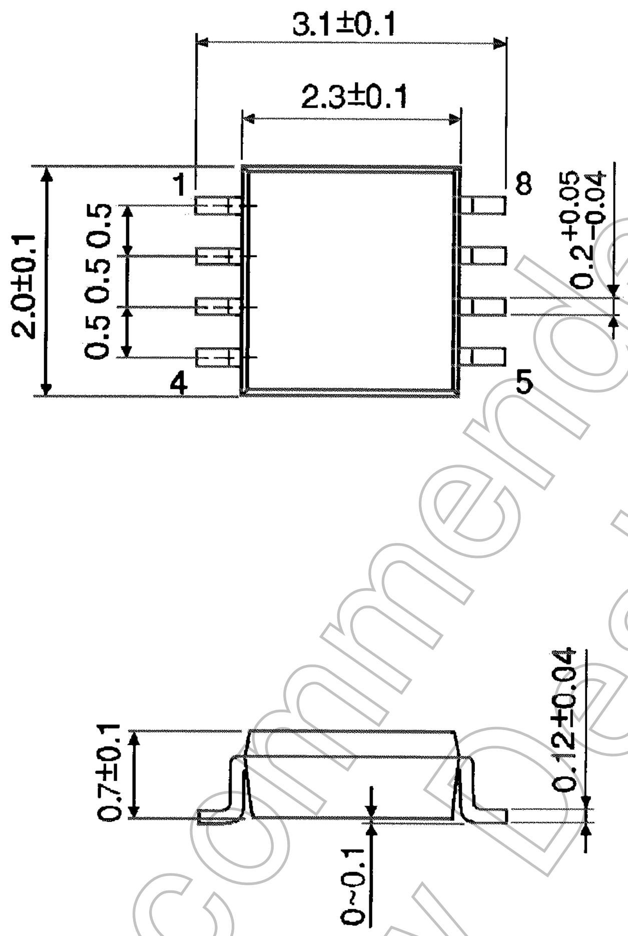




Weight: 0.02 g (Typ.)

Package Dimensions

SSOP8-P-0.50A Unit : mm



Weight: 0.01 g (Typ.)

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