CMOS Digital Integrated Circuits Silicon Monolithic

TC7WPB9306FK,TC7WPB9307FK

1. Functional Description

- Low-Voltage, Low-Power 2-Bit Dual-Supply Bus Switch

2. General

The TC7WPB9306FK and TC7WPB9307FK are CMOS 2-bit dual-supply bus switches that can provide an interface between two nodes at different voltage levels. These devices can be connected to two independent power supplies. V_{CCA} supports 1.8 V, 2.5 V and 3.3 V power supplies, whereas V_{CCB} supports 2.5 V, 3.3 V and 5.0 V power supplies.

Bidirectional level-shifting is possible by simply adding external pull-up resistors between the An/Bn data lines and the V_{CCA} / V_{CCB} supplies. There is no restriction on the relative magnitude of the An and Bn voltages; both the An and Bn data lines can be pulled up to arbitrary power supplies.

The enable signal can be used to disable the device so that the buses are effectively isolated.

The Output Enable (OE:TC7WPB9306FK, $\overline{OE}$:TC7WPB9307FK) input is common for all the 2-bits of the data lines; thus these device are used as a single 2-bits bus switch. For the TC7WPB9306FK, Output Enable (OE) is active-High: When OE is High, the switch is on; when Low, the switch is off. For the TC7WPB9307FK, Output Enable ($\overline{OE}$) is active-Low: When $\overline{OE}$ is Low, the switch is on; when High, the switch is off.

The TC7WPB9306FK and TC7WPB9307FK supports power-down protection at the $\overline{OE}$, OE input, with $\overline{OE}$, OE being 5.5 V tolerant.

The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.

3. Features

(1) AEC-Q100 (rev.H) Grade 1 qualified (Note 1)

(2) Wide operating temperature range: T_{opr} = -40 to 125 °C (Note 2)

(3) Operating voltage: 1.8 V to 2.5 V / 1.8 V to 3.3 V / 1.8 V to 5.0 V / 2.5 V to 3.3 V / 2.5 V to 5.0 V / 3.3 V to 5.0 V bidirectional interface

(4) Operating voltage: V_{CCA} = 1.65 to 5.0 V, V_{CCB} = 2.3 to 5.5 V

(5) Low ON-resistance: R_{ON} = 5.0 Ω (typ.) @ V_{IS} = 0 V, I_{IS} = 30 mA, V_{CCA} = 3.0 V, V_{CCB} = 4.5 V

(6) 5.5 V tolerance and power-down protection at the Output Enable input.

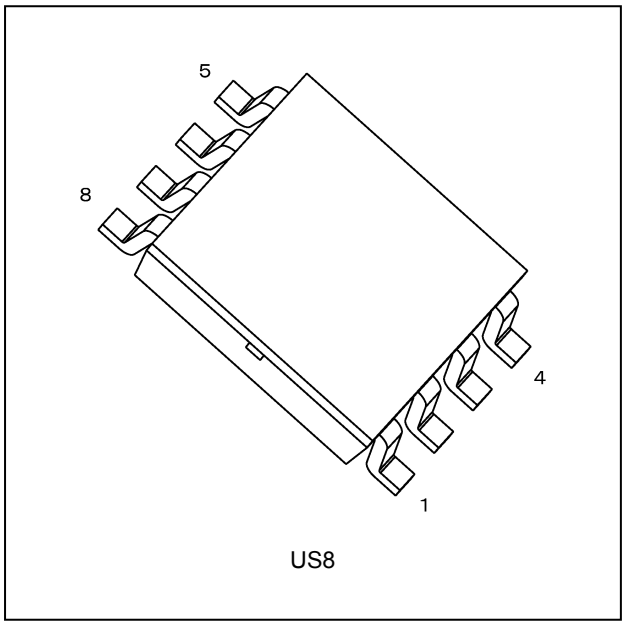
(7) Packages: US8

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

Note 2: For devices with the ordering part number ending in (CT. T_{opr} = -40 to 85 °C for the other devices.

Start of commercial production
2020-09

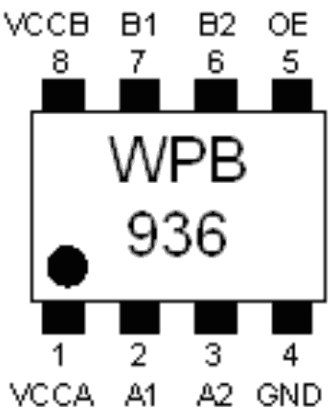
4. Packaging



US8

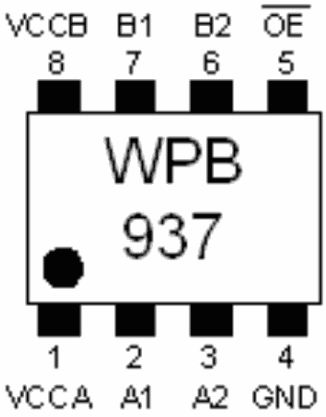
5. Pin Assignment

TC7WPB9306FK



(Top View)

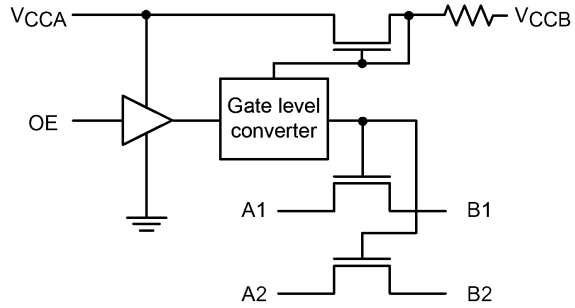
TC7WPB9307FK



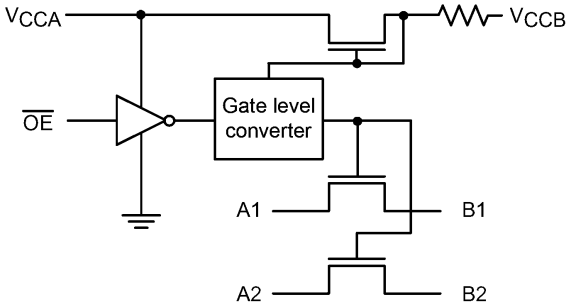
(Top View)

6. Block Diagram

TC7WPB9306FK



TC7WPB9307FK



7. Truth Table

Inputs OE (TC7WPB9306FK)	Function	Inputs $\overline{OE}$ (TC7WPB9307FK)	Function
L	Disconnect	L	A port = B port
H	A port = B port	H	Disconnect

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}		-0.5 to 7.0	V
	V_{CCB}		-0.5 to 7.0	
Input voltage	V_{IN}		-0.5 to 7.0	V
Switch I/O voltage	V_S		-0.5 to 7.0	V
Clamp diode current	I_{IK}		-50	mA
Switch I/O current	I_S		64	mA
V_{CC}/ground current per supply pin	I_{CCA}		±25	mA
	I_{CCB}		±25	
Power dissipation	P_D		200	mW
Storage temperature	T_{stg}		-65 to 150	°C

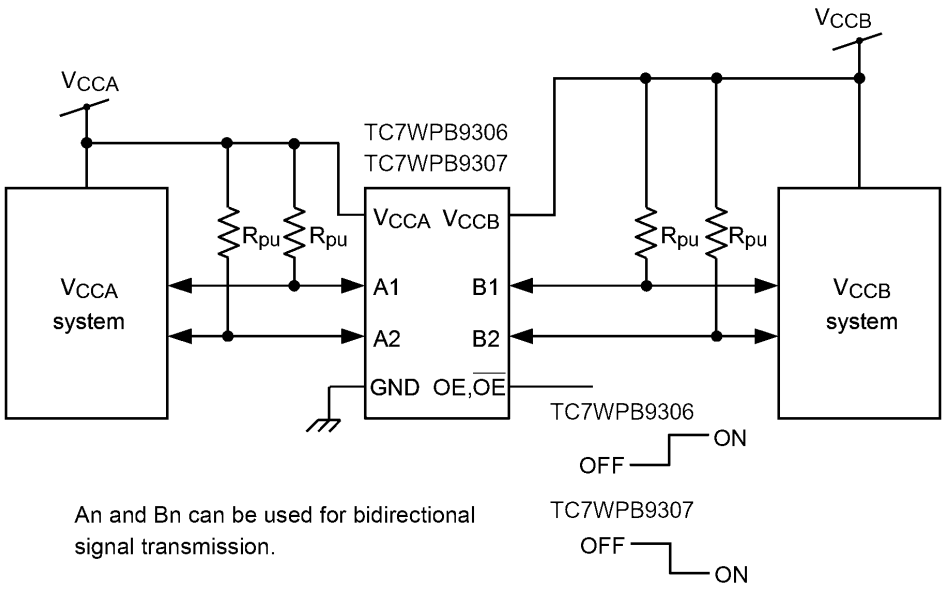
Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	1.65 to 5.0	V
	V_{CCB}		2.3 to 5.5	
Input voltage	V_{IN}		0 to 5.5	V
Switch I/O voltage	V_S		0 to 5.5	V
Operating temperature	T_{opr}	(Note 2)	-40 to 125	°C
		(Note 3)	-40 to 85	
Input rise time	dt/dv		0 to 10	ns/V
Input fall time	dt/dv		0 to 10	ns/V

Note : The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CCA} or GND.
Note 1: The V_{CCA} voltage must be lower than the V_{CCB} voltage.
Note 2: For devices with the ordering part number ending in (CT.
Note 3: For devices except those with the ordering part number ending in (CT.

10. Application Circuit (Note)



Note: The V_{CCA} < V_{CCB} voltage must be lower than the V_{CCB} voltage.

Note: Level-shifting functionality is enabled by adding pull-up resistors from An to V_{CCA} or V_{CCB} and from Bn to V_{CCB} or V_{CCA}, respectively.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IH}		—	$1.65 \le V_{CCA} < 2.3$	V_{CCA} to 5.5	$0.8 \times V_{CCA}$	—	V
				$2.3 \le V_{CCA} < 5.0$	V_{CCA} to 5.5	$0.7 \times V_{CCA}$	—	
Low-level input voltage	V_{IL}		—	$1.65 \le V_{CCA} < 2.3$	V_{CCA} to 5.5	—	$0.2 \times V_{CCA}$	V
				$2.3 \le V_{CCA} < 5.0$	V_{CCA} to 5.5	—	$0.3 \times V_{CCA}$	
ON-resistance	R_{ON}	(Note 1)	V_{IS} = 0 V, I_{IS} = 30 mA See Figure 12.1	1.65	2.3	—	16.0	Ω
				2.3	3.0	—	11.0	
				3.0	4.5	—	8.0	
Power-OFF leakage current	I_{OFF}		An, Bn = 0 to 5.5 V per circuit	0	0	—	±1.0	μA
Switch OFF-state leakage current	I_{SZ}		An, Bn = 0 to 5.5 V OE = GND, $\overline{OE}$ = V_{CCA}	1.65 to 5.0	V_{CCA} to 5.5	—	±1.0	μA
Input leakage current	I_{IN}		OE, $\overline{OE}$ = 0 to 5.5 V	1.65 to 5.0	V_{CCA} to 5.5	—	±1.0	μA
Leakage current form V_{CCB} to V_{CCA}	I_{CCBA}		OE, $\overline{OE}$ = GND or V_{CCA} $V_{CCB} \rightarrow V_{CCA}$	3.3	5.0	—	10.0	μA
Quiescent supply current	I_{CCA1}		OE, $\overline{OE}$ = V_{CCA} or GND, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	1.0	μA
	I_{CCB1}		OE, $\overline{OE}$ = V_{CCA} or GND, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	1.0	
	I_{CCA2}		$V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	±1.0	
	I_{CCB2}		$V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	±1.0	

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

11.2. DC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Note		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IH}		—	$1.65 \le V_{CCA} < 2.3$	V_{CCA} to 5.5	$0.8 \times V_{CCA}$	—	V
				$2.3 \le V_{CCA} < 5.0$	V_{CCA} to 5.5	$0.7 \times V_{CCA}$	—	
Low-level input voltage	V_{IL}		—	$1.65 \le V_{CCA} < 2.3$	V_{CCA} to 5.5	—	$0.2 \times V_{CCA}$	V
				$2.3 \le V_{CCA} < 5.0$	V_{CCA} to 5.5	—	$0.3 \times V_{CCA}$	
ON-resistance	R_{ON}	(Note 1)	V_{IS} = 0 V, I_{IS} = 30 mA See Figure 12.1	1.65	2.3	—	25.0	Ω
				2.3	3.0	—	16.0	
				3.0	4.5	—	12.0	
Power-OFF leakage current	I_{OFF}		An, Bn = 0 to 5.5 V Per circuit	0	0	—	±4.0	μA
Switch OFF-state leakage current	I_{SZ}		An, Bn = 0 to 5.5 V OE = GND, $\overline{OE}$ = V_{CCA}	1.65 to 5.0	V_{CCA} to 5.5	—	±4.0	μA
Input leakage current	I_{IN}		OE, $\overline{OE}$ = 0 to 5.5 V	1.65 to 5.0	V_{CCA} to 5.5	—	±4.0	μA
Leakage current form V_{CCB} to V_{CCA}	I_{CCBA}		OE, $\overline{OE}$ = GND or V_{CCA} $V_{CCB} \rightarrow V_{CCA}$	3.3	5.0	—	40.0	μA
Quiescent supply current	I_{CCA1}		OE, $\overline{OE}$ = V_{CCA} or GND, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	5.0	μA
	I_{CCB1}		OE, $\overline{OE}$ = V_{CCA} or GND, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	5.0	
	I_{CCA2}		$V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	±5.0	
	I_{CCB2}		$V_{CCA} \le$ OE, $\overline{OE} \le$ 5.5 V, I_{IS} = 0 A	1.65 to 5.0	V_{CCA}	—	±5.0	

Note 1: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

11.3. Level Shift Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
Input/Output characteristics (translating up)	V_{OHU}	(Note 1)	An = V_{IN} SW = ON See Fig. 14.1.	1.65	3.0 to 5.5	1.4	—	V
				2.3	4.5 to 5.5	2.05	—	
				3.0	4.5 to 5.5	2.7	—	
Input/Output characteristics (translating down)	V_{OHD}	(Note 2)	An = V_{CCA} SW = ON See Fig. 15.1.	1.65	3.0 to 5.5	1.3	1.65	V
				2.3	4.5 to 5.5	1.95	2.3	
				3.0	4.5 to 5.5	2.6	3.0	

Note 1: The Input/Output characteristics for translating up indicate the input voltages required to provide V_{CCA} + 0.5 V on the outputs when measured using the test circuitry shown in Fig. 14.1.

Note 2: The Input/Output characteristics for translating down indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Fig. 15.1.

11.4. Level Shift Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
Input/Output characteristics (translating up)	V_{OHU}	(Note 1)	An = V_{IN} SW = ON See Fig. 14.1.	1.65	3.0 to 5.5	1.4	—	V
				2.3	4.5 to 5.5	2.05	—	
				3.0	4.5 to 5.5	2.7	—	
Input/Output characteristics (translating down)	V_{OHD}	(Note 2)	An = V_{CCA} SW = ON See Fig. 15.1.	1.65	3.0 to 5.5	1.3	1.65	V
				2.3	4.5 to 5.5	1.95	2.3	
				3.0	4.5 to 5.5	2.6	3.0	

Note 1: The Input/Output characteristics for translating up indicate the input voltages required to provide V_{CCA} + 0.5 V on the outputs when measured using the test circuitry shown in Fig. 14.1.

Note 2: The Input/Output characteristics for translating down indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Fig. 15.1.

11.5. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

11.5.1. V_{CCA} = 3.3 ± 0.3 V, V_{CCB} = 5.0 ± 0.5 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.3	ns
	t_{PHL}			—	1.2	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	9.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	11.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.5.2. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 5.0 ± 0.5 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.35	ns
	t_{PHL}			—	1.8	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	13.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	15.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.5.3. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.45	ns
	t_{PHL}			—	2.2	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	17.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	19.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.6. AC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

11.6.1. V_{CCA} = 3.3 ± 0.3 V, V_{CCB} = 5.0 ± 0.5 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.5	ns
	t_{PHL}			—	1.4	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	13.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	15.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.6.2. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 5.0 ± 0.5 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.55	ns
	t_{PHL}			—	2.0	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	17.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	19.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.6.3. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (bus to bus)	t_{PLH}	(Note 1)	See Fig. 13.1, 13.3	—	0.65	ns
	t_{PHL}			—	2.4	
Output enable time	t_{PZL}		See Fig. 13.2, 13.4	—	21.0	ns
Output disable time	t_{PLZ}		See Fig. 13.2, 13.4	—	23.0	ns

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

11.7. Capacitive Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	3.3	3	pF
Switch terminal ON-capacitance	$C_{I/O}$	—	3.3	3.3	14	pF
Switch terminal OFF-capacitance	$C_{I/O}$	—	3.3	3.3	7	pF

12. DC Test Circuit

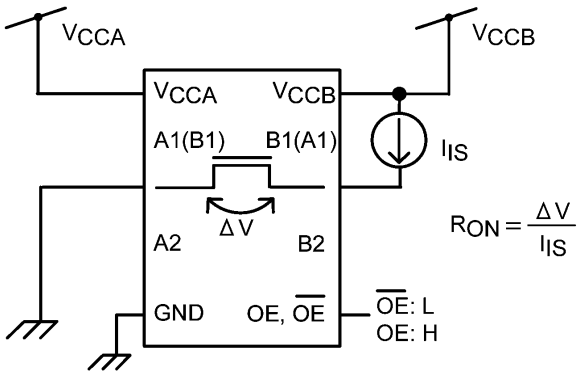


Fig. 12.1 ON-resistance Test Circuits

13. AC Test Circuits/Waveform

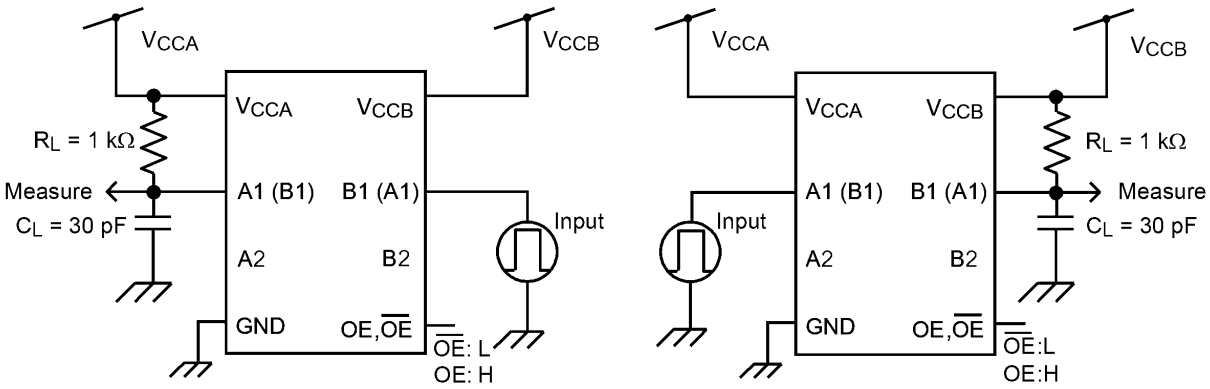


Fig. 13.1 t_{PLH}, t_{PHL} Test Circuits

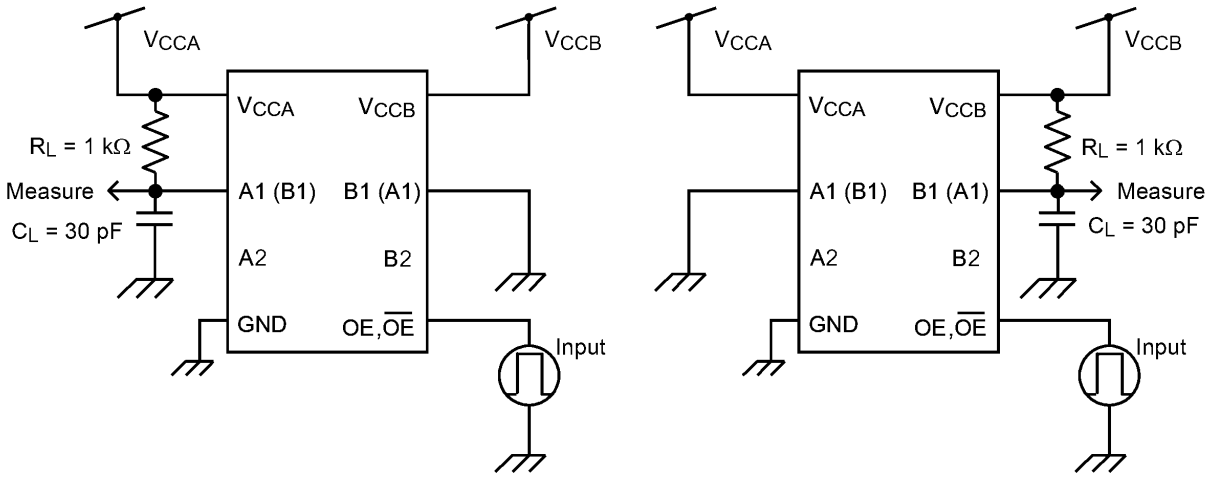


Fig. 13.2 t_{PLZ}, t_{PZL} Test Circuits

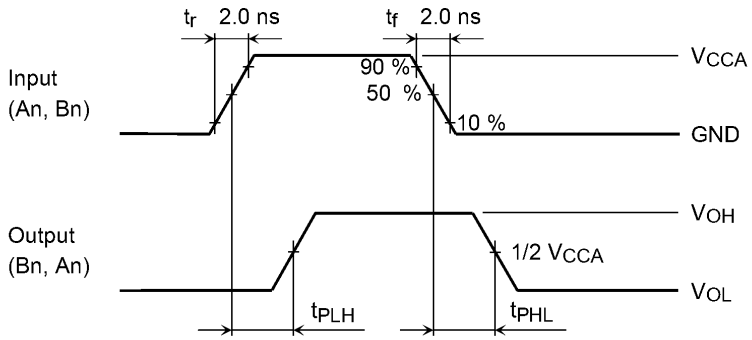


Fig. 13.3 AC Waveform of t_{PLH}, t_{PHL}

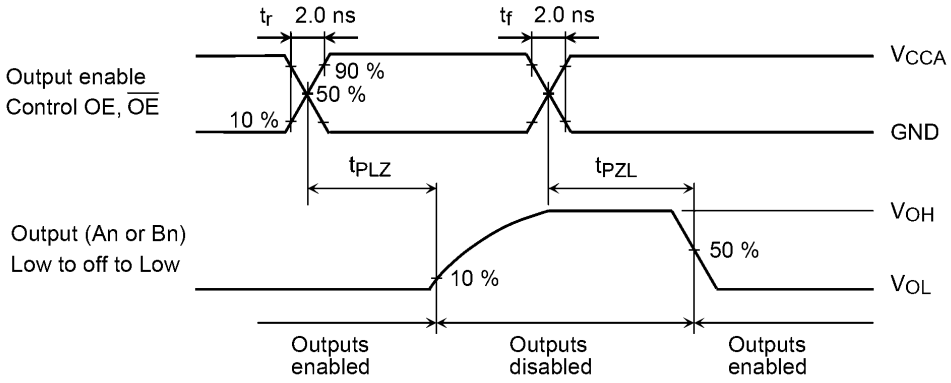


Fig. 13.4 AC Waveform of t_{PLZ}, t_{PZL}

14. Level Shift Function (Used Pull-up Resistance)

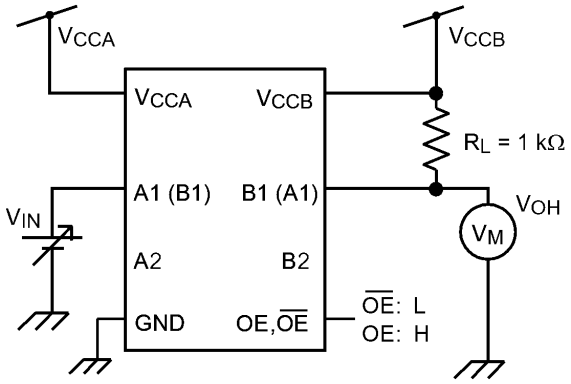


Fig. 14.1 Test Circuit

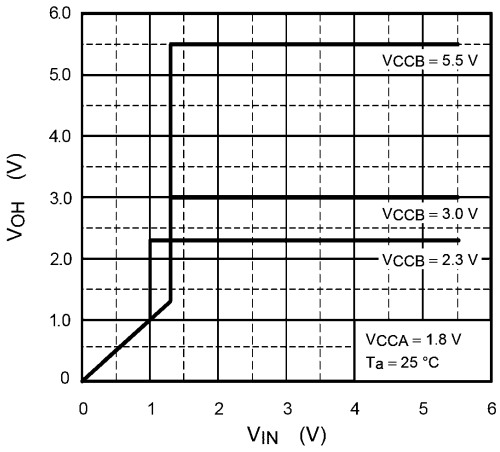


Fig. 14.2 Input/Output Characteristics (Typ.)
V_{CCA} = 1.8 V, T_a = 25 °C

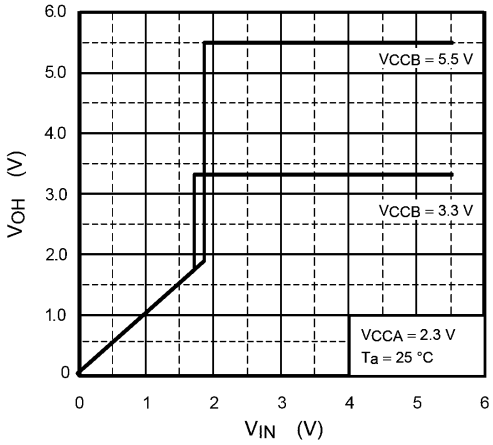


Fig. 14.3 Input/Output Characteristics (Typ.)
V_{CCA} = 2.3 V, T_a = 25 °C

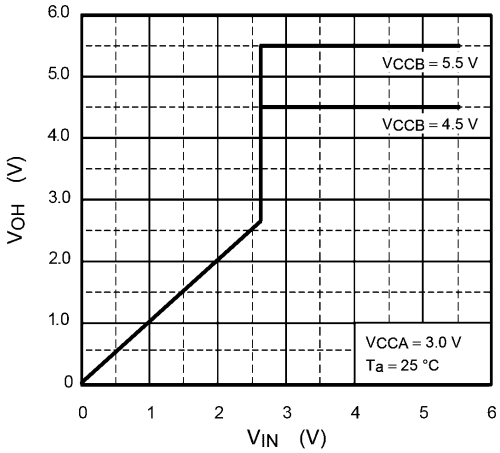


Fig. 14.4 Input/Output Characteristics (Typ.)
V_{CCA} = 3.0 V, T_a = 25 °C

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

15. Level Shift Function (Unused Pull-up Resistance)

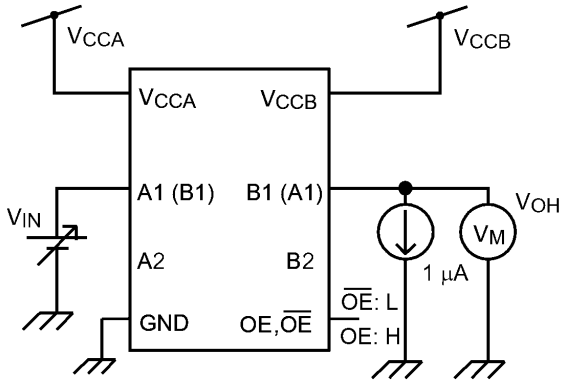


Fig. 15.1 Test Circuit

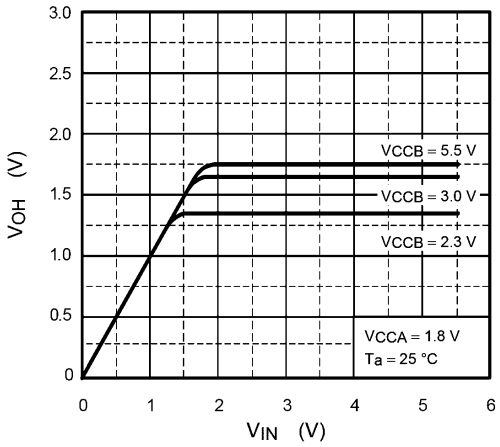


Fig. 15.2 Input/Output Characteristics (Typ.)
V_{CCA} = 1.8 V, T_a = 25 °C

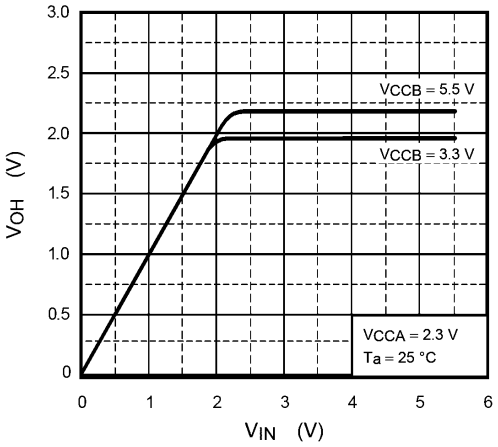


Fig. 15.3 Input/Output Characteristics (Typ.)
V_{CCA} = 2.3 V, T_a = 25 °C

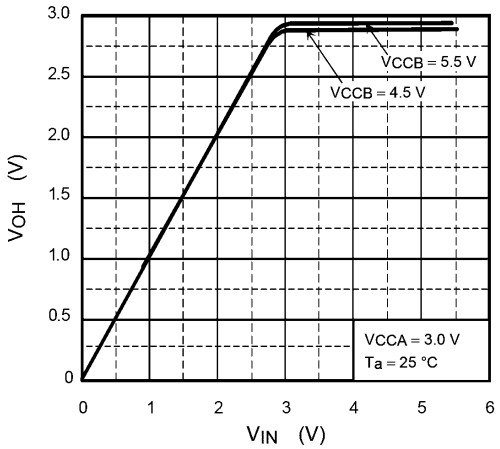
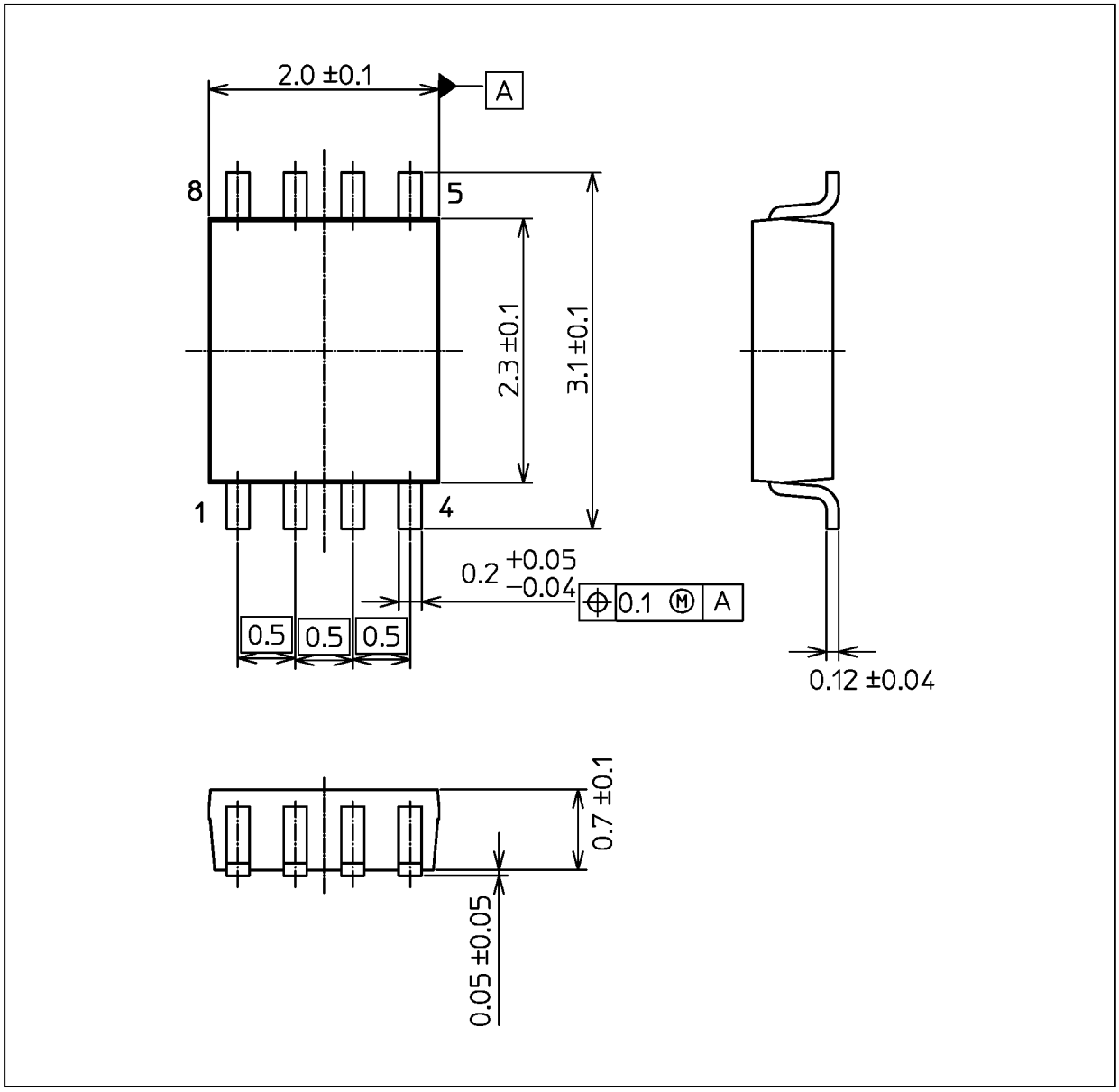


Fig. 15.4 Input/Output Characteristics (Typ.)
V_{CCA} = 3.0 V, T_a = 25 °C

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.01 g (typ.)

Package Name(s)
JEDEC: SOT-765
Nickname: US8

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